Application Report
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Dynamically Adjustable Output Using TPS63000

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ABSTRACT

This application report provides a schematic and design procedure for implementing a dynamically adjustable output for the TPS63000 using a digital-to-analog converter (DAC) or other input voltage source. Figure 1 shows a typical schematic of the implementation of the adjustable circuit.

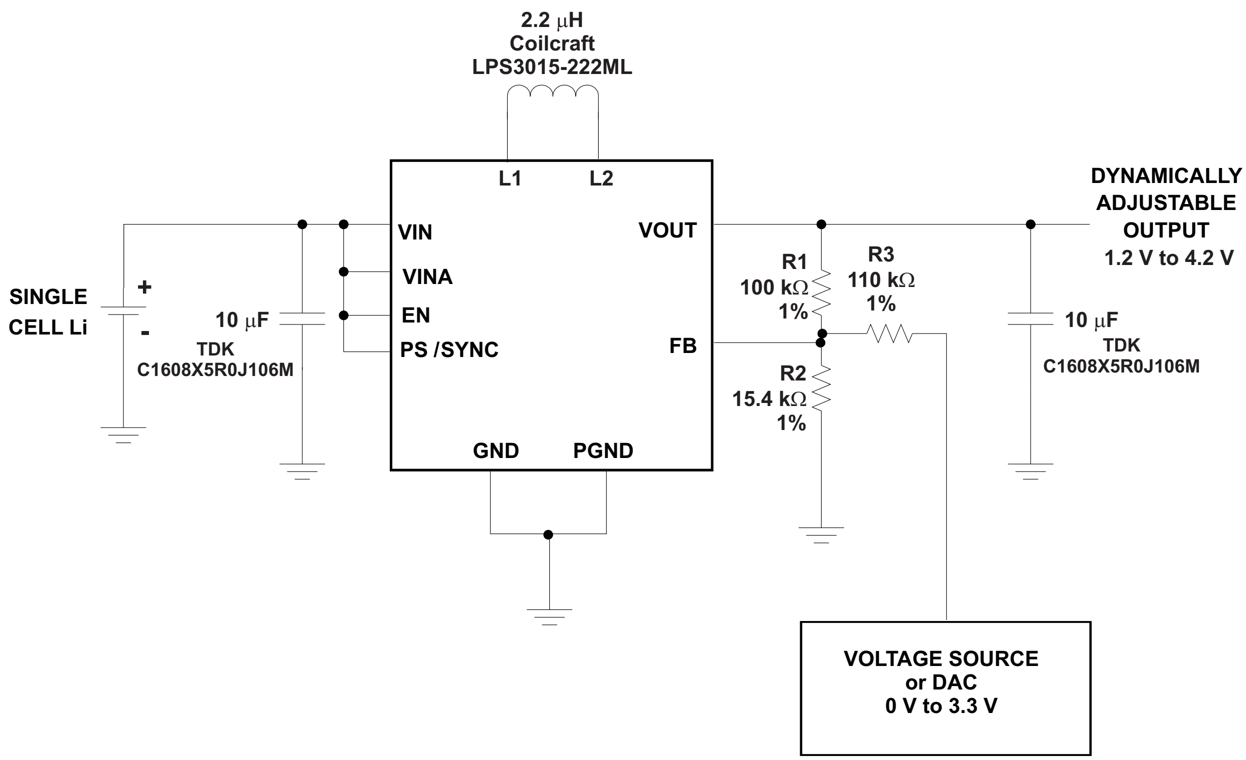

Figure 1. TPS63000 Schematic With Dynamically Adjustable Output

Begin by determining the required output voltage range and the maximum and minimum values for the adjustment input (VDACHI and VDACLOW, respectively). The maximum output voltage corresponds to the minimum adjustment input. R1, R2, and R3 set the ratio of VOUT to the VDAC_ voltage source. Choose R1 between 1 kΩ and 500 kΩ. Next, calculate R2 using Equation 1:

$$R2 = -V_{FB} \times R1 \times \frac{\left(V_{DACLOW} - V_{DACHI}\right)}{\left(V_{OUTLOW} - V_{OUTHI} + V_{DACLOW} - V_{DACHI}\right) \times V_{FB} - \left(V_{DACLOW} \times V_{OUTLOW}\right) + \left(V_{DACHI} \times V_{OUTHI}\right)} \quad (1)$$

Where V_{FB} = 0.5 V. The value for R3 then is determined by the Equation 2:

$$R3 = R2 \times R1 \times \frac{\left(V_{DACHI} - V_{FB}\right)}{\left(R2 \times V_{FB}\right) + \left(R1 \times V_{FB}\right) - \left(R2 \times V_{OUTLOW}\right)} \quad (2)$$

Note that the error between the expected ratio of $V_{DAC\_}$ to V_{OUT} and the actual ratio depends on the values of R1, R2, and R3. Choose high-precision resistors for the best results.

Example:

The circuit was tested in the laboratory under the following conditions:

V_{IN} = 3 V to 4.2 V, data taken at V_{IN} = 3.6 V

V_{OUT} = 1.2 V to 4.2 V

V_{DAC} = 0 V to 3.3V

R1 = 100 kΩ

The calculated values for R2 and R3 were found to be:

R2 = 15.4 kΩ

R3 = 110 kΩ

Standard value 1% resistors were used.

The comparison of calculated output values to actual values are shown in Figure 2.

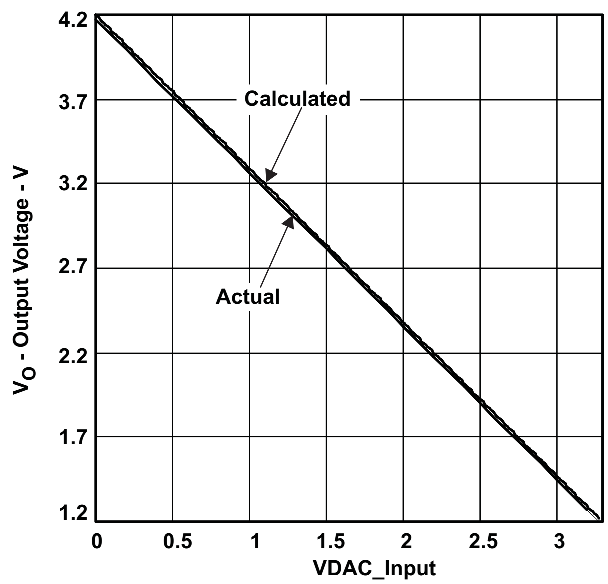

Figure 2. Output Voltage vs $V_{DAC\_}$ Input (V_{IN} = 3.6 V)

Note that the actual values were about 30 mV below the calculated values. This is due to the error in the 1% resistors as well as the tolerance of the internal reference. Note that the ratio for the actual data is nearly identical to calculated data.

This circuit also allows for fast transitions between voltage levels. Figure 3 shows a 40-mV step at $V_{DAC\_}$ and the corresponding change in the output in less than 20 µs.

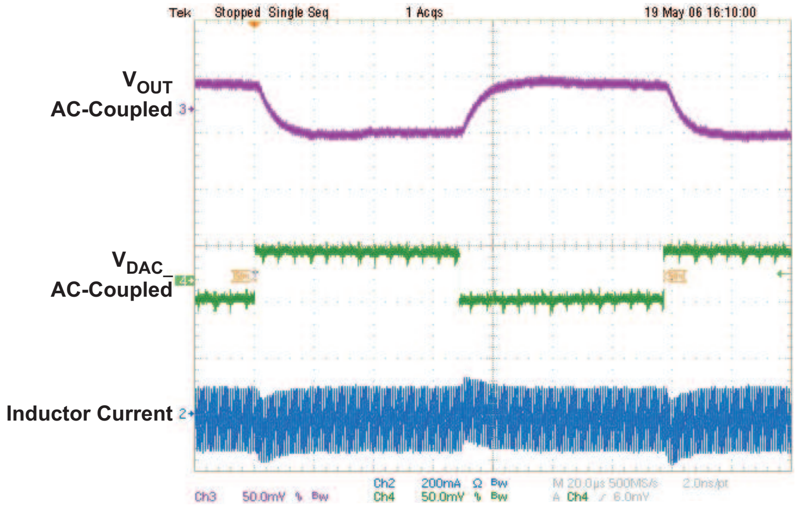

Figure 3. $V_{DAC\_}$ Step Response (V_{IN} = 3.6 V, No Load)

Note that little overshoot or undershoot results from the transition. As the $V_{DAC\_}$ step increases, the over/undershoot increases as shown in Figure 4 and Figure 5.

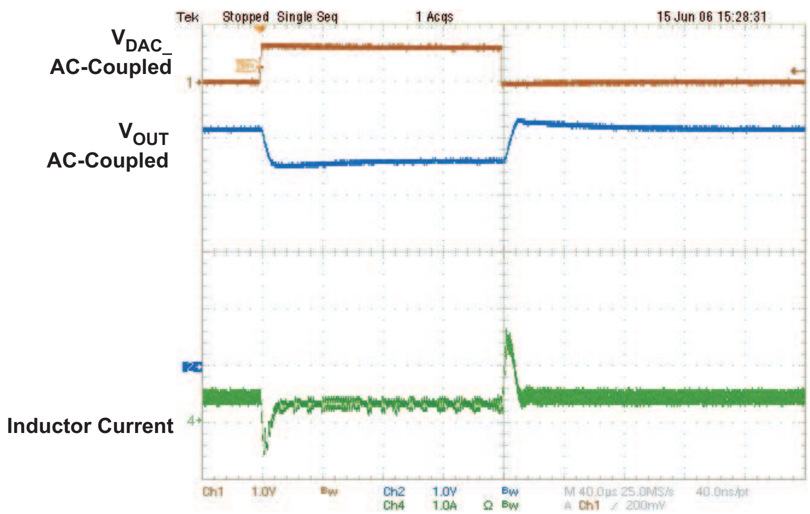

Figure 4. $V_{OUT\_}$ 4.2-V to 3.6-V Step Response (V_{IN} = 3.6 V, 15-Ω Load)

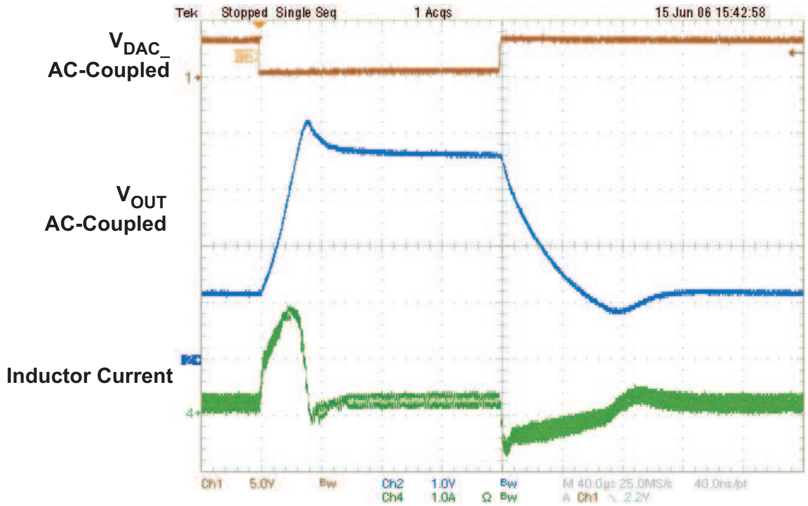

Figure 5. $V_{OUT\_}$ 1.2-V to 3.6-V Step Response (V_{IN} = 3.6-V, 15-Ω Load)

This does become an issue until the step exceeds about 300 mV. If the application requires a greater step than this, multiple smaller steps or a slow ramp should be used to reduce the amount of over/undershoot.

All of the previous data were taken in forced PWM mode. This circuit works in Power Save Mode (PSM) as well, although the speed of transition may be reduced. Note that the output range for the TPS63000 is 1.2 V to 5.5 V. The output accuracy is good over load and line and meets the specifications shown in the data sheet.

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