TEXAS INSTRUMENTS

Application Report
SLVA201–February 2005

Thermal Performance of SWIFT™ DC/DC Converters in the 28-Pin HTSSOP Package

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ABSTRACT

The thermal management of printed-circuit boards is complex, but must be well understood to achieve optimum performance and reliability. SWIFT™ dc/dc converters in the 28-pin HTSSOP package rely on an exposed lead frame die pad (PowerPAD™) on the bottom of the package to provide an extremely low thermal resistance from junction to case. The thermal performance of the 6-, 9-, and 14-A SWIFT devices is examined under varied ambient temperature and airflow conditions. A technique is demonstrated to measure actual junction temperatures of a device in a user's application circuit.

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1 Introduction

The 28-pin HTSSOP package is used for the TPS546xx, TPS548xx, TPS549xx and TPS540xx dc/dc converters. These devices offer output currents of 6, 8, 9, and 14 A, respectively. As the power FETs are integrated into the device, the power dissipation can be high at these output currents. Thermal management becomes an important factor in determining the performance and reliability of the design. The PowerPAD™ package is manufactured with the lead frame exposed on the under side of the package. This provides an extremely low thermal resistance between the integrated circuit die and the package. By soldering the exposed PowerPAD on the device directly to the PCB, the heat generated can be drawn away from the device. Thermal vias located under the device can be used to channel the heat directly to internal ground planes or other heat sinking structures built into the PCB.

2 SWIFT™ Devices Discussed in This Report

Table 1. SWIFT 28-Pin Devices

6-A Devices, 3- to 6-V Input	
TPS54610	Standard externally compensated adjustable output
TPS54611	Internally compensated 0.9-V fixed output
TPS54612	Internally compensated 1.2-V fixed output
TPS54613	Internally compensated 1.5-V fixed output
TPS54614	Internally compensated 1.8-V fixed output
TPS54615	Internally compensated 2.5-V fixed output
TPS54616	Internally compensated 3.3-V fixed output (3.7-V minimum input)
TPS54672	Adjustable regulator for tracking or bus termination applications
TPS54673	Adjustable regulator for precharged output applications
TPS54680	Adjustable regulator for sequencing applications
8-A Devices, 4- to 6-V Input	
TPS54810	Standard externally compensated adjustable output
TPS54872	Adjustable regulator for tracking or bus termination applications
TPS54873	Adjustable regulator for precharged output applications
TPS54880	Adjustable regulator for sequencing applications
9-A Devices, 3- to 4-V Input	
TPS54910	Standard externally compensated adjustable output
TPS54972	Adjustable regulator for tracking or bus termination applications
TPS54973	Adjustable regulator for precharged output applications
TPS54974	Dual input bus adjustable regulator
TPS54980	Adjustable regulator for sequencing applications
14-A Devices, 2.2- to 4-V Input	
TPS54010	Standard externally compensated adjustable output

Note that in Table 1 devices of each output current are pin compatible for a given application type. That is, all TPS54X10 are pin compatible, all TPS54X72 are pin compatible, etc.

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3 Test Methodology

From a thermal performance standpoint, the 28-pin SWIFT devices can be divided into three categories: the TPS546XX and TPS548XX devices, THE TPS549XX devices, and the TPS540XX devices. Representative devices were chosen for each type category, the TPS54610, TPS54974, and TPS54010, and were each tested in identical designs on identical PCB assemblies.

4 Printed-Circuit Board

The PCB used is the TPS54010EVM-067 evaluation module which is a 3-inch x 3-inch, four-layer PCB. All components are placed on the top side of the board as shown in Figure 1. The top layer contains most of the power and signal routing etch as well as a significant ground area as shown in Figure 2. Figure 3 and Figure 4 show the two internal ground plane layers. The bottom layer consists mostly of ground area along with an output voltage plane area and two additional signal traces. The bottom layer is shown in Figure 5.

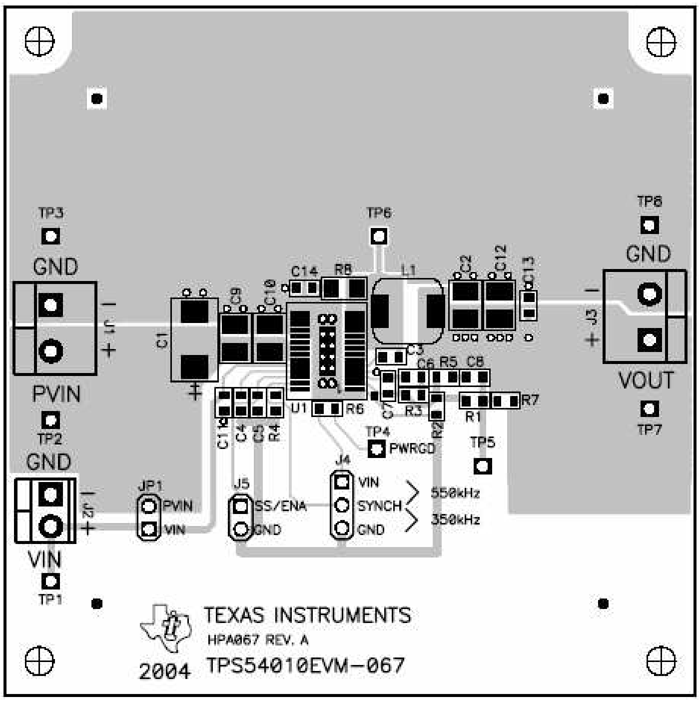

Figure 1. Top Side Assembly

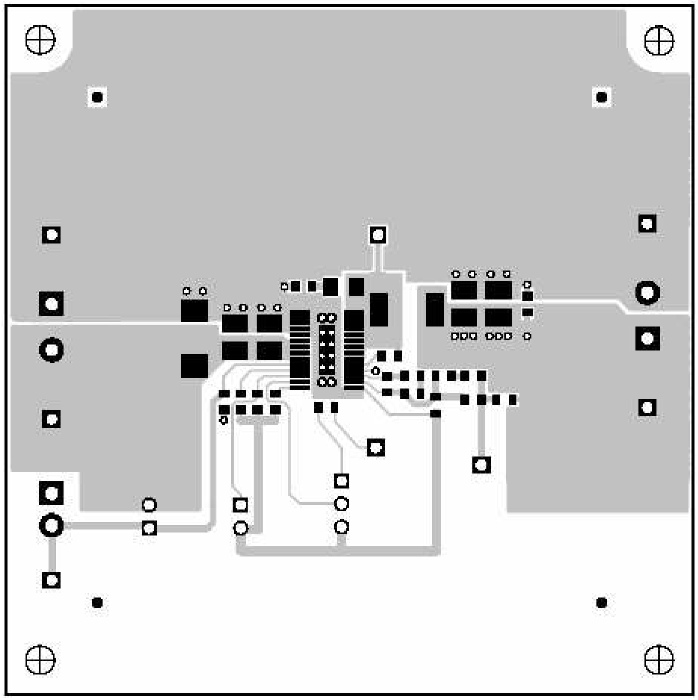

Figure 2. Top Side

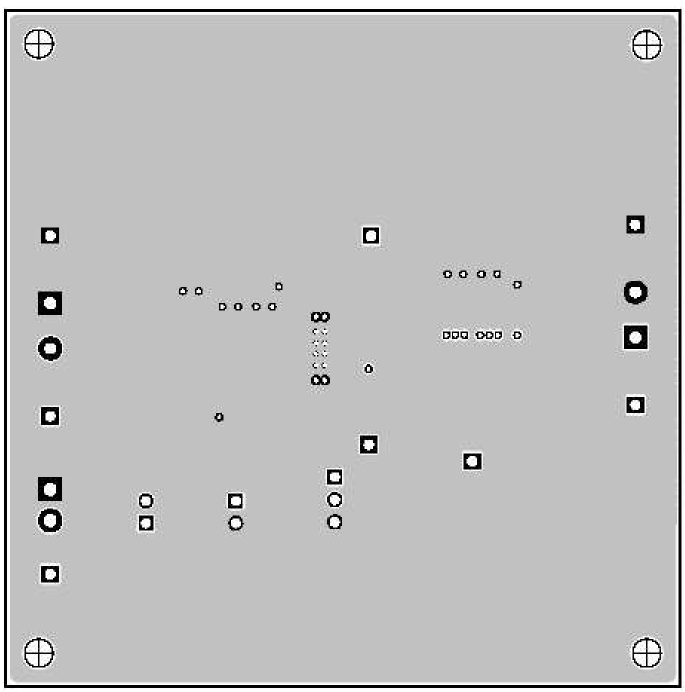

Figure 3. Internal Ground Layer 2

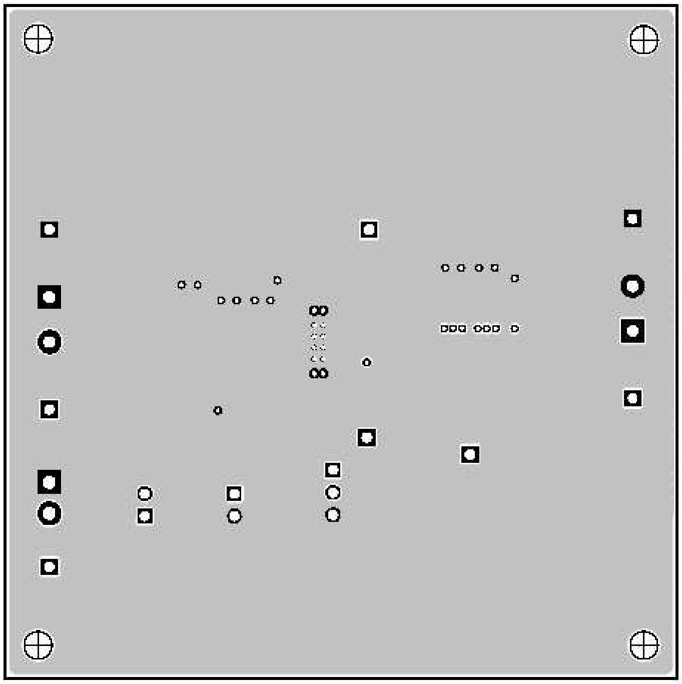

Figure 4. Internal Ground Layer 3

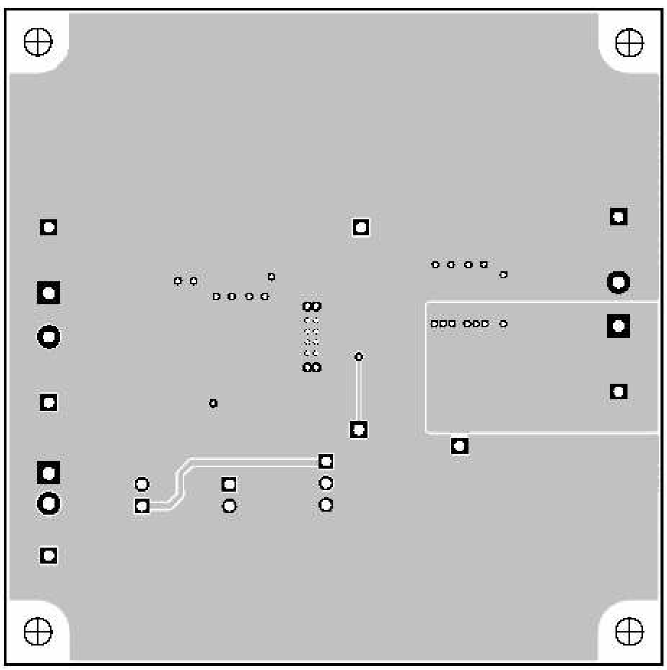

Figure 5. Bottom Layer

5 Schematic

The electrical schematic for the test board is shown in Figure 6. The output inductor is a Vishay IHLP-2525CZ-0.68 µH and the output filter capacitor is a 100-µF ceramic, TDK C3225X5R0J107M. The test board is set up with two input power connectors, J1 and J2, to support the split rail of the TPS54010. For these tests, JP1 is used to tie the VIN supply connection to PVIN, so that VIN = PVIN.

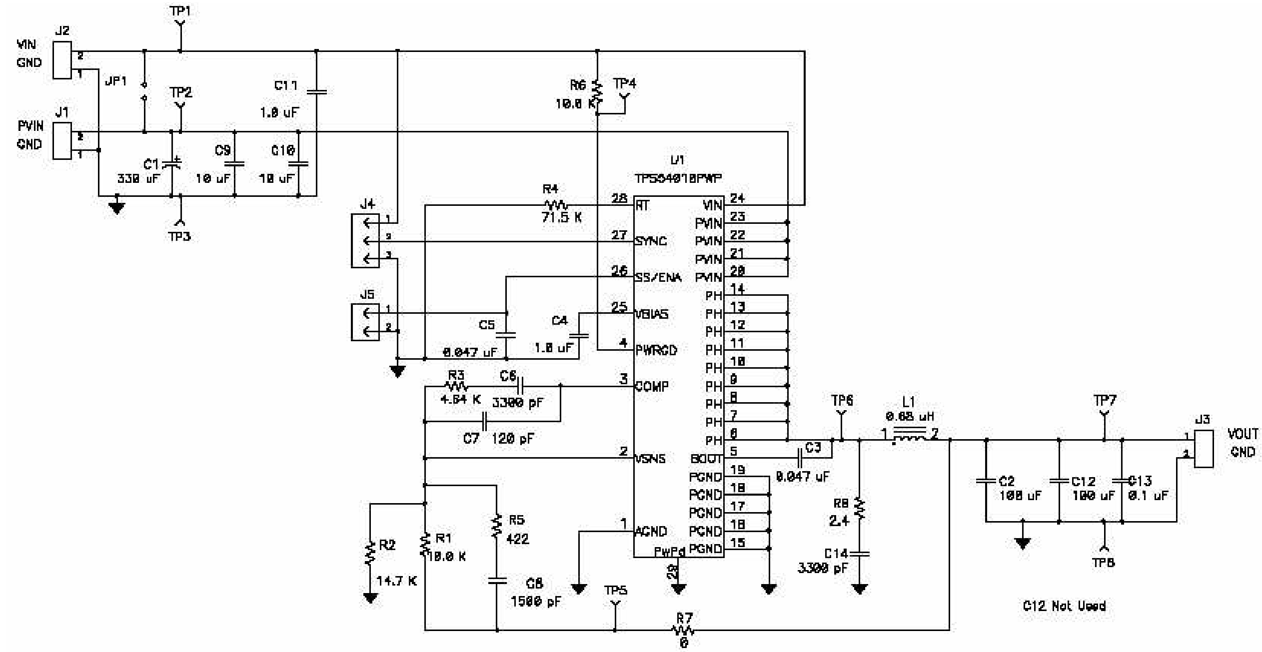

Figure 6. Electrical Schematic

5.1 Test Setup

To accurately measure the junction temperature of the device, it is possible to monitor the forward voltage drop of the internal drain-to-source body diode of the PWRGD open-drain FET. The diode is forward biased with a constant 300 µA current using the test setup of Figure 7.

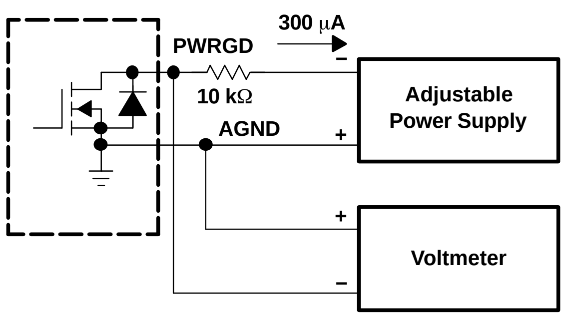

Figure 7. Test Setup

The first step in obtaining thermal data is to determine the diode forward voltage versus junction temperature characteristics. With no power applied to the VIN input PCB, measure the diode voltage at various ambient temperatures as shown in Table 2.

Table 2. Diode Voltage vs Temperature

T_J–° C	MEASURED DIODE VOLTAGE – V		
	TPS54610	TPS54974	TPS54010
25	0.6079	0.6129	0.6074
50	0.5457	0.5472	0.5465
75	0.4899	0.4900	0.4844
100	0.4363	0.4322	0.4219
125	0.3802	0.3751	0.3630

Plotting the data shows the linear relationship of the diode voltage to the junction temperature. A trend line can be used to easily determine the equation to express this relationship (see Figure 8, Figure 9, and Figure 10).

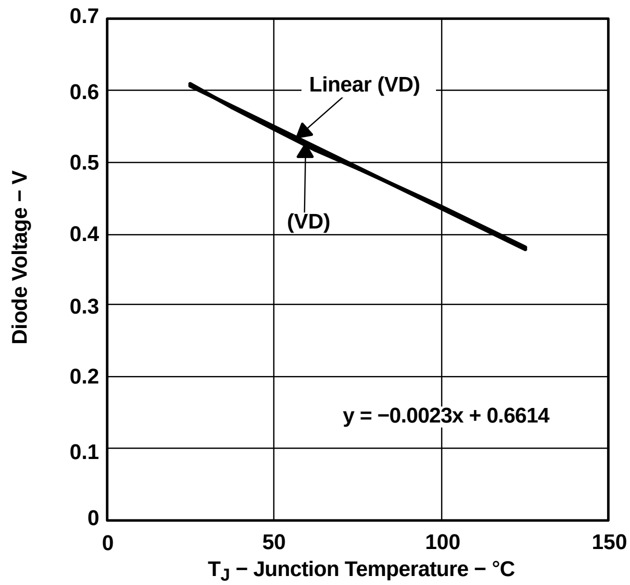

Figure 8. TPS54610 Diode Voltage vs Junction Temperature

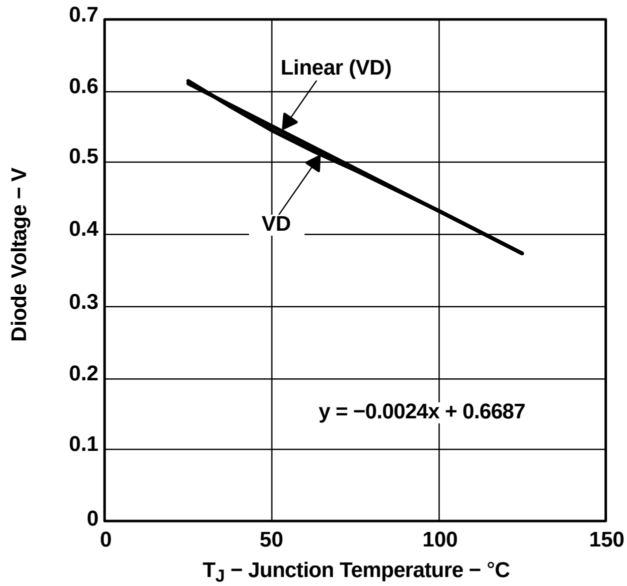

Figure 9. TPS54974 Diode Voltage vs Junction Temperature

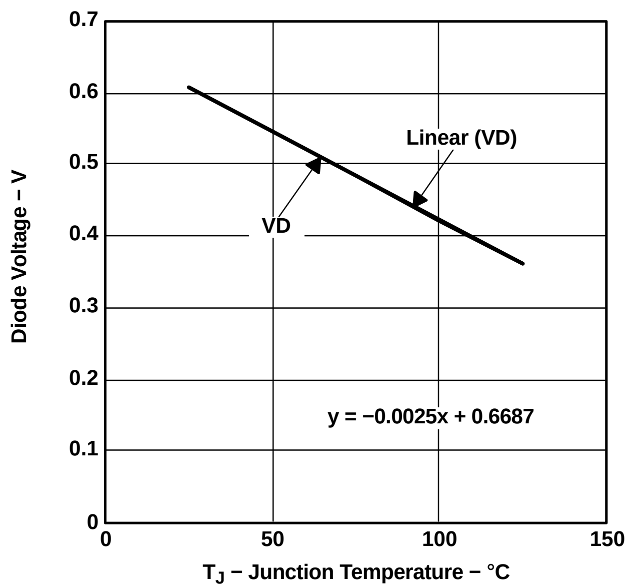

Figure 10. TPS54010 Diode Voltage vs Junction Temperature

The junction temperature as a function of diode voltage equations for each test board can be easily derived by rearranging the terms in the trend line equations:

$$T_J = \frac{V_D - 0.6614}{0.0023} \qquad \text{TPS54610}$$

$$T_J = \frac{V_D - 0.6687}{0.0024} \qquad \text{TPS54974}$$

$$T_J = \frac{V_D - 0.6687}{0.0025} \qquad \text{TPS54010}$$

5.2 Test Results

Now that the junction temperature to diode voltage characteristics are known, the thermal performance data can be taken and the junction to ambient thermal resistance can be calculated. At a known ambient temperature such as room ambient, it is necessary to calculate the device power dissipation and measure the diode voltage over the range of output currents for each device. Each test board was set up using identical input and output conditions, in this case, 3.3-V input and 1.5-V output. Power dissipation was determined by measuring the input voltage, input current, output voltage and output current. Because the high- and low-side FETs are integrated into the devices, the only other significant power loss is the series resistance of the inductor. The device power dissipation is then given by:

$$P_{DISS} = \left(V_{IN} \times I_{IN}\right) - \left(V_{OUT} \times I_{OUT}\right) - \left(I_{OUT}^2 \times R_{INDUCTOR}\right)$$

It is important to understand that these test PCBs contain only the power conversion circuitry. All load power is dissipated external to the PCB and does not contribute to the thermal measurements presented here.

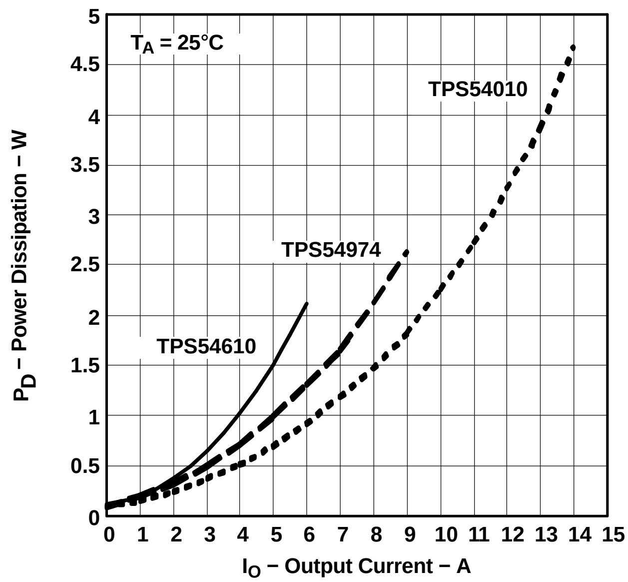

Figure 11. Device Power Dissipation vs Output Current

Figure 11 shows the device power dissipation as a function of output current for each of the three device types. Notice that for a given output current, the power dissipation is different for each device. This is primarily due to the difference in RDSon of the internal FETs. For the TPS54610, the FET on-resistance is nominally 30 mΩ. The FET on-resistance decreases to 15 mΩ for the TPS54974 and 8 mΩ for the TPS54010.

Figure 12 shows the junction temperature as a function of output current. The junction temperature characteristics are similar to the power dissipation characteristics in Figure 11, with higher junction temperatures at a given current for devices with higher RDSon.

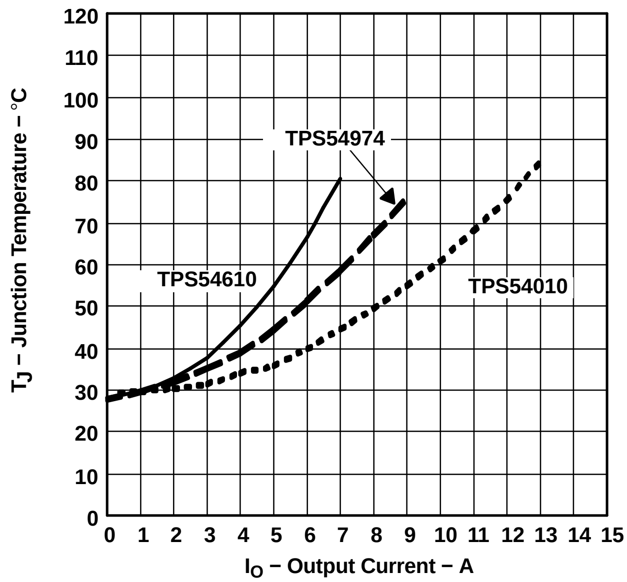

Figure 12. Device Junction Temperature vs Output Current

With the power dissipation and the junction temperatures of the devices known, the thermal resistance, θ_{JA}, can be determined. This parameter has the units of °C/W; so, the device temperature rise is plotted vs device power dissipation. These curves are shown in Figure 13.

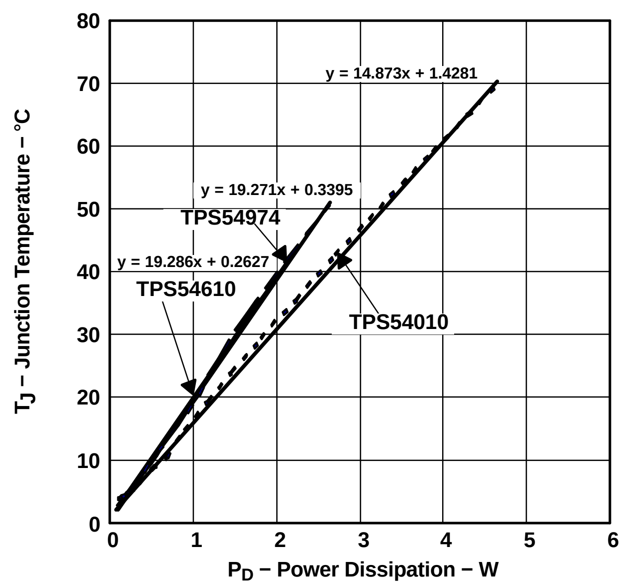

Figure 13. Junction Temperature Rise vs Device Power Dissipation

For each device, the junction temperature rise vs power dissipation curve is close to linear. The slope of this line, given by the coefficient of x in Figure 13, is the thermal resistance from junction to ambient for each of the test boards. For the TPS54610 and the TPS54974, the thermal resistance is essentially identical. This is to be expected as the two devices have the same die area. The TPS54010, however, has a larger die area, enabling better heat transfer to the PCB and corresponding lower thermal resistance.

6 Improving Thermal Performance

The junction-to-PowerPAD thermal resistance is extremely low, on the order of 1.2°C/W. Therefore, thermal performance of the these devices is almost completely dependent on outside factors. The two most important factors are PCB layout and ambient conditions. Assuming proper layout guidelines and device footprints are used, increasing the available heat-sinking area in the PCB can improve thermal performance. In the previous test cases, a 3-inch by 3-inch, four-layer PCB with two internal ground planes was tested. For comparison, a 4-inch by 4-inch, six-layer PCB with four internal planes was tested with the TPS54010. Figure 14 shows a comparison of the thermal resistances; Table 3 summarizes those resistances.

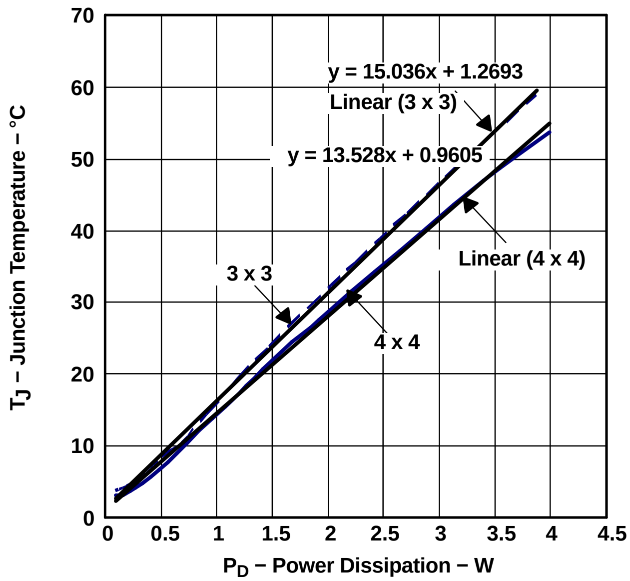

Figure 14. Board Area Comparison

In this case, the thermal resistance can be seen to decrease by about 1.5°C/W. The relatively small increase in performance is due to the fact that the available heat-sinking area in the 3-inch by 3-inch board is already quite large.

Another way to improve thermal performance is by providing airflow to the ambient condition. Figure 17 through Figure 16 show the safe-operating area for each device type with natural convection and with 200 LFM airflow. At lower output currents, the improvement is rather small. However, at higher output currents, the improvement is significant.

Table 3. Measured Thermal Resistance Summary

Device	Board	Thermal Resistance
TPS54610	3 x 3	19.27
TPS54974	3 x 3	19.27
TPS54010	3 x 3	14.95 (1)
TPS54010	4 x 4	13.53

(1) Average from data in Figure 13 and Figure 14.

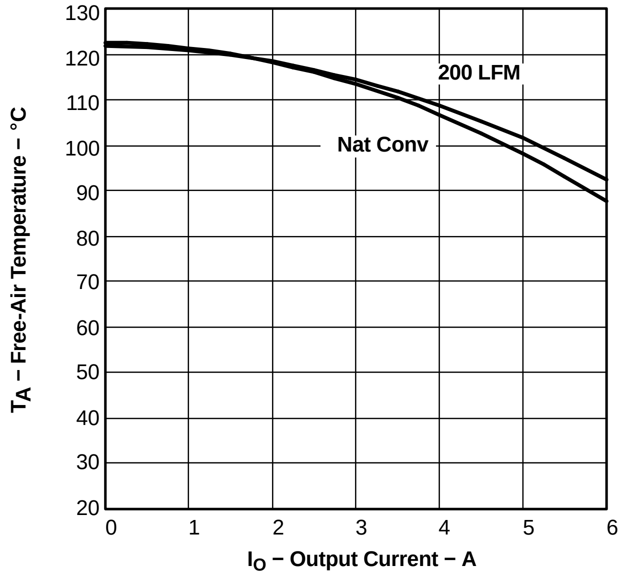

Figure 15. TPS54610 Safe-Operating Area with Airflow

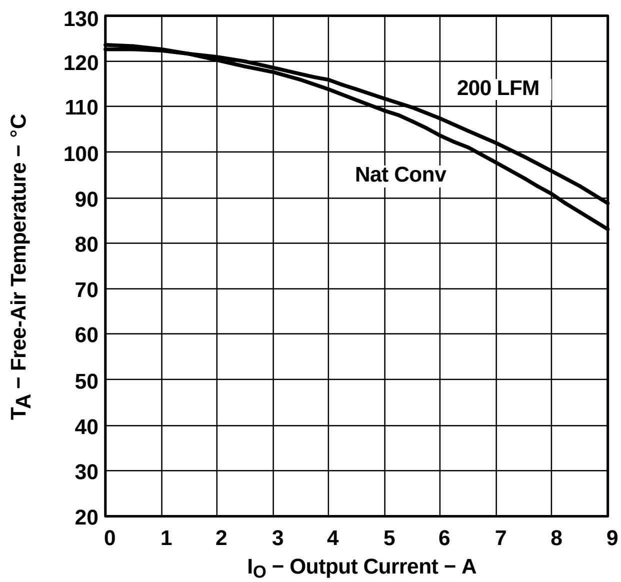

Figure 16. TPS54974 Safe-Operating Area with Airflow

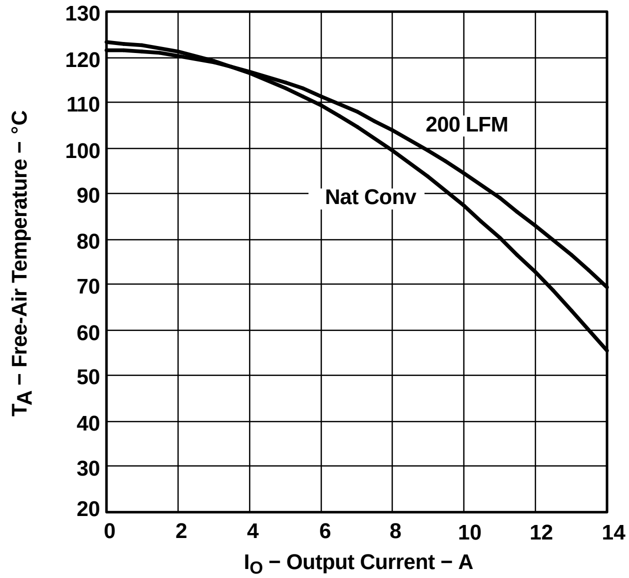

Figure 17. TPS54010 Safe-Operating Area with Airflow

7 Conclusions

For designs using the 28-pin HTSSOP package SWIFT devices, the thermal performance almost completely depends on the PCB design and layout. For optimal performance, always use the recommended footprint as provided in the device data sheets. Make sure that the device PowerPAD is soldered to the exposed copper area under the device. Increasing the amount of copper area used for heat sinking and providing for airflow can improve the thermal performance, especially in high-current applications. It is important to understand that the test results presented in this application report are only valid for the PCB configurations described herein. Results in other application circuits will vary. In typical applications, the SWIFT dc/dc converters will likely be used as point of load power supplies; the power dissipated at the load will contribute significantly to thermal performance as the heat dissipated by the load may be many times that dissipated in the SWIFT dc/dc converter. Using the technique described in the application report allows users to easily determine the thermal performance of their designs.

Although this application report deals specifically with the 28-pin HTSSOP package, the test methodology presented is valid for the 16- and 20-pin SWIFT PowerPAD devices as well.

For additional information, see the documents listed in the following references.

8 References

1. *PowerPAD Made Easy* (SLMA004)
2. *PowerPAD Thermally Enhanced Package* (SLMA002)
3. *Optimizing the Layout of the TPS5461X for Thermal Performance* (SLVA113)

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