UCD9240 Data Sheet Errata

These are the errata for the UCD9240 64-pin and UCD9240 80-pin devices.

Erratum #1

Address arbitration for a PMBus Alert Response event may not work when there is more than one device on the bus. Specifically, if two or more devices report an alert (via the PMBus-Alert signal) to the host and the host issues an Alert Response Address command (a Receive Byte command with address 12), the device with the lower PMBus address will win the arbitration and its address will be the one received by the host. The device with the higher PMBus address will be unaware that it lost arbitration, and the next command to the device with the higher PMBus address will be ignored. If the host sends a third Alert Response Address command and this device wins the arbitration, then the host will receive the higher address in response.

A simple workaround for this issue is to follow any Alert Response Address command with a PMBus STATUS_WORD command using the address that was received in the Alert Response message. Since this address will not be the address for the device that lost arbitration, it will clear the PMBus hardware for that device, allowing it to respond to the next Alert Response Address request on the PMBus.

This affects both the 64-pin and 80-pin devices.

Erratum #2

PMBus address bins 0, 1, 2, and 3 from the PMBus Address Bins Table of the UCD9240 datasheet are not reliably detected over process, temperature and component variations and should not be used. The 62 supported addresses are shown below.

		PMBus Address						
		Addr1						
		4	**5**	**6**	**7**	**8**	**9**	**10**
Addr0	4	52	64	76	88	100	112	124
	5	53	65	77	89	101	113	125
	6	54	66	78	90	102	114	126
	7	55	67	79	91	103	115	127
	8	56	68	80	92	104	116	
	9	57	69	81	93	105	117	
	10	58	70	82	94	106	118	
	11	59	71	83	95	107	119	

Refer to the “Resistor Programmed PMBus Address Decode” of the UCD9240 Datasheet (SLUS766) for more information about generating the supported addresses with the remaining allowed bins. Also, the restrictions regarding address 127 and 126 still apply.

This affects both the 64-pin and 80-pin devices.

Erratum #3

The Open-Drain output mode for the GPIO_SEQ_CONFIG command is not supported on the UCD9240 80-pin device. Please refer to the GPIO_SEQ_CONFIG command in the UCD92xx PMBus Command Reference (SLUU337).

Erratum #4

The Open-Drain Status output event type for the GPIO_SEQ_CONFIG command is not supported on the UCD9240 64-pin device. Refer to the GPIO_SEQ_CONFIG command in the UCD92xx PMBus Command Reference (SLUU337).

Erratum #5

A voltage offset may be introduced to the output if the AFE gain is different between CLA banks. The EADC_TRIM PMBus command was created so that the user could minimize this offset between two AFE gain settings. See the UCD92xx PMBus Command Reference (SLUU337) for more information on the EADC_TRIM command.

Erratum #6

When the AFE gain setting is different between CLA banks, there is a chance that the wrong AFE gain setting will be used to calculate the error between the reference voltage (Vref) and the sensed voltage at the EAP/EAN inputs. In normal operation the error is near zero and this does not affect the system. When there is a transient that causes the difference between the reference voltage and the sensed voltage to be large, the calculated error voltage may be larger or smaller than the actual error if the wrong AFE gain is used in the calculation.

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