BQ77307

Technical Reference Manual

Literature Number: SLUUCY8
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About This Manual

This technical reference manual (TRM) discusses the modules and peripherals of the BQ77307 device, and how each is used to build a complete battery pack monitor and protection solution. For details on the hardware device features and electrical specifications, see the *BQ77307 2-Series to 7-Series High Accuracy Battery Primary or Secondary Protector for Li-Ion, Li-Polymer, LiFePO$_4$ (LFP), and LTO Battery Packs* data sheet.

Battery Notational Conventions

The following notation is used if commands, subcommands, and data memory values are mentioned within a text block:

- Commands and subcommands: *italics* with parentheses and no breaking spaces; for example, *Battery Status()*
- Data memory: *italics*, **bold**, and breaking spaces; for example, ***Power Config***
- Register bits and flags: *italics* and brackets; for example, *[SCD]*
- Data memory bits: *italics* and **bold**; for example, ***[FET_EN]***
- Modes and states: ALL CAPITALS; for example, DEEPSLEEP

Trademarks

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Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

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Chapter 1

Introduction

The Texas Instruments BQ77307 provides a highly integrated, high accuracy battery primary and secondary protector for 2-series to 7-series Li-Ion, Li-Polymer, $LiFePO_4$ (LFP), and LTO battery packs. Each device includes a high accuracy voltage, current, and temperature protection subsystem, with integrated low-side protection NFET drivers, and a programmable LDO for external system use. The BQ77307 provides an interrupt to a host processor and integrates an I^2C host communication interface supporting up to 400-kHz operation with optional CRC to read status information. Device features include:

- Primary or secondary voltage, current, and temperature protection for 2-series to 7-series cells with autonomous recovery option
- Integrated low-side drivers for NFET protection with optional autonomous recovery
- Low power operation
  - NORMAL mode with both FET drivers enabled: 8 µA
  - NORMAL mode with FET drivers disabled: 6 µA
  - SHUTDOWN Mode: < 1 µA
- High voltage tolerance of 45 V on cell connect and select additional pins
- Support for temperature protections using internal sensor and external thermistor
- Integrated one-time-programmable (OTP) memory for device settings, programmed by TI
- 400-kHz I^2C serial communications with optional CRC support
- Programmable LDO for external system usage

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2.1 Overview

The BQ77307 product is a highly integrated, accurate battery primary or secondary protector for 2-series to 7-series Li-Ion, Li-Polymer, $LiFePO_4$ (LFP), and LTO battery packs. A feature-rich and highly configurable protection subsystem provides a wide set of protections which can be triggered and recovered completely autonomously by the device or under full control of a host processor. Integrated FET drivers drive low-side charge and discharge protection NFETs. A programmable LDO is included for external system use, with voltage programmable to 1.8 V, 2.5 V, 3.0 V, 3.3 V, or 5.0 V, capable of providing up to 20 mA.

The BQ77307 device includes one-time-programmable (OTP) memory which TI programs to configure default device operation settings, for systems where a host processor is not available to configure the device. Alternatively, a host processor can be connected to the device I^2C interface and configure settings in the field, depending on customer preference. A 400-kHz I^2C communication interface and ALERT interrupt output enable communication with a host processor. The device supports protections using an external thermistor as well as the internal die temperature. Figure 2-1 shows the BQ77307 block diagram.

2.2 Functional Block Diagram

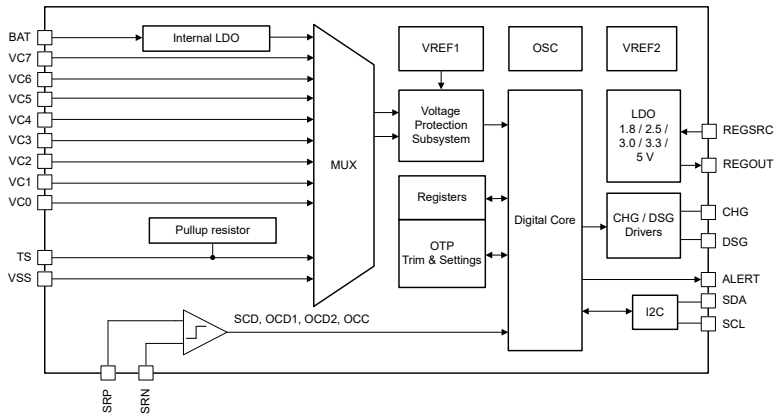

Figure 2-1. BQ77307 Block Diagram

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Chapter 3

Device Configuration

3.1 Direct Commands and Subcommands

The BQ77307 device includes support for direct commands and subcommands. The direct commands are accessed using a 7-bit command address that is sent from a host through the device serial communications interface and either triggers an action, or provides a data value to be written to the device, or instructs the device to report data back to the host. Subcommands are additional commands that are accessed indirectly using the 7-bit command address space and provide the capability for block data transfers.

When a subcommand is initiated, a 16-bit subcommand address is first written to the 7-bit command addresses 0x3E (lower byte) and 0x3F (upper byte). The device initially assumes a read-back of data is needed, and auto-populates existing data into the 32-byte transfer buffer (which uses 7-bit command addresses 0x40–0x5F), and writes the checksum for this data into address 0x60. If the host instead intends to write data into the device, the host overwrites the new data into the transfer buffer, a checksum for the data into address 0x60, and the data length into address 0x61.

As soon as address 0x61 is written, the device checks the checksum written into 0x60 with the data written into 0x40-0x5F, and if this is correct, it proceeds to transfer the data from the transfer buffer into the device's memory. The checksum is the 8-bit modulo-256 sum of the subcommand bytes (0x3E and 0x3F) and the bytes used in the transfer buffer, then the result is bit-wise inverted. The verification cannot take place until the data length is written, so the device realizes how many bytes in the transfer buffer are included. Write the data length last, after the checksum has been written (they do not need to be written together as a word). The data length includes the two bytes in 0x3E and 0x3F, the two bytes in 0x60 and 0x61, and the length of data in the transfer buffer. Therefore, if the entire 32-byte transfer buffer is used, the data length is 0x24.

When the data length in 0x61 is read, the device automatically increments the address presently in 0x3E and 0x3F by 0x0020, and populates the transfer buffer with new readback data. This allows large portions of data memory to be read by continuous reading of the address space 0x40 to 0x61. If the host attempts to read the transfer buffer data starting at 0x40 while the device is still loading the data into the transfer buffer, the device clock stretches the I2C read transaction until the data is available.

Some subcommands are only used to initiate an action and do not involve sending or receiving data. In these cases, the host can simply write the subcommand into 0x3E and 0x3F, and it is not necessary to write the length and checksum or any further data. Note that if an auto-incremented address corresponds to a subcommand that does not involve data, the auto-incrementing does not cause that subcommand to be initiated.

The commands supported in the device are described in Commands and Subcommands. Single-byte commands are direct commands, while two-byte commands are subcommands. Data formats are described in Data Formats.

The most efficient approach to read the data from a subcommand (to minimize bus traffic) is shown below:

1. Write lower byte of subcommand to 0x3E.
2. Write upper byte of subcommand to 0x3F.
3. Read back the subcommand from 0x3E and 0x3F, which echoes back the subcommand address sent in steps 1 and 2 (or the auto-incremented address from step 6).
4. Read buffer starting at 0x40 for the expected length (reading the full 32 bytes is also acceptable).
5. Read the checksum at 0x60 and verify it matches the data read over the length specified by the subcommand.

6. If auto-incrementing is desired, read the data length at 0x61, at which point the device increments the address in 0x3E and 0x3F by 32 and repopulates the buffer with the next 32 bytes of data, then go to step 2.

Note

0x61 provides the length of the buffer data plus 4 (that is, length of the buffer data plus the length of 0x3E and 0x3F plus the length of 0x60 and 0x61).

The checksum is calculated over 0x3E, 0x3F, and the length of buffer data specified by the subcommand, and it does not include the checksum or length in 0x60 and 0x61.

Write only 0 to command or subcommand bits denoted RSVD_0. Write only 1 to bits denoted RSVD_1.

3.2 Configuration Using OTP or Registers

The BQ77307 device includes Data Memory registers with values stored in digital logic, as well as one-time programmable (OTP) memory, which holds device trim information and default settings for registers. At initial power-up or after a reset, the device loads the OTP settings into registers, which are used by the device logic during operation. If the device is unsealed, it can also perform a reset on demand if the *0x0012 RESET()* subcommand is sent. Register values are preserved while the device is in NORMAL mode. If the device enters SHUTDOWN mode or a reset occurs, all register memory is cleared, and the device returns to the programmed OTP parameters when powered again.

The OTP memory is written by TI during device manufacturing and cannot be modified by the customer. A customized OTP configuration can be developed and programmed into a custom device by TI, depending on business terms.

The device supports several different potential use cases:

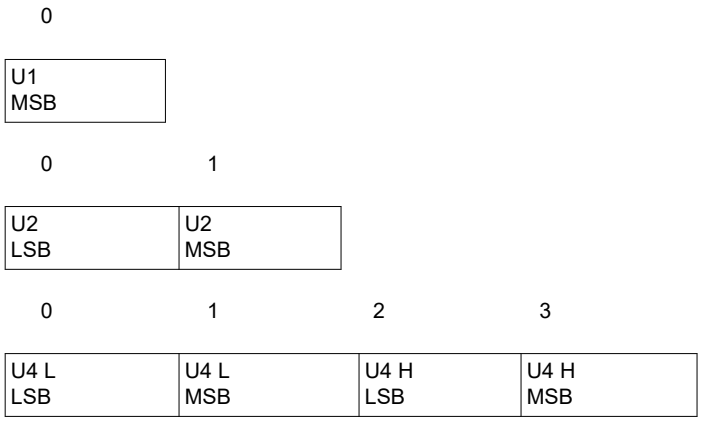
- **Standalone operation** - a customized OTP configuration is programmed into a custom device by TI. At each powerup of the device, it loads settings from OTP and operate autonomously without needing any host processor interaction. The I^2C bus on the device is not connected. If interested in this option, please contact TI for further discussion.
- **Autonomous operation with status information** - as above, the device is configured using a customized OTP programmed by TI. While the device does not *require* host interaction, a host processor can receive an interrupt whenever a protection alert or fault occurs and can query the device over I^2C to determine what event initiated the interrupt. In this case, the host processor is not involved in configuring protection settings, so is not necessarily involved in safety critical functionality. The OTP configuration can optionally allow the host processor to control the FET drivers over I^2C, or they can be set for only autonomous operation by the device itself.
- **Autonomous operation with configuration/status access** - as in **Autonomous operation with status information**, the device OTP is programmed by TI into a custom device, and the host processor can receive interrupts and check status information over I^2C. In addition, the host can use a security key to unseal the device and modify settings in registers from their preprogrammed values loaded from OTP.
- **Programmable operation with configuration/status access** - if a custom device from TI with OTP preprogrammed with settings is not desired or practical, then the device can be configured by a host processor over I^2C, either in the field or on the customer production line. In the field, any time the device is powered from SHUTDOWN mode, the host can configure the desired settings before the FETs are enabled. If a host processor is not included in the pack, then the customer can program the device on the production line, then leave it powered continuously thereafter in field operation. Status information is also available over I^2C during operation, even if the settings have been locked with the security key.

The OTP memory also includes a digital signature, which is stored in OTP. When the device is first powered or after a reset, it reads the OTP settings and check that the signature matches that stored, to provide robustness against bit errors in reading or corruption of the memory. If a signature error is detected, the device enters SHUTDOWN mode.

3.3 Data Formats

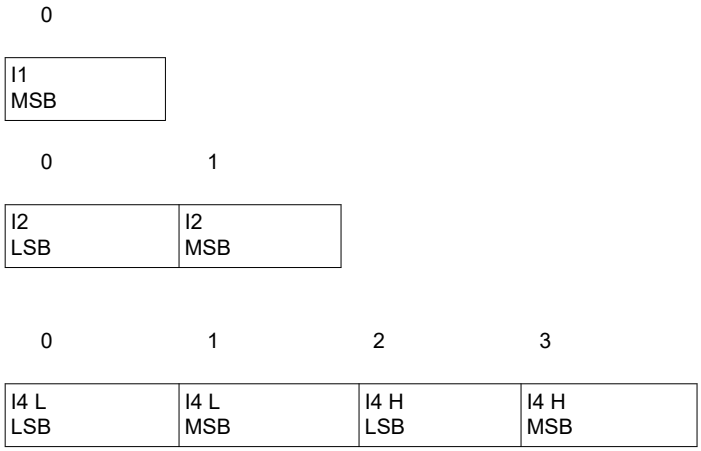
3.3.1 Unsigned Integer

Unsigned integers are stored without changes as 1-byte, 2-byte, or 4-byte values in little endian byte order.



3.3.2 Integer

Integer values are stored in 2's-complement format in 1-byte, 2-byte, or 4-byte values in little endian byte order.



3.3.3 Hex

Bit register definitions are stored in unsigned integer format.

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Chapter 4
Device Security

The BQ77307 device includes two security modes: SEALED and FULLACCESS, which can be used to limit the ability to view or change settings.

In SEALED mode, most data and status can be read using commands and subcommands, but only selected settings can be changed. Data memory settings cannot be read or changed directly.

FULLACCESS mode includes SEALED mode functionality, adds the ability to execute additional subcommands, and provides capability to read and modify all device settings.

Selected settings in the device can be modified while the device is in operation through supported commands and subcommands, but in order to modify all settings, the device must enter CONFIG_UPDATE mode, which stops device operation while settings are being updated. After the update is completed, device operation is restarted using the new settings. CONFIG_UPDATE mode is only available in FULLACCESS mode.

The BQ77307 device implements a key-access scheme to move from SEALED to FULLACCESS mode. A unique set of keys must be sent to the device through the subcommand address (0x3E and 0x3F). The keys must be sent consecutively to 0x3E and 0x3F, with no other data written between the keys. Do not set the two keys to identical values, and it is recommended to not use keys which are identical to subcommand addresses. When in SEALED mode, the *0x12 Battery Status()[SEC1, SEC0]* bits are set to [1, 1]. When the FULLACCESS keys are correctly received by the device, the bits are set to [0, 1]. The state [0, 0] is not valid and only indicates that the state has not yet been loaded. The state [1, 0] is also not valid.

The FULLACCESS keys are stored in data memory in ***Security:Full Access Key Step 1*** and ***Security:Keys:Full Access Key Step 2***. The access keys are changed during operation using the *0x0035 SECURITY_KEYS()* subcommand. This subcommand enables a R/W of the 2 key words (4 bytes). Each word is sent in little endian order using this subcommand.

When using the codes by writing them to 0x3E and 0x3F, they must be sent in little endian order; therefore, if 0x1234 and 0x5678 are written as the FULLACCESS codes to *0x0035 SECURITY_KEYS()*, then to unseal requires writing 0x34 and 0x12 to 0x3E and 0x3F, followed by writing 0x78 and 0x56 to 0x3E and 0x3F. The two codes must be written within 5 s of each other to succeed.

To read the keys (only available in FULLACCESS mode, assume for example the keys are 0x1234 0x5678):

1. Write 0x35 and 0x00 to 0x3E and 0x3F
2. Read back 4 bytes from the transfer buffer at 0x40–0x43 (for example, 0x34 0x12 0x78 0x56).

To write the keys (only available in FULLACCESS mode):

1. Write 0x35 and 0x00 to 0x3E and 0x3F.
2. Write the data in little endian format to the transfer buffer at 0x40–0x43 (for example, 0x34 0x12 0x78 0x56).
3. Write the checksum to 0x60. The checksum is calculated by inverting the modulo-256 sum of the data and command bytes (for example, 0xB6).
4. Write the length of 0x08 to 0x61. The length includes the command, data, checksum, and length bytes.

To set the device into SEALED mode when initially powering up, the ***Security:Security Settings[SEAL]*** configuration bit must be programmed into OTP. During operation, a device in FULLACCESS mode can be put into SEALED mode by sending the *0x0030 SEAL()* subcommand.

The BQ77307 device includes additional means to limit further modification of device settings. If the ***Security:Security Settings[LOCK_CFG]*** configuration bit is set, the data memory settings can no longer be modified when the device exits CONFIG_UPDATE mode. If the ***Security:Security Settings[PERM_SEAL]*** bit is set, the device cannot be unsealed after it has been sealed. If these bits are not set in OTP, the settings are lost on a full reset and the device is again able to unseal and modify data memory.

The catalog, uncustomized BQ77307 device is by default in FULLACCESS mode, so all settings can be configured in registers by the customer. If a customized, preprogrammed device is developed by TI, and the device is intended to only be used in standalone mode, then it can be preprogrammed with the ***Security:Security Settings[PERM_SEAL]*** bit set, such that settings can never be changed. If instead the customer wants the option to change settings on their production line or in the field, then the customer can use custom preprogrammed security keys to unseal the device and make changes, then can reseal the device again.

Chapter 5

Protection Subsystem

5.1 Protections Overview

The BQ77307 integrates an extensive protection subsystem which can monitor a variety of parameters, initiate protective actions, and autonomously recover based on conditions. The device also includes a wide range of flexibility, such that the device can be configured to monitor and initiate protective action, but with recovery controlled by a host processor, or such that the device only monitors and alerts the host processor whenever conditions warrant protective action, but with action and recovery fully controlled by the host processor. The protection subsystem includes a suite of individual protections that can be individually enabled and configured, as shown in Table 5-1. Some protection checks are primarily for diagnostic purposes, so the device can be autonomously disabled if a malfunction is detected. The device integrates NFET drivers for low-side CHG and DSG protection FETs, which can be configured in a series or parallel configuration.

Table 5-1. BQ77307 Protections

Protection	Description
Cell Undervoltage	Detects individual cell voltage below programmed threshold
Cell Overvoltage	Detects individual cell voltage above programmed threshold
Overcurrent in Charge	Detects charging current above programmed threshold
Overcurrent in Discharge 1 / 2	Two levels of detection for discharging current beyond programmed thresholds
Short Circuit in Discharge	Detects discharging current above programmed threshold
Undertemperature in Charge	Detects thermistor voltage below programmed threshold limit for charging operation
Overtemperature in Charge	Detects thermistor voltage above programmed threshold limit for charging operation
Undertemperature in Discharge	Detects thermistor voltage below programmed threshold limit for discharging operation
Overtemperature in Discharge	Detects thermistor voltage above programmed threshold limit for discharging operation
Internal Overtemperature	Detects internal device temperature above programmed threshold
REGOUT LDO Check	Diagnostic check - detects voltage or temperature fault on REGOUT regulator when enabled
Voltage Reference Check	Diagnostic check which compares VREF1 and VREF2, to detect if one varies significantly versus the other.
VSS Check	Diagnostic check on internal mux - device periodically switches the mux to VSS and detects if the level exceeds an expected threshold.

The individual protections are enabled by setting the related ***Settings:Protection:Enabled Protections A – B*** data memory configuration registers. Most protections include a programmable threshold, and when the monitored parameter first exceeds the programmed threshold, a protection alert is asserted. After the parameter remains beyond the threshold for a programmable delay period, a protection status fault is asserted (and the alert is deasserted). The protection alerts are provided by the *0x02 Safety Alert A()* and *0x04 Safety Alert B()* commands, while the protection status faults are provided by the *0x03 Safety Status A()* and *0x05 Safety Status*

B() commands, as shown below. Most protections also include a programmable recovery criteria, such that if the parameter no longer exceeds the threshold by some margin, the protection status fault is deasserted. Protection alert and status faults can be mapped to provide an interrupt to the host processor on the ALERT pin, using the *0x62 Alarm Status()*, *0x64 Alarm Raw Status()*, and *0x66 Alarm Enable()* commands.

Table 5-2. Format for 0x02 Safety Alert A()

Bit	Name	Description
7	COV	Cell Overvoltage Safety Alert
6	CUV	Cell Undervoltage Safety Alert
5	SCD	Short Circuit in Discharge Safety Alert
4	OCD1	Overcurrent in Discharge 1 Safety Alert
3	OCD2	Overcurrent in Discharge 2 Safety Alert
2	OCC	Overcurrent in Charge Safety Alert
1-0	RSVD0	Reserved

Table 5-3. Format for 0x03 Safety Status A()

Bit	Name	Description
7	COV	Cell Overvoltage Safety Fault
6	CUV	Cell Undervoltage Safety Fault
5	SCD	Short Circuit in Discharge Safety Fault
4	OCD1	Overcurrent in Discharge 1 Safety Fault
3	OCD2	Overcurrent in Discharge 2 Safety Fault
2	OCC	Overcurrent in Charge Safety Fault
1	CURLATCH	Current Protection Latch Safety Fault
0	REGOUT	REGOUT Safety Fault

Table 5-4. Format for 0x04 Safety Alert B()

Bit	Name	Description
7	OTD	Overtemperature in Discharge Safety Alert
6	OTC	Overtemperature in Charge Safety Alert
5	UTD	Undertemperature in Discharge Safety Alert
4	UTC	Undertemperature in Charge Safety Alert
3	OTINT	Internal Overtemperature Safety Alert
2	RSVD0	Reserved
1	VREF	VREF Diagnostic Alert
0	VSS	VSS Diagnostic Alert

Table 5-5. Format for 0x05 Safety Status B()

Bit	Name	Description
7	OTD	Overtemperature in Discharge Safety Fault
6	OTC	Overtemperature in Charge Safety Fault
5	UTD	Undertemperature in Discharge Safety Fault
4	UTC	Undertemperature in Charge Safety Fault
3	OTINT	Internal Overtemperature Safety Fault
2	RSVD0	Reserved
1	VREF	VREF Diagnostic Fault
0	VSS	VSS Diagnostic Fault

The thresholds, delays, and recovery criteria are controlled by individual data memory settings in the ***Protections*** class. For example, the Cell Undervoltage Protection is configured using the ***Protections:Cell Voltage:Cell Undervoltage Protection Threshold***, ***Protections:Cell Voltage:Cell Undervoltage Protection Delay***, and ***Protections:Cell Voltage:Cell Undervoltage Protection Recovery Hysteresis*** data memory settings.

The control of the protection FETs in response to a detected protection event is also configurable, with the device able to operate in a fully autonomous mode, a completely manual mode (controlled through host commands over the serial communications bus), or a combination of the two. Autonomous mode is enabled by setting the ***Settings:Configuration:FET Options[FET_EN]*** data memory configuration bit or sending the *0x0022 FET Enable()* subcommand, which toggles the ***[FET_EN]*** bit. The device can operate in a combined autonomous/manual mode, such that the device can operate autonomously when the host processor does not intervene, but still allows the host to override the autonomous decisions and force FETs on or off based on serial communications. This can be useful in cases where the host needs autonomous reaction to selected faults, such as a short circuit in discharge event, to provide the fastest protection response, but needs manual control for other faults, such as cell overtemperature or overvoltage faults. The *0x29 FET Control()* command provides manual FET control capability by the host. If the user is concerned about unauthorized or inadvertent manual FET control by a host, these selected commands can be disabled using the ***Settings:Configuration:FET Options[HOST_FETOFF_EN]*** and ***[HOST_FETON_EN]*** data memory configuration settings. Each protection can be configured to autonomously disable the pertinent protection FET using the ***Settings:Protection:CHG FET Protections A***, ***Settings:Protection:DSG FET Protections A***, and ***Settings:Protection:Both FET Protections C*** settings.

5.2 Protection Evaluation and Detection

The BQ77307 device includes protections for cell voltage, pack current, and cell temperature, as well as integrated diagnostics. The timing for the evaluation of these protections is different for current versus the other protections. The cell voltages, internal and thermistor temperature, and the VREF and VSS diagnostics are evaluated at periodic intervals set by ***Power:Configuration:Voltage CHECK Time***, which can be set from 250 ms to 255 seconds. The Short Circuit in Discharge (SCD) protection evaluates the differential voltage across the sense resistor (connected to the SRP and SRN pins) continuously, while the sense resistor voltage is evaluated every 305 µs to implement the Overcurrent in Charge (OCC) and Overcurrent in Discharge 1 and 2 (OCD1, OCD2) protections.

The BQ77307 device includes the capability to evaluate the internal die temperature versus selected thresholds using the difference between two internal transistor base-emitter voltages. This voltage difference is periodically compared to various thresholds, such as the Internal Overtemperature (OTINT) Protection based on ***Protections:Temperature:Internal Overtemperature Protection Threshold***, and the internal overtemperature shutdown (based on ***Power:Shutdown:Shutdown Temperature***).

The BQ77307 device also includes an evaluation of the voltage of an external thermistor on the TS pin to implement several temperature protections (OTC, OTD, UTC, UTD) described in later sections. The device uses an internal, factory trimmed 20-kΩ pullup resistor to bias an external thermistor during each evaluation. The TS pin is configured for thermistor evaluation using the ***Settings:Configuration:Eval Config[TSMODE]*** data memory setting. If the pin is not selected for thermistor evaluation, the pullup resistor is not enabled.

To provide a high precision result, the device uses the same 1.8-V internal LDO voltage for the detection threshold as is used for biasing the thermistor pullup resistor, thereby implementing a ratiometric evaluation that removes the error contribution from the LDO voltage level. Because the pullup resistor is only enabled during the periodic pin threshold evaluation, it is recommended to limit the capacitance at this node to less than 4 nF to reduce the effect of incomplete settling when the pullup resistor is biased.

5.3 Protection FET Drivers

The BQ77307 integrates low-side CHG and DSG FET drivers, which can directly drive low-side protection NFET transistors. The state of the drivers is reported by the *0x12 Battery Status()[CHG]* and *[DSG]* bits. The device supports both series and parallel FET configurations, providing FET body diode protection when configured for a

series FET configuration, if one FET driver is on, and the other FET driver is off. In this case, the DSG driver can be turned on to prevent FET damage if the battery pack is charging while the DSG FET is disabled. Similarly, the CHG driver can be turned on if the pack is discharging while the CHG FET is disabled.

The device can be configured for fully autonomous operation, in which case the device autonomously enables the protection FETs if no enabled protection status fault is present which has been configured to control the FETs, and no host command has been issued to force the FET off. Autonomous mode is enabled by setting the ***Settings:Configuration:FET Options[FET_EN]*** or sending the *0x0022 FET Enable()* subcommand, which toggles the ***[FET_EN]*** bit. If ***[FET_EN]*** = 0, the FETs remain disabled until they are manually enabled by command.

Manual FET control is available using the *0x29 FET Control()* command independent of the setting of ***[FET_EN]***. The format of the *0x29 FET Control()* command is shown below. The bits that force the FETs to be enabled are only available if the ***Settings:Configuration:FET Options[HOST_FETON_EN]*** is set, while the bits that force the FETs to be disabled are only available if the ***Settings:Configuration:FET Options[HOST_FETOFF_EN]*** is set.

Table 5-6. Format for *0x29 FET Control()* Command

Bit	Name	Description
7-4	RSVD	Reserved
3	CHG_OFF	CHG FET driver control. This bit only operates if the ***[HOST_FETOFF_EN]*** bit in data memory is set. 0x0 = CHG FET driver is allowed to turn on if other conditions are met. 0x1 = CHG FET driver is forced off.
2	DSG_OFF	DSG FET driver control. This bit only operates if the ***[HOST_FETOFF_EN]*** bit in data memory is set. 0x0 = DSG FET driver is allowed to turn on if other conditions are met. 0x1 = DSG FET driver is forced off.
1	CHG_ON	CHG FET driver control. This bit only operates if the ***[HOST_FETON_EN]*** bit in data memory is set. 0x0 = CHG FET driver is allowed to turn on if other conditions are met. 0x1 = CHG FET driver is forced on.
0	DSG_ON	DSG FET driver control. This bit only operates if the ***[HOST_FETON_EN]*** bit in data memory is set. 0x0 = DSG FET driver is allowed to turn on if other conditions are met. 0x1 = DSG FET driver is forced on.

Note that body diode protection takes priority over the manual FET commands. If the user does not want body diode protection to take effect in this case, it can be disabled by clearing the ***Settings:Configuration:FET Options[SFET]*** data memory configuration bit.

The BQ77307 provides an option for the device to autonomously disable the CHG FET when current is detected below the body diode threshold. The DSG FET can remain enabled in this mode (based on configuration), but the CHG FET can be disabled to reduce the power flowing through the gate-source resistor around the CHG FET when current is low. When a significant charging or discharging current is detected, the body diode protection then causes the CHG FET to be re-enabled unless other conditions prevent it. The state of the CHG FET in this low current mode is set by the ***Settings:Configuration:FET Options[CHGOFF]*** data memory configuration bit.

5.4 Cell Overvoltage Protection

The BQ77307 integrates Cell Overvoltage Protection (COV), periodically monitoring the voltage of every cell, and triggering a COV alert or fault when a cell voltage exceeds the COV threshold. The COV threshold is programmable from 0.0 V to 5.5 V in 1 mV steps and is set by the ***Protections:Cell Voltage:Cell Overvoltage Protection Threshold*** configuration register. The COV protection is enabled using the ***Settings:Protection:Enabled Protections A:[COV]*** configuration bit.

The COV circuitry triggers an alert signal when an overvoltage event is first detected, then triggers a fault after the voltage is detected above the threshold steadily for a programmable number of CHECK intervals. The

number of CHECK intervals required before the fault is triggered is set by the ***Protections:Cell Voltage:Cell Overvoltage Protection Delay*** configuration register, which ranges from 1 to 255. The time until a fault is triggered is based on the settings for the ***Power:Configuration:Voltage CHECK Time*** parameter, which sets the timing for each CHECK voltage evaluation interval.

When a COV fault is triggered, it recovers if the maximum cell voltage drops below the COV threshold by a COV_HYS hysteresis level, which is programmable as 50 mV, 100 mV, or 200 mV, or autonomous recovery can be disabled. The COV_HYS hysteresis level is set by the ***Protections:Cell Voltage:Cell Overvoltage Protection Recovery Hysteresis*** configuration register. If autonomous recovery is disabled, the fault can be recovered manually by the host sending the *0x009B PROT_RECOVERY()* subcommand with the *[VOLTREC]* bit set.

When a COV fault is triggered, the device turns off the CHG FET if configured for autonomous FET control based on setting in ***Settings:Protection:CHG FET Protections A[COV]*** (the DSG FET remains enabled if already enabled). The device recovers (if configured for autonomous FET control) based on all cell voltages being below COV threshold – COV_HYS.

Table 5-7. Overvoltage Protection Operation

Status	Condition	Action
Normal	Max cell voltage ≤ ***Protections:COV:Threshold***	*Safety Alert A()[COV]* = 0
Alert	Max cell voltage > ***Protections:COV:Threshold***	*Safety Alert A()[COV]* = 1
Trip	Max cell voltage > ***Protections:COV:Threshold*** for ***Protections:COV:Delay*** duration	*Safety Alert A()[COV]* = 0 *Safety Status A()[COV]* = 1 and CHG FET can be disabled depending on settings
Recovery	*Safety Status A()[COV]* = 1 and Max cell voltage ≤ ***Protections:COV:Threshold*** - ***Protections:COV:Recovery Hysteresis***	*Safety Status A()[COV]* = 0 and CHG FET can be re-enabled based on settings

5.5 Cell Undervoltage Protection

The BQ77307 integrates Cell Undervoltage Protection (CUV), periodically monitoring the voltage of every cell, and triggering a CUV alert or fault when a cell voltage falls below the CUV threshold. The CUV threshold is programmable from 0.0 V to 5.5 V in 1 mV steps and is set by the ***Protections:Cell Voltage:Cell Undervoltage Protection Threshold*** configuration register. The CUV protection is enabled using the ***Settings:Protection:Enabled Protections A:[CUV]*** configuration bit.

The CUV circuitry triggers an alert signal when an undervoltage event is first detected, then triggers a fault after the voltage is detected below the threshold steadily for a programmable number of CHECK intervals. The number of CHECK intervals required before the fault is triggered is set by the ***Protections:Cell Voltage:Cell Undervoltage Protection Delay*** configuration register, which ranges from 1 to 255. The time until a fault is triggered is based on the settings for the ***Power:Configuration:Voltage CHECK Time*** parameter, which sets the timing for each CHECK voltage evaluation interval..

When a CUV fault is triggered, it recovers if the minimum cell voltage rises above the CUV threshold by a CUV_HYS hysteresis level, which is programmable as 50 mV, 100mV, or 200 mV, or autonomous recovery can be disabled. The CUV_HYS hysteresis level is set by the ***Protections:Cell Voltage:Cell Undervoltage Protection Recovery Hysteresis*** configuration register. If autonomous recovery is disabled, the fault can be recovered manually by the host sending the *0x009B PROT_RECOVERY()* subcommand with the *[VOLTREC]* bit set.

When a CUV fault is triggered, the device turns off the DSG FET if configured for autonomous FET control based on setting in ***Settings:Protection:DSG FET Protections A[CUV]*** (the CHG FET remains enabled if already enabled). The device recovers (if configured for autonomous FET control) based on all cell voltages being above CUV threshold + CUV_HYS.

Table 5-8. Undervoltage Protection Operation

Status	Condition	Action
Normal	Min cell voltage ≥ ***Protections:CUV:Threshold***	*Safety Alert A()[CUV]* = 0
Alert	Min cell voltage < ***Protections:CUV:Threshold***	*Safety Alert A()[CUV]* = 1
Trip	Min cell voltage < ***Protections:CUV:Threshold*** for ***Protections:CUV:Delay*** duration	*Safety Alert A()[CUV]* = 0 *Safety Status A()[CUV]* = 1 and DSG FET can be disabled depending on settings
Recovery	*Safety Status A()[CUV]* = 1 and Min cell voltage ≥ ***Protections:CUV:Threshold*** + ***Protections:CUV:Recovery Hysteresis***	*Safety Status A()[CUV]* = 0 and DSG FET can be re-enabled based on settings

5.6 Short Circuit in Discharge Protection

The BQ77307 integrates Short Circuit in Discharge Protection (SCD) using a dedicated comparator that monitors the differential voltage across the SRN - SRP pins and triggers an SCD alert or fault when the voltage exceeds a programmable threshold VSCD. The VSCD threshold is programmable using the ***Protections:Current:Short Circuit in Discharge Protection Threshold*** configuration register, with available settings shown in Table 5-9. The SCD protection is enabled using the ***Settings:Protection:Enabled Protections A:[SCD]*** configuration bit.

Table 5-9. Short Circuit in Discharge Threshold Settings

Setting	Threshold
0	10 mV
1	20 mV
2	40 mV
3	60 mV
4	80 mV
5	100 mV
6	125 mV
7	150 mV
8	175 mV
9	200 mV
10	250 mV
11	300 mV
12	350 mV
13	400 mV
14	450 mV
15	500 mV

The SCD circuitry triggers an alert signal when a short circuit event is first detected and triggers a fault after a programmable detection delay, SCD_DLY, which is set by the ***Protections:Current:Short Circuit in Discharge Protection Delay*** configuration register. The fastest setting can result in detection of a short circuit with only comparator delay, which can be <1 µs depending on the overdrive of the threshold. The delay settings are shown in Table 5-10.

Table 5-10. Short Circuit in Discharge Delay Setting

Setting	Nominal Delay
0	Fastest
1	0 to 15 µs
2	15 to 30 µs
3	45 to 60 µs

Table 5-10. Short Circuit in Discharge Delay Setting (continued)

Setting	Nominal Delay
4	105 to 120 µs
5	225 to 240 µs
6	465 to 480 µs
7	945 to 960 µs
8	1905 to 1920 µs
9	3825 to 3840 µs
10	7665 to 7680 µs

When an SCD fault is triggered, the device turns off the DSG FET if configured for autonomous FET control in ***Settings:Protection:DSG FET Protections A[SCD]***. The CHG FET can also be disabled autonomously based on setting in ***Settings:Protection:CHG FET Protections A[SCD]***. The device recovers after a programmable delay given by ***Protections:Current:Recovery Time***, which can be set from 1-sec to 255-sec in 1-sec steps. A delay setting of 0 disables autonomous recovery based on time. Continual retrying of time-based recovery can be avoided by using the Current Protection Latch feature.

The SCD safety alert is set in user readable registers up to 50 µs after the event occurs, even though it was detected and the delay timer already started. When the SCD protection delay is set very short, such as the first three settings, the SCD safety status can trigger before the alert becomes visible in the *Alarm Raw Status()* or *Safety Alert A()* registers, and then the alert is cleared by the SCD safety status. When the SCD delay is set to a longer setting, the SCD safety alert is then generally visible.

If autonomous recovery has been disabled, then recovery can occur when the *0x009B PROT_RECOVERY()* command is sent from the host with the *[SCDREC]* bit set.

Table 5-11. Short Circuit in Discharge Protection Operation

Status	Condition	Action
Normal	V_{SRN}–V_{SRP} ≤ setting selected by ***Protections:Current:Short Circuit in Discharge Protection Threshold***	*Safety Alert A()[SCD]* = 0. Clear current latch counter if no current protection fault occurs for 5 seconds.
Alert	V_{SRN}–V_{SRP} > setting selected by ***Protections:Current:Short Circuit in Discharge Protection Threshold***	*Safety Alert A()[SCD]* = 1
Trip	V_{SRN}–V_{SRP} > setting selected by ***Protections:Current:Short Circuit in Discharge Protection Threshold*** for ***Protections:Current:Short Circuit in Discharge Protection Delay*** duration.	*Safety Alert A()[SCD]* = 0 *Safety Status A()[SCD]* = 1 Increment current latch counter.
Recovery	*Safety Status A()[SCD]* = 1 and V_{SRN}–V_{SRP} ≤ setting selected by ***Protections:Current:Short Circuit in Discharge Protection Threshold*** for ***Protections:Current:Recovery Time*** duration.	*Safety Status A()[SCD]* = 0 FETs can be re-enabled if conditions allow and not latched off.
Latch Limit	Current latch counter ≥ ***Protections:Current:Latch Limit***	*Safety Status A()[CURLATCH]* = 1 FETs are latched off and not autonomously re-enabled.

5.7 Overcurrent in Charge Protection

The BQ77307 integrates Overcurrent in Charge Protection (OCC) using a comparator that monitors the differential voltage across the SRP - SRN pins and triggers an OCC alert or fault when the voltage exceeds a programmable threshold VOCC. The VOCC threshold is programmable from 3 mV to 123 mV in 2-mV steps using the ***Protections:Current:Overcurrent in Charge Protection Threshold*** configuration register (threshold = 2 mV × register value - 1 mV). The OCC protection is enabled using the ***Settings:Protection:Enabled Protections A:[OCC]*** configuration bit.

The OCC circuitry triggers an alert signal when an overcurrent in charge event is first detected, then triggers a fault if it persists for a programmable detection delay, OCC_DLY, which can be set as shown below.

Setting	Nominal Delay (ms)
0	Fastest (approximately 0.46 ms)
1 to 64	1.22 ms to 20.435 ms in steps of 0.305 ms
65 to 128	22.875 ms to 176.595 ms in steps of 2.44 ms
129 to 192	181.475 ms to 488.915 ms in steps of 4.88 ms
193 to 255	498.675 ms to 1103.795 ms in steps of 9.77 ms

The delay is set by the ***Protections:Current:Overcurrent in Charge Protection Delay*** configuration register.

When an OCC fault is triggered, the device turns off the CHG FET if configured for autonomous FET control when ***Settings:Protection:CHG FET Protections A[OCC]*** is set. The device recovers after a programmable delay given by ***Protections:Current:Recovery Time*** , which can be set from 1 to 255 seconds in 1-second steps. A recovery time setting of 0 disables autonomous recovery, in which case recovery only occurs when the *PROT_RECOVERY()* subcommand is sent from the host with the *[OCCREC]* bit set. Continual retrying of time-based recovery can be avoided by using the Current Protection Latch feature.

Table 5-12. Overcurrent in Charge Protection Operation

Status	Condition	Action
Normal	V_{SRP}–V_{SRN} ≤ setting selected by ***Protections:Current:Overcurrent in Charge Protection Threshold***	*Safety Alert A()[OCC]* = 0. Clear current latch counter if no current protection fault occurs for 5 seconds.
Alert	V_{SRP}–V_{SRN} > setting selected by ***Protections:Current:Overcurrent in Charge Protection Threshold***	*Safety Alert A()[OCC]* = 1
Trip	V_{SRP}–V_{SRN} > setting selected by ***Protections:Current:Overcurrent in Charge Protection Threshold*** for ***Protections:Current:Overcurrent in Charge Protection Delay*** duration.	*Safety Alert A()[OCC]* = 0 *Safety Status A()[OCC]* = 1 Increment current latch counter.
Recovery	*Safety Status A()[OCC]* = 1 and V_{SRP}–V_{SRN} ≤ setting selected by ***Protections:Current:Overcurrent in Charge Protection Threshold*** for ***Protections:Current:Recovery Time*** duration.	*Safety Status A()[OCC]* = 0 CHG FET can be re-enabled if conditions allow and it is not latched off.
Latch Limit	Current latch counter ≥ ***Protections:Current:Latch Limit***	*Safety Status A()[CURLATCH]* = 1 CHG FET is latched off and not autonomously re-enabled.

5.8 Overcurrent in Discharge 1 and 2 Protections

The BQ77307 integrates two Overcurrent in Discharge Protections (OCD1, OCD2) using a comparator that monitors the differential voltage across the SRN - SRP pins and triggers an OCD1 or OCD2 alert or fault when the voltage exceeds a programmable threshold VOCD1 and VOCD2, respectively. The VOCD1/2 thresholds are programmable from 4 mV to 200 mV in 2 mV steps using the ***Protections:Current:Overcurrent in Discharge 1 Protection Threshold*** and ***Protections:Current:Overcurrent in Discharge 2 Protection Threshold*** configuration registers. These two protections operate identically, but can have independent threshold and delay settings. The OCD1 and OCD2 protections are enabled using the ***Settings:Protection:Enabled Protections A:[OCD1]*** and ***[OCD2]*** configuration bits.

The OCD1/2 circuitry triggers an alert signal when an overcurrent in discharge event is first detected, then triggers a fault if it persists for a programmable detection delay, OCD1_DLY or OCD2_DLY, which can be set as shown below.

Setting	Nominal Delay (ms)
0	Fastest (approximately 0.46 ms)
1 to 64	1.22 ms to 20.435 ms in steps of 0.305 ms

Setting	Nominal Delay (ms)
65 to 128	22.875 ms to 176.595 ms in steps of 2.44 ms
129 to 192	181.475 ms to 488.915 ms in steps of 4.88 ms
193 to 255	498.675 ms to 1103.795 ms in steps of 9.77 ms

The delay is set by the ***Protections:Current:Overcurrent in Discharge 1 Protection Delay*** and ***Protections:Current:Overcurrent in Discharge 2 Protection Delay*** configuration registers.

When an OCD fault is triggered, the device turns off the DSG FET if configured for autonomous FET control in ***Settings:Protection:DSG FET Protections A[OCD1, OCD2]***. The device recovers after a programmable delay given by ***Protections:Current:Recovery Time***, which can be set from 1 second to 255 second in 1-second steps. A recovery time setting of 0 disables autonomous recovery, in which case recovery only occurs when the *PROT_RECOVERY()* command is sent from the host with the appropriate *[OCD1REC]* or *[OCD2REC]* bit set. Continual retrying of time-based recovery can be avoided by using the Current Protection Latch feature.

Table 5-13. Overcurrent in Discharge Protection Operation

Status	Condition	Action
Normal	V_{SRN}–V_{SRP} ≤ setting selected by ***Protections:Current:Overcurrent in Discharge 1 Protection Threshold***	*Safety Alert A()[OCD1]* = 0. Clear current latch counter if no current protection fault occurs for 5 seconds.
Normal	V_{SRN}–V_{SRP} ≤ setting selected by ***Protections:Current:Overcurrent in Discharge 2 Protection Threshold***	*Safety Alert A()[OCD2]* = 0. Clear current latch counter if no current protection fault occurs for 5 seconds.
Alert	V_{SRN}–V_{SRP} > setting selected by ***Protections:Current:Overcurrent in Discharge 1 Protection Threshold***	*Safety Alert A()[OCD1]* = 1
Alert	V_{SRN}–V_{SRP} > setting selected by ***Protections:Current:Overcurrent in Discharge 2 Protection Threshold***	*Safety Alert A()[OCD2]* = 1
Trip	V_{SRP}–V_{SRN} > setting selected by ***Protections:Current:Overcurrent in Discharge 1 Protection Threshold*** for ***Protections:Current:Overcurrent in Discharge 1 Protection Delay*** duration.	*Safety Alert A()[OCD1]* = 0 *Safety Status A()[OCD1]* = 1 Increment current latch counter.
Trip	V_{SRP}–V_{SRN} > setting selected by ***Protections:Current:Overcurrent in Discharge 2 Protection Threshold*** for ***Protections:Current:Overcurrent in Discharge 2 Protection Delay*** duration.	*Safety Alert A()[OCD2]* = 0 *Safety Status A()[OCD2]* = 1 Increment current latch counter.
Recovery	*Safety Status A()[OCD1]* = 1 and V_{SRN}–V_{SRP} ≤ setting selected by ***Protections:Current:Overcurrent in Discharge 1 Protection Threshold*** for ***Protections:Current:Recovery Time*** duration.	*Safety Status A()[OCD1]* = 0 DSG FET can be re-enabled if conditions allow and it is not latched off.
Recovery	*Safety Status A()[OCD2]* = 1 and V_{SRN}–V_{SRP} ≤ setting selected by ***Protections:Current:Overcurrent in Discharge 2 Protection Threshold*** for ***Protections:Current:Recovery Time*** duration.	*Safety Status A()[OCD2]* = 0 DSG FET can be re-enabled if conditions allow and it is not latched off.
Latch Limit	Current latch counter ≥ ***Protections:Current:Latch Limit***	*Safety Status A()[CURLATCH]* = 1 DSG FET is latched off and not autonomously re-enabled.

5.9 Current Protection Latch

The BQ77307 also includes a current protection latch, which prevents the device from continually attempting time-based recovery indefinitely if a short circuit or overcurrent condition persists. Each time an SCD or OCD1 or OCD2 or OCC fault occurs, a latch counter is incremented. If a current protection fault does not occur for 5-sec after re-enabling the pertinent FET, the counter is cleared. If the counter reaches a level of ***Protections:Current:Latch Limit*** (settings of 0, 2, 4, 8, 16, 32, 48, 96, with setting=0 disabling the latch feature), the device disables further autonomous recovery attempts based on time, and the *Safety Status A() [CURLATCH]* bit is set. Recovery can be restarted by the host sending a *PROT_RECOVERY()* command with

any of the current protection bits set, which clears the latch counter value, so the device can again attempt recovery.

5.10 CHG Detector

The BQ77307 provides a signal that indicates if the CHG pin voltage is above a level of approximately 2 V. The raw value of this flag can be read through the communications interface, and an alarm can be generated on the ALERT pin whenever the debounced version of this flag changes state, based on device settings. This flag can be used by the system to assist in recovery from a current fault condition.

The CHG Detector signal is enabled and evaluated by logic within the device if ***Settings:Configuration:FET Options[CHGDETEN]*** = 1. The value of the raw CHG Detector output can be read over the serial communications interface at *Alarm Raw Status()[CDRAW].* If the CHG Detector output is stable for a time interval in excess of ***Settings:Configuration:CHG Detector Time*****,** its value is latched into *Battery Status() [CHGDETFLAG],* which is a debounced version of the CHG Detector signal. The *Alarm Status()[CDTOGGLE]* is set whenever the debounced signal (CHGDETFLAG) changes from its previous debounced state. The value of ***Settings:Configuration:CHG Detector Time*** is programmable from 100 ms to 25.5 s in steps of 100 ms.

The host can use the *Alarm Enable()[CDTOGGLE]* bit to mask the alarm. When *Alarm Status()[CDTOGGLE]* is set, the host can write a 1 to *Alarm Status()[CDTOGGLE]* to clear the alarm.

When a current fault occurs in a system, such as a short circuit event, the device generally disables the DSG FET, the CHG FET, or possibly both, depending on settings. The device can be configured to wait a programmed delay then reenable the FETs. If the current fault condition is still present, then a new fault is triggered, and the FETs disabled again. If a fault persists, this cycle of periodically recovering and retriggering a fault can continue indefinitely, which is generally not acceptable.

An alternative is to only allow a limited number of retries, then to disable further retries after that limit is reached. This capability is supported using the Current Protection Latch. This avoids the indefinite cycle of retries, but can render the pack unusable after a limited number of retries.

If the pack is removable, such as in a power tool, then another option is to keep the FETs disabled until the pack has been removed from the system. In this case, if the CHG driver is disabled and a charger is not connected, then the CHG pin is pulled up to the PACK+ voltage while a load is connected, resulting in the CHG Detector signal being asserted. When the pack is removed from the system (and the charger is still not connected), then the CHG pin generally falls to near the BAT- voltage level, resulting in the CHG Detector signal being deasserted. A host processor within the battery pack can then use this signal to trigger recovery of the pack.

Note that the use of this CHG Detector for load removal depends on the system configuration and is not usable in all cases. Thus, it is important for the pack designer to evaluate whether it is applicable to the system or not.

5.11 Overtemperature in Charge Protection

The BQ77307 device integrates an Overtemperature in Charge (OTC) Protection that compares the voltage of an external negative temperature coefficient (NTC) thermistor on the TS pin to a programmable threshold VOTC, and triggers an alert or fault when the voltage is less than the threshold. The thermistor is biased using an on-chip 20-kΩ pullup resistor (which is trimmed in TI factory), which is biased by the internal 1.8 V LDO (V_{REG18}) rail only when the thermistor voltage is being evaluated (which is the default recommended setting). Alternatively, the pullup resistor can be biased continuously by sending the *0x69 REGOUT_CONTROL()* command with the *[TS_ON]* bit set. The detection circuitry uses this same internal 1.8 V LDO rail to generate the detection threshold, thereby implementing a ratiometric comparison.

The VOTC threshold is programmable in units of V_{REG18} / 359, with settings from 0 to 255 using the ***Protections:Temperature:Overtemperature in Charge Protection Threshold*** configuration register. The OTC protection is enabled using the ***Settings:Protection:Enabled Protections B:[OTC]*** configuration bit.

The OTC protection triggers an alert signal when an overtemperature in charge event is first detected, then triggers a fault if this persists after a programmable number of CHECK intervals, OTC_DLY, which can be set

from 0 to 255. The delay is set by the ***Protections:Temperature:Overtemperature in Charge Protection Delay*** configuration register.

When an OTC fault is triggered, the device turns off the CHG FET if configured for autonomous FET control, based on the setting in ***Settings:Protection:CHG FET Protections A[OTC]***. The device recovers when the thermistor voltage is detected greater than or equal to the threshold set by ***Protections:Temperature:Overtemperature in Charge Protection Recovery*** (which has the same threshold range from 0 to 255 in steps of V_{REG18} / 359). If the ***Protections:Temperature:Overtemperature in Charge Protection Recovery*** is set to zero, autonomous recovery is disabled, and recovery must be initiated by the host sending the *PROT_RECOVERY()* subcommand with the *[TEMPREC]* bit set.

Table 5-14. Overtemperature in Charge Protection Operation

Status	Condition	Action
Normal	TS pin voltage ≥ ***Protections:Temperature:Overtemperature in Charge Protection Threshold***	*Safety Alert B()[OTC]* = 0
Alert	TS pin voltage < ***Protections:Temperature:Overtemperature in Charge Protection Threshold***	*Safety Alert B()[OTC]* = 1
Trip	TS pin voltage < ***Protections:Temperature:Overtemperature in Charge Protection Threshold*** for ***Protections:Temperature:Overtemperature in Charge Protection Delay*** duration	*Safety Alert B()[OTC]* = 0 *Safety Status B()[OTC]* = 1 and CHG FET can be disabled depending on settings
Recovery	*Safety Status B()[OTC]* = 1 and TS pin voltage ≥ ***Protections:Temperature:Overtemperature in Charge Protection Recovery***	*Safety Status B()[OTC]* = 0 and CHG FET can be re-enabled based on settings

5.12 Overtemperature in Discharge Protection

The BQ77307 device integrates an Overtemperature in Discharge (OTD) Protection that compares the voltage of an external negative temperature coefficient (NTC) thermistor on the TS pin to a programmable threshold VOTD, and triggers an alert or fault if the voltage is less than the threshold. The thermistor is biased using an on-chip 20-kΩ pullup resistor (which is trimmed in TI factory), which is biased by the internal 1.8 V LDO (V_{REG18}) rail only when the thermistor is being evaluated (which is the default recommended setting). Alternatively, the pullup resistor can be biased continuously by sending the *0x69 REGOUT_CONTROL()* command with the *[TS_ON]* bit set. The detection circuitry uses this same internal 1.8 V LDO rail to generate the detection threshold, thereby implementing a ratiometric comparison.

The VOTD threshold is programmable in units of V_{REG18} / 359, with settings from 0 to 255 using the ***Protections:Temperature:Overtemperature in Discharge Protection Threshold*** configuration register. The OTD protection is enabled using the ***Settings:Protection:Enabled Protections B:[OTD]*** configuration bit.

The OTD protection triggers an alert signal when an overtemperature in charge event is first detected, then triggers a fault if this persists after a programmable number of CHECK intervals, OTD_DLY, which can be set from 0 to 255. The delay is set by the ***Protections:Temperature:Overtemperature in Discharge Protection Delay*** configuration register.

When an OTD fault is triggered, the device turns off the DSG FET if configured for autonomous FET control, based on the setting in ***Settings:Protection:DSG FET Protections A[OTD]***. The device recovers when the thermistor voltage is detected greater than or equal to the threshold set by ***Protections:Temperature:Overtemperature in Discharge Protection Recovery*** (which has the same threshold range from 0 to 255 in steps of V_{REG18} / 359). If the ***Protections:Temperature:Overtemperature in Discharge Protection Recovery*** is set to zero, autonomous recovery is disabled, and recovery must be initiated by the host sending the *PROT_RECOVERY()* subcommand with the *[TEMPREC]* bit set.

Table 5-15. Overtemperature in Discharge Protection Operation

Status	Condition	Action
Normal	TS pin voltage ≥ ***Protections:Temperature:Overtemperature in Discharge Protection Threshold***	*Safety Alert B()[OTD]* = 0

Table 5-15. Overtemperature in Discharge Protection Operation (continued)

Status	Condition	Action
Alert	TS pin voltage < ***Protections:Temperature:Overtemperature in Discharge Protection Threshold***	*Safety Alert B()[OTD]* = 1
Trip	TS pin voltage < ***Protections:Temperature:Overtemperature in Discharge Protection Threshold*** for ***Protections:Temperature:Overtemperature in Discharge Protection Delay*** duration	*Safety Alert B()[OTD]* = 0 *Safety Status B()[OTD]* = 1 and DSG FET can be disabled depending on settings
Recovery	*Safety Status B()[OTD]* = 1 and TS pin voltage ≥ ***Protections:Temperature:Overtemperature in Discharge Protection Recovery***	*Safety Status B()[OTD]* = 0 and DSG FET can be re-enabled based on settings

5.13 Internal Overtemperature Protection

The BQ77307 device integrates an Internal Overtemperature Protection (OTINT) that compares the internal die temperature to a programmable threshold VOTINT, and triggers an alert or fault when the internal temperature is greater than the threshold.

The VOTINT threshold is programmable from 25°C to 150°C in 1°C steps using the ***Protections:Temperature:Internal Overtemperature Protection Threshold*** configuration register. The OTINT protection is enabled using the ***Settings:Protection:Enabled Protections B:[OTINT]*** configuration bit.

The OTINT protection triggers an alert signal when an internal overtemperature event is first detected, then triggers a fault after a programmable number of CHECK intervals, OTINT_DLY, which can be set from 0 to 255. The delay is set by the ***Protections:Temperature:Internal Overtemperature Protection Delay*** configuration register.

When an OTINT fault is triggered, the device turns off the DSG and CHG FETs if configured for autonomous FET control, based on the setting in ***Settings:Protection:DSG FET Protections A[OTINT]*** and ***Settings:Protection:CHG FET Protections A[OTINT]***. The device recovers when the temperature is equal or below ***Protections:Temperature:Internal Overtemperature Protection Recovery***. If the ***Protections:Temperature:Internal Overtemperature Protection Recovery*** is set to zero, autonomous recovery is disabled, and recovery must be initiated by the host sending the *PROT_RECOVERY()* subcommand with the *[TEMPREC]* bit set.

Table 5-16. Internal Overtemperature Protection Operation

Status	Condition	Action
Normal	Internal die temperature ≤ ***Protections:Temperature:Internal Overtemperature Protection Threshold***	*Safety Alert B()[OTINT]* = 0
Alert	Internal die temperature > ***Protections:Temperature:Internal Overtemperature Protection Threshold***	*Safety Alert B()[OTINT]* = 1
Trip	Internal die temperature > ***Protections:Temperature:Internal Overtemperature Protection Threshold*** for ***Protections:Temperature:Internal Overtemperature Protection Delay*** duration	*Safety Alert B()[OTINT]* = 0 *Safety Status B()[OTINT]* = 1 and CHG and DSG FETs can be disabled depending on settings
Recovery	*Safety Status B()[OTINT]* = 1 and Internal die temperature ≤ ***Protections:Temperature:Internal Overtemperature Protection Threshold***	*Safety Status B()[OTINT]* = 0 and CHG and DSG FETs can be re-enabled based on settings

5.14 Undertemperature in Charge Protection

The BQ77307 device integrates an Undertemperature in Charge (UTC) Protection that compares the voltage of an external negative temperature coefficient (NTC) thermistor on the TS pin to a programmable threshold VUTC, and triggers an alert or fault when the voltage at the thermistor is greater than the threshold. The thermistor is biased using an on-chip 20-kΩ pullup resistor (which is trimmed in TI factory), which is biased by the internal 1.8-V LDO (V_{REG18}) rail only when the thermistor is being evaluated (which is the default recommended setting). Alternatively, the pullup resistor can be biased continuously by sending the *0x69 REGOUT_CONTROL()*

command with the *[TS_ON]* bit set. The detection circuitry uses this same internal 1.8-V LDO rail to generate the detection threshold, thereby implementing a ratiometric comparison.

The VUTC threshold is programmable in units of V_{REG18} / 252, with settings from 0 to 255 using the ***Protections:Temperature:Undertemperature in Charge Protection Threshold*** configuration register. The UTC protection is enabled using the ***Settings:Protection:Enabled Protections B:[UTC]*** configuration bit.

The UTC protection triggers an alert signal when an undertemperature in charge event is first detected, then triggers a fault after a programmable number of CHECK intervals, UTC_DLY, which can be set from 0 to 255. The delay is set by the ***Protections:Temperature:Undertemperature in Charge Protection Delay*** configuration register.

When a UTC fault is triggered, the device turns off the CHG FET if configured for autonomous FET control, based on the setting in ***Settings:Protection:CHG FET Protections A[UTC]***. The device recovers when the thermistor voltage is detected less than or equal to the threshold set by ***Protections:Temperature:Undertemperature in Charge Protection Recovery*** (which has the same threshold range from 0 to 255 in steps of V_{REG18} / 252). If the ***Protections:Temperature:Undertemperature in Charge Protection Recovery*** is set to zero, autonomous recovery is disabled, and recovery must be initiated by the host sending the *PROT_RECOVERY()* subcommand with the *[TEMPREC]* bit set.

Table 5-17. Undertemperature in Charge Protection Operation

Status	Condition	Action
Normal	TS pin voltage ≤ ***Protections:Temperature:Undertemperature in Charge Protection Threshold***	*Safety Alert B()[UTC]* = 0
Alert	TS pin voltage > ***Protections:Temperature:Undertemperature in Charge Protection Threshold***	*Safety Alert B()[UTC]* = 1
Trip	TS pin voltage > ***Protections:Temperature:Undertemperature in Charge Protection Threshold*** for ***Protections:Temperature:Undertemperature in Charge Protection Delay*** duration	*Safety Alert B()[UTC]* = 0 *Safety Status B()[UTC]* = 1 and CHG FET can be disabled depending on settings
Recovery	*Safety Status B()[UTC]* = 1 and TS pin voltage ≤ ***Protections:Temperature:Undertemperature in Charge Protection Recovery***	*Safety Status B()[UTC]* = 0 and CHG FET can be re-enabled based on settings

5.15 Undertemperature in Discharge Protection

The BQ77307 device integrates an Undertemperature in Discharge (UTD) Protection that compares the voltage of an external negative temperature coefficient (NTC) thermistor on the TS pin to a programmable threshold VUTD, and triggers an alert or fault when the voltage is greater than the threshold. The thermistor is biased using an on-chip 20-kΩ pullup resistor (which is trimmed in TI factory), which is biased by the internal 1.8 V LDO (V_{REG18}) rail only when the thermistor is being evaluated (which is the default recommended setting). Alternatively, the pullup resistor can be biased continuously by sending the *0x69 REGOUT_CONTROL()* command with the *[TS_ON]* bit set. The detection circuitry uses this same internal 1.8 V LDO rail to generate the detection threshold, thereby implementing a ratiometric comparison.

The VUTD threshold is programmable in units of V_{REG18} / 252, with settings from 0 to 255 using the ***Protections:Temperature:Undertemperature in Discharge Protection Threshold*** configuration register. The UTD protection is enabled using the ***Settings:Protection:Enabled Protections B:[UTD]*** configuration bit.

The UTD protection triggers an alert signal when an undertemperature in discharge event is first detected, then triggers a fault after a programmable number of CHECK intervals, UTD_DLY, which can be set from 0 to 255. The delay is set by the ***Protections:Temperature:Undertemperature in Discharge Protection Delay*** configuration register.

When a UTD fault is triggered, the device turns off the DSG FET if configured for autonomous FET control, based on the setting in ***Settings:Protection:DSG FET Protections A[UTD]***. The device recovers when the thermistor voltage is detected less than or equal to the threshold set by ***Protections:Temperature:Undertemperature in Discharge Protection Recovery*** (which has the same

threshold range from 0 to 255 in steps of V_{REG18} / 252). If the ***Protections:Temperature:Undertemperature in Discharge Protection Recovery*** is set to zero, autonomous recovery is disabled, and recovery must be initiated by the host sending the *PROT_RECOVERY()* subcommand with the *[TEMPREC]* bit set.

Table 5-18. Undertemperature in Discharge Protection Operation

Status	Condition	Action
Normal	TS pin voltage ≤ ***Protections:Temperature:Undertemperature in Discharge Protection Threshold***	*Safety Alert B()[UTD]* = 0
Alert	TS pin voltage > ***Protections:Temperature:Undertemperature in Discharge Protection Threshold***	*Safety Alert B()[UTD]* = 1
Trip	TS pin voltage > ***Protections:Temperature:Undertemperature in Discharge Protection Threshold*** for ***Protections:Temperature:Undertemperature in Discharge Protection Delay*** duration	*Safety Alert B()[UTD]* = 0 *Safety Status B()[UTD]* = 1 and DSG FET can be disabled depending on settings
Recovery	*Safety Status B()[UTD]* = 1 and TS pin voltage ≤ ***Protections:Temperature:Undertemperature in Discharge Protection Recovery***	*Safety Status B()[UTD]* = 0 and DSG FET can be re-enabled based on settings

5.16 Cell Open Wire Detection

The BQ77307 device supports detecting a disconnection between a cell in the pack and the cell attachment to the PCB containing BQ77307. Without this check, the voltage at the cell input pin of the BQ77307 device can persist for some time on the board-level capacitor, leading to incorrect protection decisions. The Cell Open Wire detection in the BQ77307 device operates by enabling a small current source from each cell to VSS at programmable intervals. If a cell input pin is floating due to an open wire condition, this current discharges the capacitance, causing the voltage at the pin to slowly drop. This drop in voltage can eventually trigger a Cell Undervoltage protection fault on that particular cell, as well as a Cell Overvoltage protection fault on the cell above it. It is important that the cell undervoltage and overvoltage protections be enabled with appropriate threshold settings for the open wire condition to be detected and the desired reaction initiated.

The cell open wire protection can be enabled or disabled using the ***Settings:Protection:Cell Open Wire Check Time[COWEN]*** configuration bit. If this feature is enabled, the cell open wire current is enabled on each cell, one cell at a time, for approximately 2.93 ms at a rate set by the ***Settings:Protection:Cell Open Wire Check Time[COWTIME2:0]*** configuration register. This provides programmability in the average current drawn from ≈79 pA to ≈5 µA, based on the typical current source value of 55 µA.

Table 5-19. Cell Open-Wire Check Time Settings

Bit Setting COWTIME[2:0]	Description
0x0	Current sources are activated once every 8 CHECK intervals
0x1	Current sources are activated once every 4 CHECK intervals
0x2	Current sources are activated once every 2 CHECK intervals
0x3	Current sources are activated once every CHECK interval
0x4	Current sources are activated twice every CHECK interval
0x5	Current sources are activated four times every CHECK interval
0x6	Current sources are activated 8 times every CHECK interval
0x7	Current sources are activated 16 times every CHECK interval

Note

The cell open wire check can create a cell imbalance, so select the settings appropriately.

5.17 Voltage Reference Diagnostic Protection

The BQ77307 device integrates a diagnostic check on the voltage references used by the device. A regular check is made of the ratio between the two reference voltages every CHECK interval. Thus, if one of the two references malfunctions and deviates significantly from its expected value, the resulting ratio result changes and allows detection of this condition. When detected, the device triggers a Voltage Reference Diagnostic Fault and sets *0x03 Safety Status B()[VREF]*, if enabled, and the device can disable FETs based on settings in ***Settings:Protection:Both FET Protections B[VREF]***. The fault can be recovered by the host sending the *0x009B PROT_RECOVERY()[DIAGREC]* subcommand. The diagnostic protection alert is triggered whenever the deviates from the expected value by approximately 25%. The diagnostic protection status fault is triggered when this occurs for two consecutive CHECK intervals.

5.18 VSS Diagnostic Protection

The BQ77307 device includes an evaluation of the VSS voltage during each CHECK interval, comparing the resulting value to a threshold, to implement the VSS Diagnostic Protection. If the internal detection mux were to malfunction and remain fixed on one particular input, whether that being a cell voltage input, a thermistor, or a diagnostic check, this check of VSS helps make sure this condition is detected. When detected, the device triggers the VSS Diagnostic Protection Fault and sets *0x03 Safety Status B()[VSS]*, if enabled, and the device can disable FETs based on ***Settings:Protection:Both FET Protections B[VSS]***. The fault can be recovered by the host sending the *0x009B PROT_RECOVERY()[DIAGREC]* subcommand. The diagnostic protection alert is triggered whenever the VSS voltage is detected above approximately 100 mV. The diagnostic protection status fault is triggered when this occurs for two consecutive CHECK intervals.

5.19 REGOUT Diagnostic Protection

The REGOUT LDO integrated in the BQ77307 device includes circuitry to detect an error condition, such as the regulator is in short circuit current limit, or if the die temperature exceeds approximately 120°C. When an error condition is detected, the device disables the REGOUT LDO, triggers the REGOUT Diagnostic Protection Fault, and sets *0x05 Safety Status A()[REGOUT]*, if enabled. The device can disable FETs based on the setting of ***Settings:Protection:Both FET Protections B[REGOUT]***. When an overtemperature condition is detected, the device can transition to SHUTDOWN mode if ***Settings:Configuration:Power Config[OTSD]*** is set. The fault is recovered if the cause of the error is removed (such as the short circuit is removed or the regulator temperature falls below the overtemperature threshold).

5.20 LFO Oscillator Integrity Diagnostic Protection

The BQ77307 device integrates a special hardware block that monitors if the LFO stops oscillating or deviates significantly in frequency versus its expected value. If this is detected, the device immediately transitions into SHUTDOWN mode if ***Settings:Configuration:Power Config[LFOWD]*** is set.

5.21 Internal Factory Trim Diagnostic Protection

The BQ77307 device performs a check of the digital trim information within the device at initial power up or after any full reset. If an error is detected during this check, the device immediately transitions to SHUTDOWN mode.

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6.1 *0x00 Control Status()* and *0x12 Battery Status()* Commands

The BQ77307 device includes a *0x00 Control Status()* command, which is primarily intended for legacy bqStudio auto-detection and is not recommended for customer usage. The *0x00 Control Status()* command behaves similarly to 0x3E and 0x3F when written, accepting subcommand addresses. When this command is read back immediately after it has been written, it returns 0xFFA5 once.

The device also includes the *0x12 Battery Status()* command, which reports various status information on the pack, as shown below.

Table 6-1. *0x12 Battery Status()* Bit Definitions

Bit	Name	Description
15	RSVD0	Reserved
14	RSVD0	Reserved
13	SA	This flag asserts if an enabled safety alert is present. 0x0 = Indicates an enabled safety alert is not present 0x1 = Indicates an enabled safety alert is present
12	SS	This flag asserts if an enabled safety fault is present. 0x0 = Indicates an enabled safety fault is not present 0x1 = Indicates an enabled safety fault is present
11-10	SEC1:SEC0	SEC1:0 indicate the present security state of the device. When in SEALED mode, device configuration cannot be read or written and some commands are restricted. When in FULLACCESS mode, unrestricted read and write access is allowed and all commands are accepted. 0x0 = 0: Device has not initialized yet. 0x1 = 1: Device is in FULLACCESS mode. 0x2 = 2: Unused. 0x3 = 3: Device is in SEALED mode.
9	RSVD0	Reserved
8	FET_EN	This bit is set when the device is in autonomous FET control mode. The default value of this bit is set by the Settings:FET Options[FET_EN] bit in Data Memory upon exit of CONFIG_UPDATE mode. Its value can be modified during operation using the FET_ENABLE() subcommand. 0x0 = Device is not in autonomous FET control mode, FETs are only enabled through manual command. 0x1 = Device is in autonomous FET control mode, FETs can be enabled by the device if no conditions or commands prevent them being enabled.
7	POR	This bit is set when the device fully resets. It is cleared upon exit of CONFIG_UPDATE mode. It can be used by the host to determine if any register configuration changes were lost due to a reset. 0x0 = Full reset has not occurred since last exit of CONFIG_UPDATE mode. 0x1 = Full reset has occurred since last exit of CONFIG_UPDATE and reconfiguration of any register settings is required.
6	RSVD0	Reserved
5	CFGUPDATE	This bit indicates whether or not the device is in CONFIG_UPDATE mode. It is set after the SET_CFGUPDATE() subcommand is received and fully processed. Configuration settings can be changed only while this bit is set. 0x0 = Device is not in CONFIG_UPDATE mode. 0x1 = Device is in CONFIG_UPDATE mode.
4	ALERTPIN	This bit indicates whether the ALERT pin is asserted (pulled low). 0x0 = ALERT pin is not asserted (stays in hi-Z mode). 0x1 = ALERT pin is asserted (pulled low).

Table 6-1. *0x12 Battery Status()* Bit Definitions (continued)

Bit	Name	Description
3	CHG	This bit indicates whether the CHG driver is enabled. 0x0 = CHG driver is disabled. 0x1 = CHG driver is enabled.
2	DSG	This bit indicates whether the DSG driver is enabled. 0x0 = DSG driver is disabled. 0x1 = DSG driver is enabled.
1	CHGDETFLAG	This bit indicates the value of the debounced CHG Detector signal. 0x0 = CHG Detector debounced signal is low. 0x1 = CHG Detector debounced signal is high.
0	RSVD0	Reserved

6.2 Unused VC Cell Input Pins

If the BQ77307 device is used in a system with fewer than 7 series cells, specific cells must be used for connection to real cells, as shown in Table 6-2. Short out the unused cell inputs on the circuit board. The device only evaluates protections associated with those cells designated as real cells.

Table 6-2. Cell Usage

Number of Cell Used (*Vcell Mode* setting)	Cell Connections	Shorted Cells
0, 1, or 7	VC7–VC6, VC6–VC5, VC5–VC4, VC4–VC3, VC3–VC2, VC2–VC1, VC1–VC0	none
6	VC7–VC6, VC6–VC5, VC5–VC4, VC3–VC2, VC2–VC1, VC1–VC0	VC4–VC3
5	VC7–VC6, VC5–VC4, VC3–VC2, VC2–VC1, VC1–VC0	VC6–VC5, VC4–VC3
4	VC7–VC6, VC5–VC4, VC3–VC2, VC1–VC0	VC6–VC5, VC4–VC3, VC2–VC1
3	VC7–VC6, VC5–VC4, VC1–VC0	VC6–VC5, VC4–VC3, VC3–VC2, VC2–VC1
2	VC7–VC6, VC1–VC0	VC6–VC5, VC5–VC4, VC4–VC3, VC3–VC2, VC2–VC1

Note

It is important that the differential input for each cell input not fall below –0.3 V (the Absolute Maximum data sheet limit), with the recommended minimum voltage of –0.2 V. Therefore, it is important that the I·R voltage drop across the interconnect resistance does not cause a violation of this requirement.

Short the unused cell input pins to adjacent cell input pins, as shown in Figure 6-1.

It is also important to note that the range of voltages supported by the different VC pins differs depending on the pin. For example, pins VC7, VC6, and VC5 can only support cell protections if their pin voltage is greater than or equal to 2 V. Thus if implementing a 2s system using the top and bottom cell input pins, the upper cell voltage protections are not evaluated correctly if the bottom cell voltage drops below 2 V, because VC6 is below 2 V.

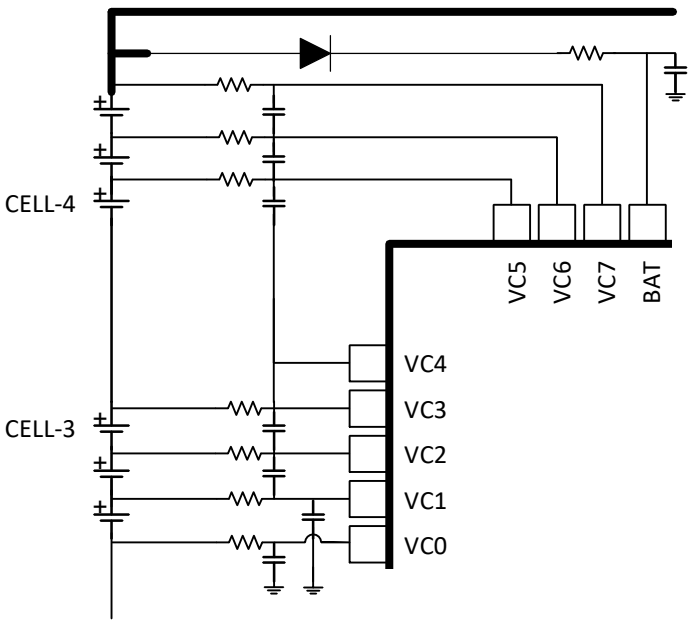

Figure 6-1. Connecting an Unused Cell Input Pin

The ***Settings:Configuration:Vcell Mode*** data memory setting is used to specify which cell inputs are used for actual cells. The device uses this information to disable cell voltage protections associated with inputs which are not used.

6.3 LDOs

The BQ77307 contains an integrated 1.8 V LDO (REG18) that provides a regulated 1.8 V supply voltage for the device's internal circuitry and digital logic. The supply current for this LDO is drawn from the BAT pin.

The device also integrates a programmable LDO (REGOUT) for external circuitry, such as a host processor or external transceiver circuitry. The REGOUT LDO takes its input from the REGSRC pin, which is generally expected to be connected to the top-of-stack, or can be generated by a separate DC/DC converter in the system. The REGOUT LDO output voltage can be programmed to 1.8 V, 2.5 V, 3.0 V, 3.3 V, or 5.0 V, and it can provide an output current of up to 20 mA if thermal conditions permit.

The REGOUT LDO voltage level is selected using the ***Settings:Configuration:REGOUT Config[REGCTL_2:0]*** configuration bits as shown below. The LDO is enabled using the ***Settings:Configuration:REGOUT Config[REG_EN]*** configuration bit, and its setting can be modified during operation using the *0x69 REGOUT Control()* command.

The REGOUT LDO can be programmed to either remain disabled or power up automatically whenever the device exits SHUTDOWN mode, depending on OTP configuration. When the REGOUT LDO is disabled, its output is pulled to VSS with an internal resistance of approximately 2.5-kΩ while the device is in NORMAL mode. If the LDO is configured based on OTP settings to be powered, then at each later power-up the device autonomously loads the OTP settings and enable the LDO as configured, without requiring communications first.

The BQ77307 is designed to operate properly with a die temperature up to 110°C. Therefore the system design must avoid drawing excessive current from the REGOUT LDO if it could result in the die temperature exceeding this level. For example, with an ambient temperature of 60°C, a stack voltage of 31.5 V, and LDO programmed to an output voltage of 2.5 V, the device dissipates approximately 580 mW when supplying 20 mA of load current. The package thermal impedance can be used to calculate the resulting die temperature. If this exceeds the device's specified temperature range, the load current must be limited in the system. The BQ77307 REGOUT LDO includes an overtemperature detector, which detects if the die temperature exceeds a level of

approximately 120°C and automatically causes the LDO to shutdown, and if the ***Settings:Configuration:Power Config[OTSD]*** bit is set, the entire device also enters SHUTDOWN mode.

Table 6-3. REGOUT LDO Voltage Settings from *Settings:Configuration:REGOUT Config* and *0x69 REGOUT Control()*

REGCTL[2:0] or REGOUTV[2:0]	REGOUT Voltage (V)
0x0 - 0x3	1.8
0x4	2.5
0x5	3.0
0x6 (default)	3.3
0x7	5.0

6.4 ALERT Pin Operation

The BQ77307 includes functionality to generate an alarm signal at the ALERT pin, which can be used as an interrupt to a host processor. The ALERT pin is an open-drain pin that is pulled low by the device whenever an alarm signal is generated. The alarm signal is an OR of all bits in the *0x62 Alarm Status()* result. The alarm function includes a programmable mask (set using *0x66 Alarm Enable()*), to allow the customer to decide which flags or events can trigger an alarm. The instantaneous, unlatched bits available to trigger an alarm can be read from the *0x64 Alarm Raw Status()* command, these bits are described in the table below.

Table 6-4. Alarm Options

Name	Description
SSA	This bit is set when a bit in *0x03 Safety Status A()* is set
SSB	This bit is set when a bit in *0x05 Safety Status B()* is set
SAA	This bit is set when a bit in *0x02 Safety Alert A()* is set
SAB	This bit is set when a bit in *0x04 Safety Alert B()* is set
XCHG	This bit is set when the CHG FET is off.
XDSG	This bit is set when the DSG FET is off.
SHUTV	Stack voltage is below ***Power:Shutdown:Shutdown Stack Voltage*** or a cell voltage is below ***Power:Shutdown:Shutdown Cell Voltage***.
INITCOMP	This bit in *0x64 Alarm Raw Status()* pulses momentarily when the device completes the startup evaluation sequence (which occurs at initial power up, reset, and exit of CONFIG_UPDATE mode).
CDRAW / CDTOGGLE	This bit in *0x64 Alarm Raw Status()* is CDRAW, the value of the CHG Detector output. The corresponding bit in *0x62 Alarm Status()* is CDTOGGLE, which is set whenever the debounced version of CDRAW changes state from the previous latched state.
POR	This bit reflects the POR bit in *0x12 Battery Status()*. It is set when the device is first powered up, and is cleared when CONFIG_UPDATE mode is exited. If the host initializes settings at each device power up, monitoring this bit can alert the host that a reset has occurred and the device needs to be reinitialized.

The *0x64 Alarm Raw Status()* command provides the unlatched instantaneous value of each signal listed above. For each signal that is specified by the masking to be included in the alarm, when the bit in *0x64 Alarm Raw Status()* is asserted, the bit is latched into the *0x62 Alarm Status()* register, and the ALERT pin is asserted (pulled low) if any bit in *0x62 Alarm Status()* is asserted. When the host receives the interrupt from the ALERT pin pulled low, the host can read the *0x62 Alarm Status()* register to determine which flag has caused the alarm. The host can then write to the *0x62 Alarm Status()* command with the corresponding bits set, and the corresponding flags are unlatched.

The default alarm mask is set by the ***Settings:Configuration:Default Alarm Mask*** data memory value. This mask can be changed during operation using the *0x66 Alarm Enable()* command, to mask or unmask individual bits from generating an alarm signal.

The *[INITCOMP]* bit in *Alarm Raw Status()* only pulses momentarily when an event occurs, so is not intended to be monitored by reading *0x64 Alarm Raw Status()*. If this bit is included by mask setting in the *0x62 Alarm Status()*, then the corresponding bit in *0x62 Alarm Status()* latches and remains asserted until cleared by the host.

6.5 TS Pin Operation

The TS pin on the BQ77307 device can be used to implement cell temperature protections with a thermistor connected from the TS pin to VSS, if the ***Settings:Configuration:TS Mode[TSMODE]*** bit is set. In this mode, the pin is internally connected to a 20-kΩ trimmed pullup resistor, which is biased by the internal 1.8V LDO (REG18) voltage. The voltage at the TS pin is compared to a programmed threshold which is also based on the same 1.8 V LDO voltage used for the pullup resistor, thereby implementing a ratiometric evaluation.

When the TS pin is configured for thermistor temperature protection, the device enables the internal pullup resistor only while the pin voltage is being evaluated during each CHECK interval (which is the default recommended setting). Alternatively, the pullup resistor can be biased continuously by sending the *0x69 REGOUT_CONTROL()* command with the *[TS_ON]* bit set.

6.6 Device Event Timing

The timing of events in the BQ77307 device varies based on the specific event. Several events and their associated timing are described below. Timings described below do not include the delays related to individual protections, as described in their respective sections.

Table 6-5. Timing of Events

Event Description	Timing
TS or VC0 pin raised to wake device from SHUTDOWN mode	0 ms
REGOUT LDO enabled	2.6 ms
I^2C communications active after initial power-up	3.2 ms
0x64 Alarm Raw Status()[INITCOMP] is asserted (7s)	9.4 ms
Protections evaluated and FETs enabled (7s)	9.4 ms

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7.1 Overview of Operational Modes

This device supports two operational modes, one for normal operation, and one used for host configuration.

- NORMAL mode: In this mode, the device evaluates system current, cell voltages, internal and thermistor temperature, and various diagnostic checks, operates protections as configured, and provides interrupt and status updates. Battery protections are enabled, and the FET drivers are typically enabled (in the absence of any protection fault).
- SHUTDOWN mode: The device is completely disabled (including the internal 1.8 V and REGOUT LDOs), the CHG and DSG FETs are both disabled, all battery protections are disabled, and no protections are evaluated. This is the lowest power state of the device, which can be used for shipment or long-term storage. All register settings (other than settings programmed into OTP by TI) are lost when in SHUTDOWN mode.

The device also includes a CONFIG_UPDATE mode, which is used for parameter updates. Transitioning between operational modes is shown in BQ77307 Operational Power Modes.

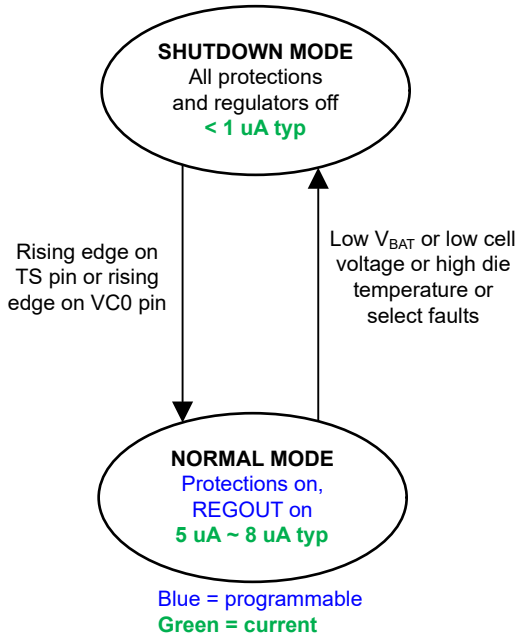

Figure 7-1. BQ77307 Operational Power Modes

7.2 NORMAL Mode

When in NORMAL mode, the BQ77307 regularly evaluates cell voltage, pack current, and thermistor and internal die temperature, implementing all enabled battery protections, and controlling FET drivers based on programmed settings.

The device remains in this mode unless it autonomously enters SHUTDOWN mode if the stack voltage or the minimum cell voltage drops below programmable thresholds, or the TS pin thermistor temperature is detected above a programmable threshold, or an excessive die temperature is detected.

7.3 SHUTDOWN Mode

SHUTDOWN mode is the lowest power mode of the BQ77307, which can be used for shipping or long term storage. In this mode, the device loses all register state information (except for what has been programmed into OTP by TI), the internal logic is powered down, the protection FETs are all disabled, so no voltage is provided at the battery pack terminals. All protections are disabled, all voltage, current, and temperature measurements are disabled, and no communications are supported. When the device exits SHUTDOWN mode, it reads any parameters stored in OTP. If the OTP has not been programmed (this is only supported by TI), the device powers up with default settings, and then settings can be changed by the host writing device registers.

The device can be configured to enter SHUTDOWN mode automatically based on the minimum top of stack voltage, the minimum cell voltage, or an excessive die temperature. If the top-of-stack voltage falls below ***Power:Shutdown:Shutdown Stack Voltage*** or if the minimum cell voltage falls below ***Power:Shutdown:Shutdown Cell Voltage***, or if the internal die temperature exceeds ***Power:Shutdown:Shutdown Temperature***, the SHUTDOWN mode sequence is automatically initiated. The shutdown based on cell voltage only applies to cell input pins being used for actual cells, based on settings in ***Settings:Configuration:Vcell Mode***.

The BQ77307 integrates a hardware overtemperature detection circuit, which determines when the die temperature passes an excessive temperature of approximately 120°C. If this detector triggers, the device automatically begins the sequence to enter SHUTDOWN, based on the configuration setting.

When the device is wakened from SHUTDOWN, it requires approximately 10 ms for the internal circuitry to power up, load settings from OTP memory, perform initial evaluation of conditions relative to enabled protections, then to enable FETs if conditions and settings allow.

The BQ77307 wakes from SHUTDOWN if a voltage is applied at the TS or VC0 pins above a level of approximately 1.2 V. If the shutdown sequence has been initiated, but the device detects the wakeup criteria (either the TS or VCO pin voltage detected high) is present, then the device stays in a "soft shutdown" state until the wakeup criteria has been removed (meaning both the TS and VCO pin voltages must be detected low). While in "soft shutdown", FETs and protections are disabled. The device exits "soft shutdown" when conditions allow the device to continue into SHUTDOWN mode. If the host wants to abort the entry into SHUTDOWN mode, the *0x0012 RESET()*command can be written, and the device restarts operation as if returning from a POR.

When the SHUTDOWN mode sequence has been initiated by the stack voltage detected below ***Power:Shutdown:Shutdown Stack Voltage*** or a cell voltage detected below ***Power:Shutdown:Shutdown Cell Voltage***, the device asserts the *Alarm Raw Status()[SHUTV]* bit and wait for 10 seconds to disable the protection FETs, then proceed toward SHUTDOWN mode. During this 10 second shutdown delay, the device does not abort entering SHUTDOWN if the voltages rise back above the shutdown thresholds. If the host prefers to abort the SHUTDOWN entry, it can send the *0x0012 RESET()* command, and the device restarts with settings loaded from OTP.

When the device is wakened from SHUTDOWN, it requires < 10 ms for the internal circuitry to power up, load settings from OTP memory, evaluate conditions relative to enabled protections, then enable FETs if conditions allow.

7.4 CONFIG_UPDATE Mode

The BQ77307 uses a special CONFIG_UPDATE mode to make changes to the data memory settings. Note that this mode is not available for device versions programmed **and sealed** by TI. Changes made to the data memory settings while the normal protection evaluations are in operation can result in unexpected operation or consequences if settings used by the logic changed in the midst of operation. When changes to the data

memory settings are needed (which generally is done only on the customer manufacturing line or in an offline condition), the host must:

1. Send a command (such as *FET_CONTROL()*) to disable the protection FETs if they are enabled.
2. Place the device into CONFIG_UPDATE mode by sending the *0x0090 SET_CFGUPDATE()* subcommand.
3. Wait for the *0x12 Battery Status()[CFGUPDATE]* flag to set.
4. Modify settings as needed by writing updated data memory settings.
5. Send the *0x0092 EXIT_CFGUPDATE()* command to resume normal operation.

When in CONFIG_UPDATE mode, the device stops normal operation and stops all protections (the protection subsystem is disabled). The host can then make changes to data memory settings. After changes are complete, the host then sends the *0x0092 EXIT_CFGUPDATE()* command, at which point the device restarts normal operation using the new data memory settings. As soon as the device enters CONFIG_UPDATE mode, all protection alerts and status faults are cleared. When the device exits CONFIG_UDPATE mode, it evaluates whether or not any protection faults are present, based on the new settings.

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8.1 I²C Serial Communications Interface

The I²C serial communications interface in the BQ77307 device acts as a target device and supports rates up to 400 kHz with an optional CRC check. The BQ77307 initially powers up by default with CRC disabled, which is determined by the OTP settings factory programmed by TI. The host can change the CRC mode setting while in CONFIG_UPDATE mode, then the new setting takes effect upon exit of CONFIG_UPDATE mode.

The I²C device address (as an 8-bit value including target address and R/W bit) is set by default as 0x10 (write), 0x11 (read), which can be changed by the ***Settings:Configuration:I2C Address*** configuration setting.

The communications interface includes programmable timeout capability, with the internal I²C bus logic reset when an enabled timeout occurs:

- SCL Short Low Timeout - triggers if SCL stays low for approximately 25 ms. Enabled when ***Settings:Configuration:I2C Config[I2CCSLTO]*** is set.
- SCL Long Low Timeout - triggers if SCL stays low for a duration given by TLLO. TLLO is programmable using ***Settings:Configuration:I2C Config[I2CLLTOT2:0]*** as 0x0 = timeout is disabled, 0x1 = 0.5 sec, 0x2 = 1 sec, 0x3 = 1.5 sec, 0x4 = 2 sec, 0x5 = 2.5 sec, 0x6 = 3 sec, 0x7 = 3.5 sec. To use this timeout, ***Settings:Configuration:I2C Config[I2CLLTO]*** must be cleared.

An I²C write transaction is shown in I²C Write. Block writes are allowed by sending additional data bytes before the Stop. The I²C logic auto-increments the register address after each data byte. The shaded regions show when the device can clock stretch.

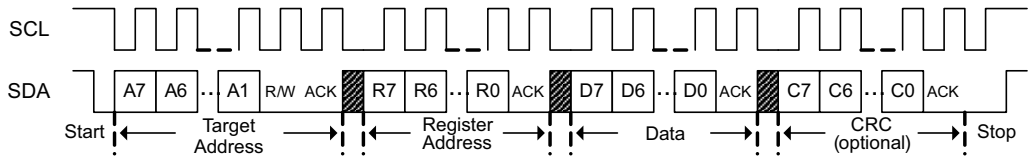

Figure 8-1. I²C Write

The CRC check is enabled by setting the ***Settings:Configuration:I2C Config[CRC]*** data memory bit. When enabled, the CRC is calculated as follows:

- The CRC is reset after each data byte and after each stop.
- In a single-byte write transaction, the CRC is calculated over the target address, register address, and data.
- In a block write transaction, the CRC for the first data byte is calculated over the target address, register address, and data. The CRC for subsequent data bytes is calculated over the data byte only.

The CRC polynomial is $x^8 + x^2 + x + 1$, and the initial value is 0.

When the target detects an invalid CRC, the I²C target NACKs the CRC, which causes the I²C target to go to an idle state.

I²C Read with Repeated Start shows a read transaction using a Repeated Start. The shaded regions show when the device can clock stretch.

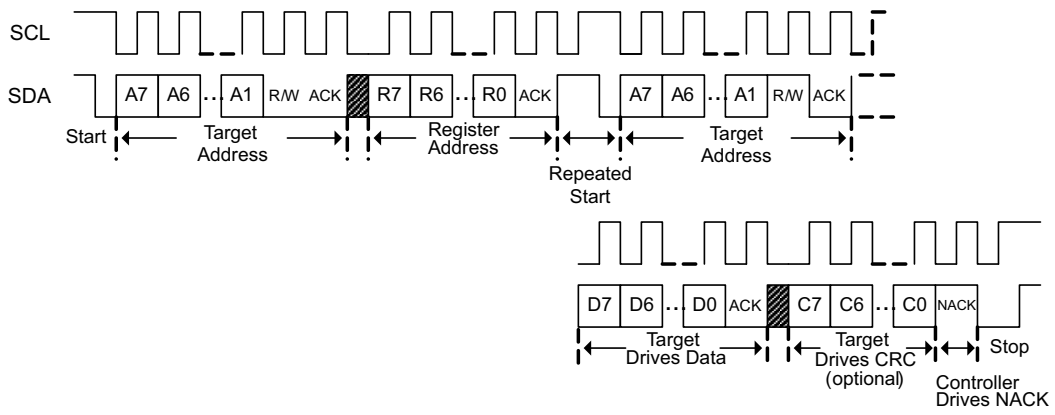

Figure 8-2. I²C Read with Repeated Start

I²C Read without Repeated Start shows a read transaction where a Repeated Start is not used, for example if not available in hardware. For a block read, the controller ACKs each data byte except the last and continues to clock the interface. The I²C block auto-increments the register address after each data byte. The shaded regions show when the device can clock stretch.

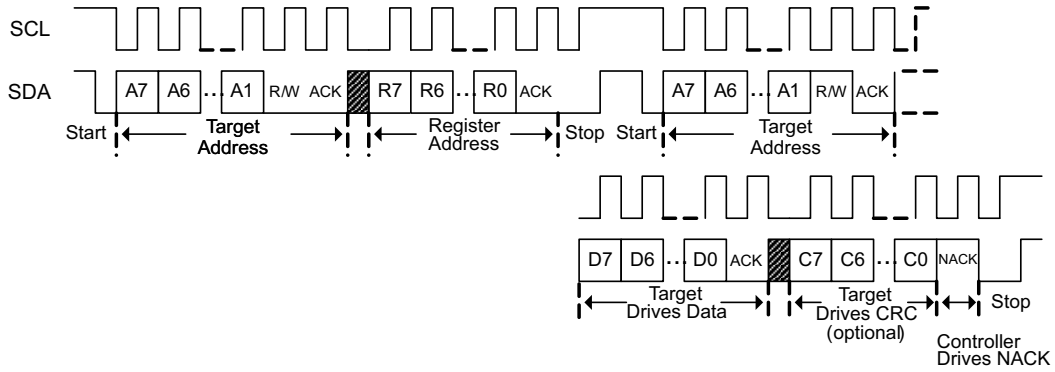

Figure 8-3. I²C Read without Repeated Start

When enabled, the CRC for a read transaction is calculated as follows:

- The CRC is reset after each data byte and after each stop.
- In a single-byte read transaction using a repeated start, the CRC is calculated beginning at the first start, so includes the target address, the register address, then the target address with read bit set, then the data byte.
- In a single-byte read transaction using a stop after the initial register address, the CRC is reset after the stop, so only includes the target address with read bit set and the data byte.
- In a block read transaction using repeated starts, the CRC for the first data byte is calculated beginning at the first start and includes the target address, the register address, then the target address with read bit set, then the data byte. The CRC for subsequent data bytes is calculated over the data byte only.
- In a block read transaction using a stop after the initial register address, the CRC is reset after the stop, so only includes the target address with read bit set and the first data byte. The CRC for subsequent data bytes is calculated over the data byte only.

The CRC polynomial is $x^8 + x^2 + x + 1$, and the initial value is 0.

When the controller detects an invalid CRC, the I²C controller NACKs the CRC, which causes the I²C target to go to an idle state.

9.1 Direct Commands

9.1.1 Direct Commands Table

Command	Name	Units	Type	Access	Description
0x02	Safety Alert A	Hex	H1	Sealed: R Full Access: R	Provides individual alert signals when enabled safety alerts have triggered. Bit descriptions can be found in Safety Alert A Register.
0x03	Safety Status A	Hex	H1	Sealed: R Full Access: R	Provides individual fault signals when enabled safety faults have triggered. Bit descriptions can be found in Safety Status A Register.
0x04	Safety Alert B	Hex	H1	Sealed: R Full Access: R	Provides individual alert signals when enabled safety alerts have triggered. Bit descriptions can be found in Safety Alert B Register.
0x05	Safety Status B	Hex	H1	Sealed: R Full Access: R	Provides individual fault signals when enabled safety faults have triggered. Bit descriptions can be found in Safety Status B Register.
0x12	Battery Status	Hex	H2	Sealed: R Full Access: R	Provides flags related to battery status. Bit descriptions can be found in Battery Status Register.
0x62	Alarm Status	Hex	H2	Sealed: R/W Full Access: R/W	Latched signal used to assert the ALERT pin. Write a bit high to clear the latched bit. Bit descriptions can be found in Alarm Status Register.
0x64	Alarm Raw Status	Hex	H2	Sealed: R Full Access: R	Unlatched value of flags which can be selected to be latched (using Alarm Enable()) and used to assert the ALERT pin. Bit descriptions can be found in Alarm Raw Status Register.
0x66	Alarm Enable	Hex	H2	Sealed: R/W Full Access: R/W	Mask for Alarm Status(). Can be written to change during operation to change which alarm sources are enabled. The default value of this parameter is set by Settings:Configuration:Default Alarm Mask. Bit descriptions can be found in Alarm Enable Register.
0x68	FET CONTROL	Hex	H1	Sealed: R/W Full Access: R/W	FET Control: Allows host control of individual FET drivers. Bit descriptions can be found in FET CONTROL Register.
0x69	REGOUT CONTROL	Hex	H1	Sealed: R/W Full Access: R/W	REGOUT Control: Changes voltage regulator settings. Bit descriptions can be found in REGOUT CONTROL Register.

9.2 Bit Field Definitions for Direct Commands

9.2.1 Safety Alert A Register

7	6	5	4	3	2	1	0
COV	CUV	SCD	OCD1	OCD2	OCC	RSVD0_1	RSVD0_0

Description: Provides individual alert signals when enabled safety alerts have triggered.

Table 9-1. Safety Alert A Register Field Descriptions

Bit	Field	Description
7	COV	Cell Overvoltage Safety Alert 0 = Indicates protection alert has not triggered 1 = indicates protection alert has triggered

Table 9-1. Safety Alert A Register Field Descriptions (continued)

Bit	Field	Description
6	CUV	Cell Undervoltage Safety Alert 0 = Indicates protection alert has not triggered 1 = indicates protection alert has triggered
5	SCD	Short Circuit in Discharge Safety Alert 0 = Indicates protection alert has not triggered 1 = indicates protection alert has triggered
4	OCD1	Overcurrent in Discharge 1 Safety Alert 0 = Indicates protection alert has not triggered 1 = indicates protection alert has triggered
3	OCD2	Overcurrent in Discharge 2 Safety Alert 0 = Indicates protection alert has not triggered 1 = indicates protection alert has triggered
2	OCC	Overcurrent in Charge Safety Alert 0 = Indicates protection alert has not triggered 1 = indicates protection alert has triggered

9.2.2 Safety Status A Register

7	6	5	4	3	2	1	0
COV	CUV	SCD	OCD1	OCD2	OCC	CURLATCH	REGOUT

Description: Provides individual fault signals when enabled safety faults have triggered.

Table 9-2. Safety Status A Register Field Descriptions

Bit	Field	Description
7	COV	Cell Overvoltage Safety Fault 0 = Indicates protection fault has not triggered 1 = indicates protection fault has triggered
6	CUV	Cell Undervoltage Safety Fault 0 = Indicates protection fault has not triggered 1 = indicates protection fault has triggered
5	SCD	Short Circuit in Discharge Safety Fault 0 = Indicates protection fault has not triggered 1 = indicates protection fault has triggered
4	OCD1	Overcurrent in Discharge 1 Safety Fault 0 = Indicates protection fault has not triggered 1 = indicates protection fault has triggered
3	OCD2	Overcurrent in Discharge 2 Safety Fault 0 = Indicates protection fault has not triggered 1 = indicates protection fault has triggered
2	OCC	Overcurrent in Charge Safety Fault 0 = Indicates protection fault has not triggered 1 = indicates protection fault has triggered
1	CURLATCH	Current Protection Latch Safety Fault 0 = Indicates the number of attempted current protection recoveries has not yet exceeded the latch count. 1 = Indicates the number of attempted current protection recoveries has exceeded the latch count, and autorecovery based on time is disabled.

Table 9-2. Safety Status A Register Field Descriptions (continued)

Bit	Field	Description
0	REGOUT	REGOUT Safety Fault 0 = Indicates protection fault has not triggered 1 = indicates protection fault has triggered

9.2.3 Safety Alert B Register

7	6	5	4	3	2	1	0
OTD	OTC	UTD	UTC	OTINT	RSVD0	VREF	VSS

Description: Provides individual alert signals when enabled safety alerts have triggered.

Table 9-3. Safety Alert B Register Field Descriptions

Bit	Field	Description
7	OTD	Overtemperature in Discharge Safety Alert 0 = Indicates protection alert has not triggered 1 = indicates protection alert has triggered
6	OTC	Overtemperature in Charge Safety Alert 0 = Indicates protection alert has not triggered 1 = indicates protection alert has triggered
5	UTD	Undertemperature in Discharge Safety Alert 0 = Indicates protection alert has not triggered 1 = indicates protection alert has triggered
4	UTC	Undertemperature in Charge Safety Alert 0 = Indicates protection alert has not triggered 1 = indicates protection alert has triggered
3	OTINT	Internal Overtemperature Safety Alert 0 = Indicates protection alert has not triggered 1 = indicates protection alert has triggered
2	RSVD0	Reserved
1	VREF	VREF Diagnostic Alert 0 = Indicates protection alert has not triggered 1 = indicates protection alert has triggered
0	VSS	VSS Diagnostic Alert 0 = Indicates protection alert has not triggered 1 = indicates protection alert has triggered

9.2.4 Safety Status B Register

7	6	5	4	3	2	1	0
OTD	OTC	UTD	UTC	OTINT	RSVD0	VREF	VSS

Description: Provides individual fault signals when enabled safety faults have triggered.

Table 9-4. Safety Status B Register Field Descriptions

Bit	Field	Description
7	OTD	Overtemperature in Discharge Safety Fault 0 = Indicates protection fault has not triggered 1 = indicates protection fault has triggered

Table 9-4. Safety Status B Register Field Descriptions (continued)

Bit	Field	Description
6	OTC	Overtemperature in Charge Safety Fault 0 = Indicates protection fault has not triggered 1 = indicates protection fault has triggered
5	UTD	Undertemperature in Discharge Safety Fault 0 = Indicates protection fault has not triggered 1 = indicates protection fault has triggered
4	UTC	Undertemperature in Charge Safety Fault 0 = Indicates protection fault has not triggered 1 = indicates protection fault has triggered
3	OTINT	Internal Overtemperature Safety Fault 0 = Indicates protection fault has not triggered 1 = indicates protection fault has triggered
2	RSVD0	Reserved
1	VREF	VREF Diagnostic Fault 0 = Indicates protection fault has not triggered 1 = indicates protection fault has triggered
0	VSS	VSS Diagnostic Fault 0 = Indicates protection fault has not triggered 1 = indicates protection fault has triggered

9.2.5 Battery Status Register

15	14	13	12	11	10	9	8
NORMAL	RSVD0	SA	SS	SEC_1	SEC_0	RSVD0	FET_EN
7	6	5	4	3	2	1	0
POR	RSVD0	CFGUPDATE	ALERTPIN	CHG	DSG	CHGDETFLAG	RSVD0

Description: Provides flags related to battery status.

Table 9-5. Battery Status Register Field Descriptions

Bit	Field	Description
15	NORMAL	This flag asserts when the device is in NORMAL mode. 0 = Indicates the device is not in NORMAL mode. 1 = Indicates the device is in NORMAL mode.
13	SA	This flag asserts if an enabled safety alert is present. 0 = Indicates an enabled safety alert is not present 1 = Indicates an enabled safety alert is present
12	SS	This flag asserts if an enabled safety fault is present. 0 = Indicates an enabled safety fault is not present 1 = Indicates an enabled safety fault is present

Table 9-5. Battery Status Register Field Descriptions (continued)

Bit	Field	Description
11–10	SEC_1–SEC_0	SEC1:0 indicate the present security state of the device. When in SEALED mode, device configuration cannot be read or written and some commands are restricted. When in FULLACCESS mode, unrestricted read and write access is allowed and all commands are accepted. 0 = 0: Device has not initialized yet. 1 = 1: Device is in FULLACCESS mode. 2 = 2: Unused. 3 = 3: Device is in SEALED mode.
8	FET_EN	This bit is set when the device is in autonomous FET control mode. The default value of this bit is set by the Settings:FET Options[FET_EN] bit in Data Memory upon exit of CONFIG_UPDATE mode. Its value can be modified during operation using the FET_ENABLE() subcommand. 0 = Device is not in autonomous FET control mode, FETs are only enabled through manual command. 1 = Device is in autonomous FET control mode, FETs can be enabled by the device if no conditions or commands prevent them being enabled.
7	POR	This bit is set when the device fully resets. It is cleared upon exit of CONFIG_UPDATE mode. It can be used by the host to determine if any RAM configuration changes were lost due to a reset. 0 = Full reset has not occurred since last exit of CONFIG_UPDATE mode. 1 = Full reset has occurred since last exit of CONFIG_UPDATE and reconfiguration of any RAM settings is required.
5	CFGUPDATE	This bit indicates whether or not the device is in CONFIG_UPDATE mode. It is set after the SET_CFGUPDATE() subcommand is received and fully processed. Configuration settings can be changed only while this bit is set. 0 = Device is not in CONFIG_UPDATE mode. 1 = Device is in CONFIG_UPDATE mode.
4	ALERTPIN	This bit indicates whether the ALERT pin is asserted (pulled low). 0 = ALERT pin is not asserted (stays in hi-Z mode). 1 = ALERT pin is asserted (pulled low).
3	CHG	This bit indicates whether the CHG driver is enabled. 0 = CHG driver is disabled. 1 = CHG driver is enabled.
2	DSG	This bit indicates whether the DSG driver is enabled. 0 = DSG driver is disabled. 1 = DSG driver is enabled.
1	CHGDETFLAG	This bit indicates the value of the debounced CHG Detector signal. 0 = CHG Detector debounced signal is low. 1 = CHG Detector debounced signal is high.

9.2.6 Alarm Status Register

15	14	13	12	11	10	9	8
SSA	SSB	SAA	SAB	XCHG	XDSG	SHUTV	RSVD0
7	6	5	4	3	2	1	0
CHECK	CHECK	RSVD0	RSVD0	RSVD0	INITCOMP	CDTOGGLE	POR

Description: Latched signal used to assert the ALERT pin. Write a bit high to clear the latched bit.

Table 9-6. Alarm Status Register Field Descriptions

Bit	Field	Description
15	SSA	This bit is latched when a bit in Safety Status A() is set, and the bit is included in the mask. The bit is cleared when written with a "1". A bit set here causes the ALERT pin to be asserted low. 0 = Flag is not set 1 = Flag is set
14	SSB	This bit is latched when a bit in Safety Status B() is set, and the bit is included in the mask. The bit is cleared when written with a "1". A bit set here causes the ALERT pin to be asserted low. 0 = Flag is not set 1 = Flag is set
13	SAA	This bit is latched when a bit in Safety Alert A() is set, and the bit is included in the mask. The bit is cleared when written with a "1". A bit set here causes the ALERT pin to be asserted low. 0 = Flag is not set 1 = Flag is set
12	SAB	This bit is latched when a bit in Safety Alert B() is set, and the bit is included in the mask. The bit is cleared when written with a "1". A bit set here causes the ALERT pin to be asserted low. 0 = Flag is not set 1 = Flag is set
11	XCHG	This bit is latched when the CHG driver is disabled, and the bit is included in the mask. The bit is cleared when written with a "1". A bit set here causes the ALERT pin to be asserted low. 0 = Flag is not set 1 = Flag is set
10	XDSG	This bit is latched when the DSG driver is disabled, and the bit is included in the mask. The bit is cleared when written with a "1". A bit set here causes the ALERT pin to be asserted low. 0 = Flag is not set 1 = Flag is set
9	SHUTV	This bit is latched when either a cell voltage has been detected below Shutdown Cell Voltage, or the stack voltage has been detected below Shutdown Stack Voltage. The bit is cleared when written with a "1". A bit set here causes the ALERT pin to be asserted low. 0 = Flag is not set 1 = Flag is set
7	CHECK	This bit is latched when the device completes a CHECK interval while in NORMAL mode, and the bit is included in the mask. The bit is cleared when written with a "1". A bit set here causes the ALERT pin to be asserted low. 0 = Flag is not set 1 = Flag is set
6	CHECK	This bit is latched when the device completes a CHECK interval while in NORMAL mode, and the bit is included in the mask. The bit is cleared when written with a "1". A bit set here causes the ALERT pin to be asserted low. 0 = Flag is not set 1 = Flag is set
2	INITCOMP	This bit is latched when the device first powers up or exits CONFIG_UPDATE mode, loads settings, and completes first evaluation of conditions related to enabled protections, and the bit is included in the mask. The bit is cleared when written with a "1". A bit set here causes the ALERT pin to be asserted low. 0 = Flag is not set 1 = Flag is set
1	CDTOGGLE	This bit is latched when the debounced CHG Detector signal is different from the last debounced value. 0 = Flag is not set 1 = Flag is set

Table 9-6. Alarm Status Register Field Descriptions (continued)

Bit	Field	Description
0	POR	This bit is latched when the POR bit in Battery Status is asserted. 0 = Flag is not set 1 = Flag is set

9.2.7 Alarm Raw Status Register

15	14	13	12	11	10	9	8
SSA	SSB	SAA	SAB	XCHG	XDSG	SHUTV	RSVD0
7	6	5	4	3	2	1	0
CHECK	CHECK	RSVD0	RSVD0	RSVD0	INITCOMP	CDRAW	POR

Description: Unlatched value of flags which can be selected to be latched (using Alarm Enable()) and used to assert the ALERT pin.

Table 9-7. Alarm Raw Status Register Field Descriptions

Bit	Field	Description
15	SSA	This bit is set when a bit in Safety Status A() is set. 0 = Flag is not set 1 = Flag is set
14	SSB	This bit is set when a bit in Safety Status B() is set. 0 = Flag is not set 1 = Flag is set
13	SAA	This bit is set when a bit in Safety Alert A() is set. 0 = Flag is not set 1 = Flag is set
12	SAB	This bit is set when a bit in Safety Alert B() is set. 0 = Flag is not set 1 = Flag is set
11	XCHG	This bit is set when the CHG driver is disabled. 0 = Flag is not set 1 = Flag is set
10	XDSG	This bit is set when the DSG driver is disabled. 0 = Flag is not set 1 = Flag is set
9	SHUTV	This bit is set when either a cell voltage has been detected below Shutdown Cell Voltage, or the stack voltage has been detected below Shutdown Stack Voltage. The bit is cleared when written with a "1". A bit set here causes the ALERT pin to be asserted low. 0 = Flag is not set 1 = Flag is set
7	CHECK	Bits 6 and 7 pulse high briefly every CHECK interval when the device is in NORMAL mode.
6	CHECK	Bits 6 and 7 pulse high briefly every CHECK interval when the device is in NORMAL mode.
2	INITCOMP	This bit pulses high briefly when the device first powers up or exits CONFIG_UPDATE mode, loads settings, and completes the first evaluation of conditions related to enabled protections.
1	CDRAW	This bit is set when the CHG Detector output is set, indicating that the CHG pin has been detected above a level of approximately 2 V. 0 = CHG Detector output is not set 1 = CHG Detector output is set

Table 9-7. Alarm Raw Status Register Field Descriptions (continued)

Bit	Field	Description
0	POR	This bit is set if the POR bit in Battery Status is asserted. 0 = Flag is not set 1 = Flag is set

9.2.8 Alarm Enable Register

15	14	13	12	11	10	9	8
SSA	SSB	SAA	SAB	XCHG	XDSG	SHUTV	RSVD0
7	6	5	4	3	2	1	0
CHECK	CHECK	RSVD0	RSVD0	RSVD0	INITCOMP	CDTOGGLE	POR

Description: Mask for Alarm Status(). Can be written to change during operation to change which alarm sources are enabled. The default value of this parameter is set by Settings:Configuration:Default Alarm Mask.

Table 9-8. Alarm Enable Register Field Descriptions

Bit	Field	Description
15	SSA	Setting this bit allows the corresponding bit in Alarm Raw Status() to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. 0 = This bit in Alarm Raw Status() is not included in Alarm Status() 1 = This bit in Alarm Raw Status() is included in Alarm Status()
14	SSB	Setting this bit allows the corresponding bit in Alarm Raw Status() to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. 0 = This bit in Alarm Raw Status() is not included in Alarm Status() 1 = This bit in Alarm Raw Status() is included in Alarm Status()
13	SAA	Setting this bit allows the corresponding bit in Alarm Raw Status() to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. 0 = This bit in Alarm Raw Status() is not included in Alarm Status() 1 = This bit in Alarm Raw Status() is included in Alarm Status()
12	SAB	Setting this bit allows the corresponding bit in Alarm Raw Status() to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. 0 = This bit in Alarm Raw Status() is not included in Alarm Status() 1 = This bit in Alarm Raw Status() is included in Alarm Status()
11	XCHG	Setting this bit allows the corresponding bit in Alarm Raw Status() to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. 0 = This bit in Alarm Raw Status() is not included in Alarm Status() 1 = This bit in Alarm Raw Status() is included in Alarm Status()
10	XDSG	Setting this bit allows the corresponding bit in Alarm Raw Status() to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. 0 = This bit in Alarm Raw Status() is not included in Alarm Status() 1 = This bit in Alarm Raw Status() is included in Alarm Status()
9	SHUTV	Setting this bit allows the corresponding bit in Alarm Raw Status() to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. 0 = This bit in Alarm Raw Status() is not included in Alarm Status() 1 = This bit in Alarm Raw Status() is included in Alarm Status()
7	CHECK	Setting this bit allows the corresponding bit in Alarm Raw Status() to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. 0 = This bit in Alarm Raw Status() is not included in Alarm Status() 1 = This bit in Alarm Raw Status() is included in Alarm Status()

Table 9-8. Alarm Enable Register Field Descriptions (continued)

Bit	Field	Description
6	CHECK	Setting this bit allows the corresponding bit in Alarm Raw Status() to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. 0 = This bit in Alarm Raw Status() is not included in Alarm Status() 1 = This bit in Alarm Raw Status() is included in Alarm Status()
2	INITCOMP	Setting this bit allows the corresponding bit in Alarm Raw Status() to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. 0 = This bit in Alarm Raw Status() is not included in Alarm Status() 1 = This bit in Alarm Raw Status() is included in Alarm Status()
1	CDTOGGLE	Setting this bit allows the internally determined value of CDTOGGLE to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. This flag is set whenever the debounced CHG Detector signal differs from the previous debounced value. 0 = The CDTOGGLE signal is not included in Alarm Status() 1 = The CDTOGGLE signal is included in Alarm Status()
0	POR	Setting this bit allows the corresponding bit in Alarm Raw Status() to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. 0 = This bit in Alarm Raw Status() is not included in Alarm Status() 1 = This bit in Alarm Raw Status() is included in Alarm Status()

9.2.9 FET CONTROL Register

7	6	5	4	3	2	1	0
RSVD0_3	RSVD0_2	RSVD0_1	RSVD0_0	CHG_OFF	DSG_OFF	CHG_ON	DSG_ON

Description: FET Control: Allows host control of individual FET drivers.

Table 9-9. FET CONTROL Register Field Descriptions

Bit	Field	Description
3	CHG_OFF	CHG FET driver control. This bit only operates if the HOST_FETOFF_EN bit in data memory is set. 0 = CHG FET driver is allowed to turn on if other conditions are met. 1 = CHG FET driver is forced off.
2	DSG_OFF	DSG FET driver control. This bit only operates if the HOST_FETOFF_EN bit in data memory is set. 0 = DSG FET driver is allowed to turn on if other conditions are met. 1 = DSG FET driver is forced off.
1	CHG_ON	CHG FET driver control. This bit only operates if the HOST_FETON_EN bit in data memory is set. 0 = CHG FET driver is allowed to turn on if other conditions are met. 1 = CHG FET driver is forced on.
0	DSG_ON	DSG FET driver control. This bit only operates if the HOST_FETON_EN bit in data memory is set. 0 = DSG FET driver is allowed to turn on if other conditions are met. 1 = DSG FET driver is forced on.

9.2.10 REGOUT CONTROL Register

7	6	5	4	3	2	1	0
RSVD0_2	RSVD0_1	RSVD0_0	TS_ON	REG_EN	REGOUTV_2	REGOUTV_1	REGOUTV_0

Description: REGOUT Control: Changes voltage regulator settings.

Table 9-10. REGOUT CONTROL Register Field Descriptions

Bit	Field	Description
4	TS_ON	Control for TS pullup to stay biased continuously. 0 = TS pullup resistor is not continuously connected. 1 = TS pullup resistor is continuously connected.
3	REG_EN	REGOUT LDO enable. 0 = REGOUT LDO is disabled 1 = REGOUT LDO is enabled
2–0	REGOUTV_2–REGOUTV_0	REGOUT LDO voltage control. 0 = REGOUT LDO is set to 1.8V 1 = REGOUT LDO is set to 1.8V 2 = REGOUT LDO is set to 1.8V 3 = REGOUT LDO is set to 1.8V 4 = REGOUT LDO is set to 2.5 V 5 = REGOUT LDO is set to 3.0 V 6 = REGOUT LDO is set to 3.3 V 7 = REGOUT LDO is set to 5 V

9.3 Command-only Subcommands

Table of Command-only Subcommands

Command	Name	Access	Description
0x0012	RESET	Sealed: — Full Access: W	This command is sent to reset the device
0x0022	FET_ENABLE	Sealed: — Full Access: W	This command is sent to toggle the FET_EN bit in Battery Status(). FET_EN=0 means manual FET control. FET_EN=1 means autonomous device FET control
0x0030	SEAL	Sealed: — Full Access: W	This command is sent to place the device in SEALED mode
0x0090	SET_CFGUPDATE	Sealed: — Full Access: W	This command is sent to place the device in CONFIG_UPDATE mode
0x0092	EXIT_CFGUPDATE	Sealed: — Full Access: W	This command is sent to exit CONFIG_UPDATE mode

9.4 Subcommands with Data

Subcommands Table

Command	Name	Access	Offset	Data	Units	Type	Description
0x0001	DEVICE_NUMBER	Sealed: R Full Access: R	0	DEVICE NUMBER	Hex	H2	The DEVICE_NUMBER subcommand reports the device number that identifies the product. The data is returned in little-endian format Bit descriptions can be found in DEVICE NUMBER Register.
0x0002	FW_VERSION	Sealed: R Full Access: R	0	FW VERSION	Hex	H6	The FW_VERSION subcommand returns three 16-bit word values. Bytes 0-1: Device Number (Big-Endian): Device number in big-endian format for compatibility with legacy products. Bytes 3-2: Firmware Version (Big-Endian): Device firmware major and minor version number (Big-Endian). Bytes 5-4: Build Number (Big-Endian): Firmware build number in big-endian, binary coded decimal format for compatibility with legacy products Bit descriptions can be found in FW VERSION Register.

Command	Name	Access	Offset	Data	Units	Type	Description
0x0003	HW_VERSION	Sealed: R Full Access: R	0	HW VERSION	Hex	H2	Hardware Version: Reports the device hardware version number Bit descriptions can be found in HW VERSION Register.
0x0035	SECURITY_KEYS	Sealed: — Full Access: W	0	SECURITY KEYS	Hex	H4	Security key that must be sent to transition from SEALED to FULLACCESS mode. The subcommand includes two 16-bit words Bit descriptions can be found in SECURITY KEYS Register.
0x009b	PROT_RECOVERY	Sealed: R Full Access: R/W	0	PROT RECOVERY	Hex	H1	This command enables the host to allow recovery of selected protection faults Bit descriptions can be found in PROT RECOVERY Register.

9.5 Bitfield Definitions for Subcommands

9.5.1 DEVICE NUMBER Register

15	14	13	12	11	10	9	8
DEVNUM_15	DEVNUM_14	DEVNUM_13	DEVNUM_12	DEVNUM_11	DEVNUM_10	DEVNUM_9	DEVNUM_8
7	6	5	4	3	2	1	0
DEVNUM_7	DEVNUM_6	DEVNUM_5	DEVNUM_4	DEVNUM_3	DEVNUM_2	DEVNUM_1	DEVNUM_0

Description: The DEVICE_NUMBER subcommand reports the device number that identifies the product. The data is returned in little-endian format

Table 9-11. DEVICE NUMBER Register Field Descriptions

Bit	Field	Description
15–0	DEVNUM_15–DEVNUM_0	Reports the device number that identifies the product. The data is returned in little-endian format.

9.5.2 FW VERSION Register

47	46	45	44	43	42	41	40
FVBLDNUM_15	FVBLDNUM_14	FVBLDNUM_13	FVBLDNUM_12	FVBLDNUM_11	FVBLDNUM_10	FVBLDNUM_9	FVBLDNUM_8
39	38	37	36	35	34	33	32
FVBLDNUM_7	FVBLDNUM_6	FVBLDNUM_5	FVBLDNUM_4	FVBLDNUM_3	FVBLDNUM_2	FVBLDNUM_1	FVBLDNUM_0
31	30	29	28	27	26	25	24
FVFWVER_15	FVFWVER_14	FVFWVER_13	FVFWVER_12	FVFWVER_11	FVFWVER_10	FVFWVER_9	FVFWVER_8
23	22	21	20	19	18	17	16
FVFWVER_7	FVFWVER_6	FVFWVER_5	FVFWVER_4	FVFWVER_3	FVFWVER_2	FVFWVER_1	FVFWVER_0
15	14	13	12	11	10	9	8

FVDEVNUM_15	FVDEVNUM_14	FVDEVNUM_13	FVDEVNUM_12	FVDEVNUM_11	FVDEVNUM_10	FVDEVNUM_9	FVDEVNUM_8
7	6	5	4	3	2	1	0
FVDEVNUM_7	FVDEVNUM_6	FVDEVNUM_5	FVDEVNUM_4	FVDEVNUM_3	FVDEVNUM_2	FVDEVNUM_1	FVDEVNUM_0

Description: The FW_VERSION subcommand returns three 16-bit word values. Bytes 0-1: Device Number (Big-Endian): Device number in big-endian format for compatibility with legacy products. Bytes 3-2: Firmware Version (Big-Endian): Device firmware major and minor version number (Big-Endian). Bytes 5-4: Build Number (Big-Endian): Firmware build number in big-endian, binary coded decimal format for compatibility with legacy products

Table 9-12. FW VERSION Register Field Descriptions

Bit	Field	Description
47–32	FVBLDNUM_15–FVBLDNUM_0	Build Number (Big-Endian): Firmware build number in big-endian, binary coded decimal format for compatibility with legacy products
31–16	FVFWVER_15–FVFWVER_0	Firmware Version (Big-Endian): Device firmware major and minor version number (Big-Endian)
15–0	FVDEVNUM_15–FVDEVNUM_0	Device Number (Big-Endian): Device number in big-endian format for compatibility with legacy products

9.5.3 HW VERSION Register

15	14	13	12	11	10	9	8
HWVER_15	HWVER_14	HWVER_13	HWVER_12	HWVER_11	HWVER_10	HWVER_9	HWVER_8
7	6	5	4	3	2	1	0
HWVER_7	HWVER_6	HWVER_5	HWVER_4	HWVER_3	HWVER_2	HWVER_1	HWVER_0

Description: Hardware Version: Reports the device hardware version number

Table 9-13. HW VERSION Register Field Descriptions

Bit	Field	Description
15–0	HWVER_15–HWVER_0	Hardware Version: Reports the device hardware version number.

9.5.4 SECURITY KEYS Register

31	30	29	28	27	26	25	24
FAKEY2_6_15	FAKEY2_6_14	FAKEY2_6_13	FAKEY2_6_12	FAKEY2_6_11	FAKEY2_6_10	FAKEY2_6_9	FAKEY2_6_8
23	22	21	20	19	18	17	16
FAKEY2_6_7	FAKEY2_6_6	FAKEY2_6_5	FAKEY2_6_4	FAKEY2_6_3	FAKEY2_6_2	FAKEY2_6_1	FAKEY2_6_0
15	14	13	12	11	10	9	8
FAKEY1__15	FAKEY1__14	FAKEY1__13	FAKEY1__12	FAKEY1__11	FAKEY1__10	FAKEY1__9	FAKEY1__8
7	6	5	4	3	2	1	0

FAKEY1__7	FAKEY1__6	FAKEY1__5	FAKEY1__4	FAKEY1__3	FAKEY1__2	FAKEY1__1	FAKEY1__0

Description: Security key that must be sent to transition from SEALED to FULLACCESS mode. The subcommand includes two 16-bit words

Table 9-14. SECURITY KEYS Register Field Descriptions

Bit	Field	Description
31–16	FAKEY2_6_15–FAKEY2_6_0	Full Access Key Step 2: This is the second word of the security key that must be sent to transition from SEALED to FULLACCESS mode. Do not choose a word that is identical to a subcommand address or the same as the first word. This word must be sent within 5 seconds of the first word of the key and with no other commands in between.
15–0	FAKEY1__15–FAKEY1__0	Full Access Key Step 1: This is the first word of the security key that must be sent to transition from SEALED to FULLACCESS mode. Do not choose a word that is identical to a subcommand address.

9.5.5 PROT RECOVERY Register

7	6	5	4	3	2	1	0
VOLTREC	DIAGREC	SCDREC	OCD1REC	OCD2REC	OCCREC	TEMPREC	RSVD0

Description: This command enables the host to allow recovery of selected protection faults

Table 9-15. PROT RECOVERY Register Field Descriptions

Bit	Field	Description
7	VOLTREC	Cell Overvoltage or Cell Undervoltage fault recovery 0 = Recovery of an COV/CUV fault is not triggered 1 = Recovery of an COV/CUV fault is triggered.
6	DIAGREC	Recovery for a VSS or VREF fault from Safety Status B() 0 = Recovery of a VSS or VREF fault is not triggered 1 = Recovery of a VSS or VREF fault is triggered.
5	SCDREC	Short Circuit in Discharge fault recovery 0 = Recovery of an SCD fault is not triggered 1 = Recovery of an SCD fault is triggered.
4	OCD1REC	Overcurrent in Discharge 1 fault recovery 0 = Recovery of an OCD1 fault is not triggered 1 = Recovery of an OCD1 fault is triggered.
3	OCD2REC	Overcurrent in Discharge 2 fault recovery 0 = Recovery of an OCD2 fault is not triggered 1 = Recovery of an OCD2 fault is triggered.
2	OCCREC	Overcurrent in Charge fault recovery 0 = Recovery of an OCC fault is not triggered 1 = Recovery of an OCC fault is triggered.
1	TEMPREC	Temperature fault recovery 0 = Recovery of a temperature fault is not triggered 1 = Recovery of a temperature fault is triggered.

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10.1 Settings

10.1.1 Settings:Configuration

10.1.1.1 Settings:Configuration:Reserved

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Configuration	Reserved	H2	0x0000	0xFFFF	-	Hex

7	6	5	4	3	2	1	0
RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD

Description: This register is reserved, do not write to this register.

10.1.1.2 Settings:Configuration:Power Config

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Configuration	Power Config	H1	0x00	0xFF	0x01	Hex

7	6	5	4	3	2	1	0
RSVD0	RSVD0	RSVD0	RSVD0	OTSD	LFOWD	RSVD0	RSVD1

Description: This register contains settings that affect the power control of the device

Table 10-1. Power Config Register Field Descriptions

Bit	Field	Default	Description
3	OTSD	0	Determines whether or not the device shuts down if the die HW overtemperature detector triggers a fault. 0 = Do not shutdown when the HW OT triggers 1 = Device enters shutdown when the HW OT triggers
2	LFOWD	0	Determines whether or not the device shuts down if the LFO watchdog triggers a fault. 0 = Do not shutdown the device when an LFO watchdog fault occurs. 1 = Shutdown the device when an LFO watchdog fault occurs.

10.1.1.3 Settings:Configuration:REGOUT Config

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Configuration	REGOUT Config	H1	0x00	0xFF	0x08	Hex

7	6	5	4	3	2	1	0
RSVD0_3	RSVD0_2	RSVD0_1	RSVD0_0	REG_EN	REGCTL_2	REGCTL_1	REGCTL_0

Description: This register contains settings to control the REGOUT voltage regulator

Table 10-2. REGOUT Config Register Field Descriptions

Bit	Field	Default	Description
3	REG_EN	1	Default value of enable for REG_EN. This value is used upon exit of CONFIG_UPDATE mode, but can be modified during operation using the REGOUT Control() command. 0 = REGOUT is not enabled (default) 1 = REGOUT is enabled
2–0	REGCTL_2–REGCTL_0	0	Default value for the REGOUT LDO settings. This value is used upon exit of CONFIG_UPDATE mode, but can be modified during operation using the REGOUT Control() command. 0 = Set to 1.8V 1 = Set to 1.8V 2 = Set to 1.8V 3 = Set to 1.8V 4 = Set to 2.5V 5 = Set to 3.0V 6 = Set to 3.3V (default) 7 = Set to 5V

10.1.1.4 Settings:Configuration:I2C Address

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Configuration	I2C Address	H1	0x00	0x7F	0x08	Hex

7	6	5	4	3	2	1	0
RSVD0	I2CADDR_6	I2CADDR_5	I2CADDR_4	I2CADDR_3	I2CADDR_2	I2CADDR_1	I2CADDR_0

Description: This register sets the I^2C address for the serial communications interface

Table 10-3. I2C Address Register Field Descriptions

Bit	Field	Default	Description
6–0	I2CADDR_6–I2CADDR_0	8	7-bit I^2C Address. 0 = The device uses address 0x08. All other values are used as the address directly.

10.1.1.5 Settings:Configuration:I2C Config

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Configuration	I2C Config	H2	0x0000	0xFFFF	0x3400	Hex

15	14	13	12	11	10	9	8
I2CCSLTO	I2CCSHTO	I2CCSHTOT_1	I2CCSHTOT_0	I2CLLTO	I2CLLTOT_2	I2CLLTOT_1	I2CLLTOT_0

7	6	5	4	3	2	1	0
RSVD0_5	RSVD0_4	RSVD0_3	RSVD0_2	RSVD0_1	RSVD0_0	I2CBBTO	CRC

Description: This register includes configuration settings for the I^2C address for the serial communications interface

Table 10-4. I2C Config Register Field Descriptions

Bit	Field	Default	Description
15	I2CCSLTO	0	SCL Short Low Timeout, times out I²C logic if SCL is detected low for approximately 25ms 0 = Timeout is not enabled (default) 1 = Timeout is enabled
14	I2CCSHTO	0	SCL Short High Timeout, times out I²C logic if SCL is detected high for duration given by I²CCSHTOT1:0 0 = Timeout is not enabled (default) 1 = Timeout is enabled
13–12	I2CCSHTOT_1–I2CCSHTOT_0	3	SCL Short High Timeout Duration 0 = Timeout occurs after 64 ms 1 = Timeout occurs after 512 ms 2 = Timeout occurs after 1 ms 3 = Timeout occurs after 15 ms (default)
11	I2CLLTO	0	Long Low Timeout, times out I²C logic if SCL or SCL and SDA are detected low for duration given by I²CLLTOT 0 = Timeout occurs if SCL is detected low for duration I²CLLTOT (default) 1 = Timeout occurs if both SCL and SDA are detected low for duration I²CLLTOT
10–8	I2CLLTOT_2–I2CLLTOT_0	4	Long Low Timeout Duration 0 = Timeout is disabled 1 = Timeout occurs after 0.5 seconds 2 = Timeout occurs after 1 seconds 3 = Timeout occurs after 1.5 seconds 4 = Timeout occurs after 2 seconds (default) 5 = Timeout occurs after 2.5 seconds 6 = Timeout occurs after 3 seconds 7 = Timeout occurs after 3.5 seconds
1	I2CBBTO	0	I²C Bus Busy Timeout, times out I²C logic if a transaction is detected longer than the duration given by I²CLLTOT2:0 0 = Timeout is not enabled (default) 1 = Timeout is enabled
0	CRC	0	Controls whether the I²C serial communications interface uses CRC. 0 = CRC is not used (default) 1 = CRC is enabled

10.1.1.6 Settings:Configuration:TS Mode

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Configuration	TS Mode	H1	0x00	0x01	0x00	Hex

7	6	5	4	3	2	1	0
RSVD0	RSVD0	RSVD0	RSVD0	RSVD0	RSVD0	RSVD0	TSMODE

Description: This register includes a configuration setting related to the TS pin operation.

Table 10-5. TS Mode Register Field Descriptions

Bit	Field	Default	Description
0	TSMODE	0	This bit controls whether the TS pin is used for external thermistor temperature protection. 0 = TS pin is used for external thermistor temperature protection, with the internal pullup resistor enabled during each evaluation. 1 = TS pin is not used for external thermistor temperature protection.

10.1.1.7 Settings:Configuration:Vcell Mode

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Configuration	Vcell Mode	H1	0x00	0x07	0x0	Hex

7	6	5	4	3	2	1	0
RSVD0_4	RSVD0_3	RSVD0_2	RSVD0_1	RSVD0_0	VCELL_2	VCELL_1	VCELL_0

Description: Not every system uses all of the cell input pins. If the system has fewer cells than the device supports, some VC input pins must be shorted together. To prevent action being taken for cell under-voltage conditions on pins that are shorted, set these bits appropriately

Table 10-6. Vcell Mode Register Field Descriptions

Bit	Field	Default	Description
2–0	VCELL_2–VCELL_0	0	Not every system uses all of the cell input pins. If the system has fewer cells than the device supports, some VC input pins must be shorted together. To prevent action being taken for cell under-voltage conditions on pins that are shorted, set these bits appropriately. 0 = All cell inputs are used for actual cells. 1 = All cell inputs are used for actual cells. 2 = Two actual cells are in use (VC7-VC6, VC1-VC0), short unused cell pins to an adjacent cell pin at the device. 3 = Three actual cells are in use (VC7-VC6, VC5-VC4, VC1-VC0), short unused cell pins to an adjacent cell pin at the device. 4 = Four actual cells are in use (VC7-VC6, VC5-VC4, VC3-VC2, VC1-VC0), short unused cell pins to an adjacent cell pin at the device. 5 = Five actual cells are in use (VC7-VC6, VC5-VC4, VC3-VC2, VC2-VC1, VC1-VC0), short unused cell pins to an adjacent cell pin at the device. 6 = Six actual cells are in use (all except VC4-VC3), short pins VC4 and VC3 together at the device. 7 = All cell inputs are used for actual cells.

10.1.1.8 Settings:Configuration:Default Alarm Mask

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Configuration	Default Alarm Mask	H2	0x0000	0xFFFF	0xC200	Hex

15	14	13	12	11	10	9	8
SSA	SSB	SAA	SAB	XCHG	XDSG	SHUTV	RSVD0

7	6	5	4	3	2	1	0
CHECK	CHECK	RSVD0	RSVD0	RSVD0	INITCOMP	CDTOGGLE	POR

Description: This parameter sets the default value of the AlarmEnable() register. The default value is reloaded at reset (if programmed into OTP) and at exit of CONFIG_UPDATE mode

Table 10-7. Default Alarm Mask Register Field Descriptions

Bit	Field	Default	Description
15	SSA	1	Setting this bit allows the corresponding bit in Alarm Raw Status() to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. 0 = This bit in Alarm Raw Status() is not included in Alarm Status() 1 = This bit in Alarm Raw Status() is included in Alarm Status()

Table 10-7. Default Alarm Mask Register Field Descriptions (continued)

Bit	Field	Default	Description
14	SSB	1	Setting this bit allows the corresponding bit in Alarm Raw Status() to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. 0 = This bit in Alarm Raw Status() is not included in Alarm Status() 1 = This bit in Alarm Raw Status() is included in Alarm Status()
13	SAA	0	Setting this bit allows the corresponding bit in Alarm Raw Status() to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. 0 = This bit in Alarm Raw Status() is not included in Alarm Status() 1 = This bit in Alarm Raw Status() is included in Alarm Status()
12	SAB	0	Setting this bit allows the corresponding bit in Alarm Raw Status() to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. 0 = This bit in Alarm Raw Status() is not included in Alarm Status() 1 = This bit in Alarm Raw Status() is included in Alarm Status()
11	XCHG	0	Setting this bit allows the corresponding bit in Alarm Raw Status() to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. 0 = This bit in Alarm Raw Status() is not included in Alarm Status() 1 = This bit in Alarm Raw Status() is included in Alarm Status()
10	XDSG	0	Setting this bit allows the corresponding bit in Alarm Raw Status() to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. 0 = This bit in Alarm Raw Status() is not included in Alarm Status() 1 = This bit in Alarm Raw Status() is included in Alarm Status()
9	SHUTV	1	Setting this bit allows the corresponding bit in Alarm Raw Status() to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. 0 = This bit in Alarm Raw Status() is not included in Alarm Status() 1 = This bit in Alarm Raw Status() is included in Alarm Status()
7	CHECK	0	Setting this bit allows the corresponding bit in Alarm Raw Status() to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. 0 = This bit in Alarm Raw Status() is not included in Alarm Status() 1 = This bit in Alarm Raw Status() is included in Alarm Status()
6	CHECK	0	Setting this bit allows the corresponding bit in Alarm Raw Status() to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. 0 = This bit in Alarm Raw Status() is not included in Alarm Status() 1 = This bit in Alarm Raw Status() is included in Alarm Status()
2	INITCOMP	0	Setting this bit allows the corresponding bit in Alarm Raw Status() to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. 0 = This bit in Alarm Raw Status() is not included in Alarm Status() 1 = This bit in Alarm Raw Status() is included in Alarm Status()
1	CDTOGGLE	0	Setting this bit allows the internally determined value of CDTOGGLE to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. This flag is set whenever the debounced CHG Detector signal differs from the previous debounced value. 0 = The CDTOGGLE signal is not included in Alarm Status() 1 = The CDTOGGLE signal is included in Alarm Status()
0	POR	0	Setting this bit allows the corresponding bit in Alarm Raw Status() to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. 0 = This bit in Alarm Raw Status() is not included in Alarm Status() 1 = This bit in Alarm Raw Status() is included in Alarm Status()

10.1.1.9 Settings:Configuration:FET Options

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Configuration	FET Options	H1	0x00	0xFF	0x18	Hex

7	6	5	4	3	2	1	0

CHGDETEN	HOST_FETOFF_EN	HOST_FETON_EN	CHGOFF	SFET	FET_EN	RSVD0	PROTRCVR

Description: This bit field includes settings related to the FET driver operation

Table 10-8. FET Options Register Field Descriptions

Bit	Field	Default	Description
7	CHGDETEN	0	The CHG Detector block is enabled and provides an output signal to the Alarm logic. 0 = CHG Detector block is disabled 1 = CHG Detector block is enabled
6	HOST_FETOFF_EN	0	Some systems need the ability to override the device's FET control and force the FETs to turn off through commands. If that functionality is not needed, it can be disabled to prevent commands from turning the FETs off. 0 = Host FET turnoff control commands are ignored 1 = Host FET turnoff control commands are allowed
5	HOST_FETON_EN	0	Some systems need the ability to override the device's FET control and force the FETs to turn on through commands. If that functionality is not needed, it can be disabled to prevent commands from turning the FETs on. 0 = Host FET turn-on control commands are ignored 1 = Host FET turn-on control commands are allowed
4	CHGOFF	1	The CHG FET can be disabled to conserve power while discharge current is low (body diode protection can enable it when discharge current rises). This bit configures whether or not to disable the CHG FET while current is low. 0 = CHG FET is turned off when current is low. 1 = CHG FET can remain enabled with current is low.
3	SFET	1	The device supports both series and parallel FET configurations. When the CHG and DSG FETs are in series, current can flow through the body diode of one of the FETs when the other is enabled. In this configuration, body diode protection is used to turn the FET on when current above a threshold is detected to be flowing through that FET. When the system has separate DSG and CHG paths and parallel FETs, body diode protection is not needed and can be disabled. 0 = Parallel FET mode: Body diode protection is disabled 1 = Series FET mode: Body diode protection is enabled
2	FET_EN	0	This is the default value of the bit which enables or disables device autonomous control of the FET drivers. If autonomous FET control is disabled, the device is in FET Test mode, in which the FET states are entirely controlled by the FET Control command. This is typically used during manufacturing to test FET circuitry or manual host control. Note that the FETs can still be enabled for body diode protection in FET Test mode. This bit is loaded into the active state upon exit of CONFIG_UPDATE mode. The active state in use is provided by BatteryStatus([FET_EN]) and can be toggled during operation using the FET_ENABLE() subcommand. 0 = Autonomous FET control is disabled by default upon exit of CONFIG_UPDATE mode. FET Test mode is enabled. Device does not turn on FETs unless FET Control command instructs it to do so. 1 = Autonomous FET control is enabled by default upon exit of CONFIG_UPDATE mode. FET Test mode is disabled. FET Control commands can still be used, based on the settings of HOST_FETOFF_EN and HOST_FETON_EN.
0	PROTRCVR	0	This bit enables or disables the capability to manually recover faults using the PROT_RECOVERY() subcommand. 0 = PROT_RECOVERY() subcommand cannot be used in SEALED mode. 1 = PROT_RECOVERY() subcommand can be used in SEALED mode.

10.1.1.10 Settings:Configuration:Charge Detector Time

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Configuration	Charge Detector Time	U1	0	255	1	100ms

Description: This value sets the debounce timing used for the Charge Detect signal. The debounce delay is programmable in units of 100 ms, from 0 to 25.5 seconds

10.1.2 Settings:Protection

10.1.2.1 Settings:Protection:Enabled Protections A

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Protection	Enabled Protections A	H1	0x00	0xFF	0xA1	Hex

7	6	5	4	3	2	1	0
COV	CUV	SCD	OCD1	OCD2	OCC	CURLATCH	REGOUT

Description: This bit field enables or disables various protections. Protections that are enabled set their corresponding Safety Status flags when a fault is detected.

Note that Settings:Protection:CHG FET Protections A, Settings:Protection:DSG FET Protections A, and Settings:Protection:Both FET Protections B must be appropriately configured to control the FET action taken when these faults are detected.

Table 10-9. Enabled Protections A Register Field Descriptions

Bit	Field	Default	Description
7	COV	1	Cell Overvoltage Protection 0 = Disabled 1 = Enabled
6	CUV	0	Cell Undervoltage Protection 0 = Disabled 1 = Enabled
5	SCD	1	Short circuit in discharge protection 0 = Disabled 1 = Enabled
4	OCD1	0	Overcurrent in discharge protection 1 0 = Disabled 1 = Enabled
3	OCD2	0	Overcurrent in discharge protection 2 0 = Disabled 1 = Enabled
2	OCC	0	Overcurrent in charge protection 0 = Disabled 1 = Enabled
1	CURLATCH	0	Current latch protection 0 = Disabled 1 = Enabled
0	REGOUT	1	REGOUT safety check 0 = Disabled 1 = Enabled

10.1.2.2 Settings:Protection:Enabled Protections B

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Protection	Enabled Protections B	H1	0x00	0xFF	0x00	Hex

7	6	5	4	3	2	1	0
RSVD0_1	RSVD0_0	OTD	OTC	UTD	UTC	OTINT	RSVD0

Description: This bit field enables or disables various protections. Protections that are enabled set their corresponding Safety Status flags when a fault is detected. Note that Settings:Protection:CHG FET Protections A, Settings:Protection:DSG FET Protections A, and Settings:Protection:Both FET Protections B must be appropriately configured to control the FET action taken when these faults are detected

Table 10-10. Enabled Protections B Register Field Descriptions

Bit	Field	Default	Description
5	OTD	0	Overtemperature in Discharge Protection 0 = Disabled 1 = Enabled
4	OTC	0	Overtemperature in Charge Protection 0 = Disabled 1 = Enabled
3	UTD	0	Undertemperature in Discharge Protection 0 = Disabled 1 = Enabled
2	UTC	0	Undertemperature in Charge Protection 0 = Disabled 1 = Enabled
1	OTINT	0	Internal Overtemperature Protection 0 = Disabled 1 = Enabled

10.1.2.3 Settings:Protection:DSG FET Protections A

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Protection	DSG FET Protections A	H1	0x00	0xFF	0xFF	Hex

7	6	5	4	3	2	1	0
CUV	SCD	OCD1	OCD2	RSVD0	OTD	UTD	OTINT

Description: This bit field configures which protections disable the DSG FET.

Table 10-11. DSG FET Protections A Register Field Descriptions

Bit	Field	Default	Description
7	CUV	1	Cell Undervoltage Protection 0 = DSG FET is not disabled when protection is triggered. 1 = DSG FET is disabled when protection is triggered.
6	SCD	1	Short circuit in discharge protection 0 = DSG FET is not disabled when protection is triggered. 1 = DSG FET is disabled when protection is triggered.
5	OCD1	1	Overcurrent in discharge protection 1 0 = DSG FET is not disabled when protection is triggered. 1 = DSG FET is disabled when protection is triggered.

Table 10-11. DSG FET Protections A Register Field Descriptions (continued)

Bit	Field	Default	Description
4	OCD2	1	Overcurrent in discharge protection 2 0 = DSG FET is not disabled when protection is triggered. 1 = DSG FET is disabled when protection is triggered.
2	OTD	1	Overtemperature in Discharge Protection 0 = DSG FET is not disabled when protection is triggered. 1 = DSG FET is disabled when protection is triggered.
1	UTD	1	Undertemperature in Discharge Protection 0 = DSG FET is not disabled when protection is triggered. 1 = DSG FET is disabled when protection is triggered.
0	OTINT	1	Internal Overtemperature Protection 0 = DSG FET is not disabled when protection is triggered. 1 = DSG FET is disabled when protection is triggered.

10.1.2.4 Settings:Protection:CHG FET Protections A

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Protection	CHG FET Protections A	H1	0x00	0xFF	0xEF	Hex

7	6	5	4	3	2	1	0
COV	SCD	OCC	RSVD0	RSVD0	OTC	UTC	OTINT

Description: This bit field configures which protections disable the CHG FET.

Table 10-12. CHG FET Protections A Register Field Descriptions

Bit	Field	Default	Description
7	COV	1	Cell Overvoltage Protection 0 = CHG FET is not disabled when protection is triggered. 1 = CHG FET is disabled when protection is triggered.
6	SCD	1	Short Circuit in Discharge Protection 0 = CHG FET is not disabled when protection is triggered. 1 = CHG FET is disabled when protection is triggered.
5	OCC	1	Overcurrent in Charge Protection 0 = CHG FET is not disabled when protection is triggered. 1 = CHG FET is disabled when protection is triggered.
2	OTC	1	Overtemperature in Charge Protection 0 = CHG FET is not disabled when protection is triggered. 1 = CHG FET is disabled when protection is triggered.
1	UTC	1	Undertemperature in Charge Protection 0 = CHG FET is not disabled when protection is triggered. 1 = CHG FET is disabled when protection is triggered.
0	OTINT	1	Internal Overtemperature Protection 0 = CHG FET is not disabled when protection is triggered. 1 = CHG FET is disabled when protection is triggered.

10.1.2.5 Settings:Protection:Both FET Protections B

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Protection	Both FET Protections B	H1	0x00	0xFF	0x06	Hex

7	6	5	4	3	2	1	0

RSVD0_4	RSVD0_3	RSVD0_2	RSVD0_1	RSVD0_0	VREF	VSS	REGOUT

Description: This bit field configures which protections disable Both FETs.

Table 10-13. Both FET Protections B Register Field Descriptions

Bit	Field	Default	Description
2	VREF	1	VREF Diagnostic Check 0 = Both FETs are not disabled when protection is triggered. 1 = Both FETs are disabled when protection is triggered.
1	VSS	1	VSS Diagnostic Check 0 = Both FETs are not disabled when protection is triggered. 1 = Both FETs are disabled when protection is triggered.
0	REGOUT	0	REGOUT flag 0 = Both FETs are not disabled when protection is triggered. 1 = Both FETs are disabled when protection is triggered.

10.1.2.6 Settings:Protection:Cell Open Wire Check Time

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Protection	Cell Open Wire Check Time	H1	0x10	0x1F	0x10	Hex

7	6	5	4	3	2	1	0
RSVD0	RSVD0	RSVD0	RSVD1	COWEN	COWTIME_2	COWTIME_1	COWTIME_0

Description: This register sets the timing for the cell open wire checks. Note that if *[COWTIME2:0]* is set to 0x7 while ***Voltage CHECK Time*** = 250 ms, then the actual CHECK interval is extended approximately 50%.

Table 10-14. Cell Open Wire Check Time Register Field Descriptions

Bit	Field	Default	Description
3	COWEN	0	Enable cell open wire checks. 0 = Cell open wire checks are disabled. 1 = Cell open wire checks are enabled.
2–0	COWTIME_2–COWTIME_0	0	In order to detect a broken connection between a cell in the stack and the PCB, the device periodically enables a current from each enabled cell input to VSS. 0 = Current sources are activated once every 8 CHECK intervals. 1 = Current sources are activated once every 4 CHECK intervals. 2 = Current sources are activated once every 2 CHECK intervals. 3 = Current sources are activated once every CHECK interval. 4 = Current sources are activated twice every CHECK interval. 5 = Current sources are activated 4 times every CHECK interval. 6 = Current sources are activated 8 times every CHECK interval. 7 = Current sources are activated 16 times every CHECK interval.

10.2 Protections

10.2.1 Protections:Cell Voltage

10.2.1.1 Protections:Cell Voltage:Cell Undervoltage Protection Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Cell Voltage	Cell Undervoltage Protection Threshold	I2	0	5500	2500	mV

Description: This parameter sets the Cell Undervoltage Protection threshold in units of mV.

Minimum value = 0 (setting for 0 V)

Maximum value = 5500 (setting for 5.5 V)

10.2.1.2 Protections:Cell Voltage:Cell Undervoltage Protection Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Cell Voltage	Cell Undervoltage Protection Delay	U1	0	255	10	CHECK intervals

Description: This parameter sets the Cell Undervoltage Protection delay. Units are the number of CHECK intervals and can range from 1 to 255

10.2.1.3 Protections:Cell Voltage:Cell Undervoltage Protection Recovery Hysteresis

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Cell Voltage	Cell Undervoltage Protection Recovery Hysteresis	H1	0x00	0x03	0x02	Hex

7	6	5	4	3	2	1	0
RSVD0_5	RSVD0_4	RSVD0_3	RSVD0_2	RSVD0_1	RSVD0_0	CUVRCVR_1	CUVRCVR_0

Description: This parameter sets the Cell Undervoltage Protection recovery hysteresis threshold. The minimum cell voltage must be greater than or equal to the CUV threshold plus this hysteresis to recover from a CUV condition

Table 10-15. Cell Undervoltage Protection Recovery Hysteresis Register Field Descriptions

Bit	Field	Default	Description
1–0	CUVRCVR_1–CUVRCVR_0	2	This parameter sets the Cell Undervoltage Protection recovery hysteresis threshold. The minimum cell voltage must be greater than or equal to the CUV threshold plus this hysteresis to recover from a CUV condition. 0 = no autonomous recovery 1 = 50mV 2 = 100mV 3 = 200mV

10.2.1.4 Protections:Cell Voltage:Cell Overvoltage Protection Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Cell Voltage	Cell Overvoltage Protection Threshold	I2	0	5500	4200	mV

Description: This parameter sets the Cell Overvoltage Protection threshold in units of mV.

Minimum value = 0 (setting for 0 V)

Maximum value = 5500 (setting for 5.5 V)

10.2.1.5 Protections:Cell Voltage:Cell Overvoltage Protection Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Cell Voltage	Cell Overvoltage Protection Delay	U1	0	255	10	CHECK intervals

Description: This parameter sets the Cell Overvoltage Protection delay. Units are the number of CHECK intervals and can range from 1 to 255.

10.2.1.6 Protections:Cell Voltage:Cell Overvoltage Protection Recovery Hysteresis

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Cell Voltage	Cell Overvoltage Protection Recovery Hysteresis	H1	0x00	0x03	0x02	Hex

7	6	5	4	3	2	1	0
RSVD0_5	RSVD0_4	RSVD0_3	RSVD0_2	RSVD0_1	RSVD0_0	COVRCVR_1	COVRCVR_0

Description: This parameter sets the Cell Overvoltage Protection recovery hysteresis threshold. The maximum cell voltage must be less than or equal to the COV threshold minus this hysteresis to recover from a COV condition

Table 10-16. Cell Overvoltage Protection Recovery Hysteresis Register Field Descriptions

Bit	Field	Default	Description
1–0	COVRCVR_1–COVRCVR_0	2	This parameter sets the Cell Overvoltage Protection recovery hysteresis threshold. The maximum cell voltage must be less than or equal to the COV threshold minus this hysteresis to recover from a COV condition. 0 = no autonomous recovery 1 = 50mV 2 = 100mV 3 = 200mV

10.2.2 Protections:Current

10.2.2.1 Protections:Current:Overcurrent in Charge Protection Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Current	Overcurrent in Charge Protection Threshold	U1	2	62	2	2 mV

Description: This parameter sets the Overcurrent in Charge Protection threshold in units of 2 mV, with an offset of -1 mV.

Minimum value = 2 (setting for 3 mV)

Maximum value = 62 (setting for 123 mV)

10.2.2.2 Protections:Current:Overcurrent in Charge Protection Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Current	Overcurrent in Charge Protection Delay	U1	0	255	58	Varying

Description: This parameter sets the Overcurrent in Charge Protection delay.

0x00 = Fastest delay (approximately 0.46 ms)

0x01 - 0x40 = 1.22 ms to 20.435 ms in steps of 0.305 ms

0x41 - 0x80 = 22.875 ms to 176.595 ms in steps of 2.44 ms

0x81 - 0xC0 = 181.475 ms to 488.915 ms in steps of 4.88 ms

0xC1 - 0xFF = 498.675 ms to 1103.795 ms in steps of 9.77 ms

10.2.2.3 Protections:Current:Overcurrent in Discharge 1 Protection Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Current	Overcurrent in Discharge 1 Protection Threshold	U1	2	100	4	2mV

Description: This parameter sets the Overcurrent in Discharge 1 Protection threshold in units of 2mV.

Minimum value = 2 (setting for 4 mV)

Maximum value = 100 (setting for 200 mV)

10.2.2.4 Protections:Current:Overcurrent in Discharge 1 Protection Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Current	Overcurrent in Discharge 1 Protection Delay	U1	0	255	6	Varying

Description: This parameter sets the Overcurrent in Discharge 1 Protection delay.

0x00 = Fastest delay (approximately 0.46 ms)

0x01 - 0x40 = 1.22 ms to 20.435 ms in steps of 0.305 ms

0x41 - 0x80 = 22.875 ms to 176.595 ms in steps of 2.44 ms

0x81 - 0xC0 = 181.475 ms to 488.915 ms in steps of 4.88 ms

0xC1 - 0xFF = 498.675 ms to 1103.795 ms in steps of 9.77 ms

10.2.2.5 Protections:Current:Overcurrent in Discharge 2 Protection Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Current	Overcurrent in Discharge 2 Protection Threshold	U1	2	100	3	2mV

Description: This parameter sets the Overcurrent in Discharge 2 Protection threshold in units of 2mV.

Minimum value = 2 (setting for 4 mV)

Maximum value = 100 (setting for 200 mV)

10.2.2.6 Protections:Current:Overcurrent in Discharge 2 Protection Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Current	Overcurrent in Discharge 2 Protection Delay	U1	0	255	19	Varying

Description: This parameter sets the Overcurrent in Discharge 2 Protection delay.

0x00 = Fastest delay (approximately 0.46 ms)

0x01 - 0x40 = 1.22 ms to 20.435 ms in steps of 0.305 ms

0x41 - 0x80 = 22.875 ms to 176.595 ms in steps of 2.44 ms

0x81 - 0xC0 = 181.475 ms to 488.915 ms in steps of 4.88 ms

0xC1 - 0xFF = 498.675 ms to 1103.795 ms in steps of 9.77 ms

10.2.2.7 Protections:Current:Short Circuit in Discharge Protection Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Current	Short Circuit in Discharge Protection Threshold	H1	0x00	0xFF	0x0	Varying

7	6	5	4	3	2	1	0
RSVD0_3	RSVD0_2	RSVD0_1	RSVD0_0	SCDTHR_3	SCDTHR_2	SCDTHR_1	SCDTHR_0

Description: This parameter sets the Short Circuit in Discharge Protection threshold for the sense resistor voltage

Table 10-17. Short Circuit in Discharge Protection Threshold Register Field Descriptions

Bit	Field	Default	Description
3–0	SCDTHR_3–SCDTHR_0	0	This parameter sets the Short Circuit in Discharge Protection threshold for the sense resistor voltage. 0 = 10 mV 1 = 20 mV 2 = 40 mV 3 = 60 mV 4 = 80 mV 5 = 100 mV 6 = 125 mV 7 = 150 mV 8 = 175 mV 9 = 200 mV 10 = 250 mV 11 = 300 mV 12 = 350 mV 13 = 400 mV 14 = 450 mV 15 = 500 mV

10.2.2.8 Protections:Current:Short Circuit in Discharge Protection Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Current	Short Circuit in Discharge Protection Delay	H1	0x00	0x0A	0x01	Varying

7	6	5	4	3	2	1	0
RSVD0_3	RSVD0_2	RSVD0_1	RSVD0_0	SCDDLY_3	SCDDLY_2	SCDDLY_1	SCDDLY_0

Description: This parameter sets the Short Circuit in Discharge Protection delay

Table 10-18. Short Circuit in Discharge Protection Delay Register Field Descriptions

Bit	Field	Default	Description
3–0	SCDDLY_3–SCDDLY_0	1	This parameter sets the delay before the fault is triggered. 0 = Fastest 1 = 15 µs 2 = 31 µs 3 = 61 µs 4 = 122 µs 5 = 244 µs 6 = 488 µs 7 = 977 µs 8 = 1953 µs 9 = 3906 µs 10 = 7797 µs

10.2.2.9 Protections:Current:Latch Limit

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Current	Latch Limit	H1	0x00	0x07	0x0	Varying

7	6	5	4	3	2	1	0
RSVD0_4	RSVD0_3	RSVD0_2	RSVD0_1	RSVD0_0	CURRLAT_2	CURRLAT_1	CURRLAT_0

Description: This parameter configures the number of retries for recovery of the SCD, OCD1, OCD2, or OCC before the FETs are latched as disabled.

Table 10-19. Latch Limit Register Field Descriptions

Bit	Field	Default	Description
2–0	CURRLAT_2–CURRLAT_0	0	This parameter configures the number of retries for recovery of the SCD, OCD1, OCD2, or OCC before the FETs are latched as disabled. If the protection does not retrigger within 5 seconds after a recovery, the counter is reset to 0. 0 = Latching is disabled 1 = 2 retries before FETs are latched disabled 2 = 4 retries before FETs are latched disabled 3 = 8 retries before FETs are latched disabled 4 = 16 retries before FETs are latched disabled 5 = 32 retries before FETs are latched disabled 6 = 48 retries before FETs are latched disabled 7 = 96 retries before FETs are latched disabled

10.2.2.10 Protections:Current:Recovery Time

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Current	Recovery Time	U1	0	255	5	Seconds

Description: This parameter configures the delay after which current protections recover.

Programmable from 1 second to 255 seconds in 1-second steps.

0x0 = Disable auto recovery

10.2.3 Protections:Temperature

10.2.3.1 Protections:Temperature:Overtemperature in Charge Protection Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Temperature	Overtemperature in Charge Protection Threshold	U1	0	255	55	V_{REG18} / 359

Description: This parameter configures the threshold for the Overtemperature in Charge Protection. The protection is triggered when the TS pin voltage is detected below this threshold.

This sets the threshold detected at the TS pin from 0 to 255 in units of V_{REG18} / 359.

10.2.3.2 Protections:Temperature:Overtemperature in Charge Protection Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Temperature	Overtemperature in Charge Protection Delay	U1	0	255	15	CHECK Intervals

Description: This parameter configures the delay for the Overtemperature in Charge Protection in units of numbers of CHECK intervals.

The settings are from 0 (fastest) to 255 CHECK intervals.

10.2.3.3 Protections:Temperature:Overtemperature in Charge Protection Recovery

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Temperature	Overtemperature in Charge Protection Recovery	U1	0	255	63	V_{REG18} / 359

Description: This parameter configures the recovery threshold for the Overtemperature in Charge Protection. The protection recovers when the TS pin voltage is detected above this threshold.

This sets the threshold detected at the TS pin from 0 to 255 in units of V_{REG18} / 359.

10.2.3.4 Protections:Temperature:Undertemperature in Charge Protection Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Temperature	Undertemperature in Charge Protection Threshold	U1	0	255	147	V_{REG18} / 252

Description: This parameter configures the threshold for the Undertemperature in Charge Protection. The protection is triggered when the TS pin voltage is detected above this threshold.

This sets the threshold detected at the TS pin from 0 to 255 in units of V_{REG18} / 252.

10.2.3.5 Protections:Temperature:Undertemperature in Charge Protection Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Temperature	Undertemperature in Charge Protection Delay	U1	0	255	15	CHECK intervals

Description: This parameter configures the delay for the Undertemperature in Charge Protection in units of numbers of CHECK intervals.

The settings are from 0 (fastest) to 255 CHECK intervals.

10.2.3.6 Protections:Temperature:Undertemperature in Charge Protection Recovery

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Temperature	Undertemperature in Charge Protection Recovery	U1	0	255	134	V_{REG18} / 252

Description: This parameter configures the recovery threshold for the Undertemperature in Charge Protection. The protection recovers when the TS pin voltage falls below this threshold.

This sets the threshold detected at the TS pin from 0 to 255 in units of V_{REG18} / 252.

10.2.3.7 Protections:Temperature:Overtemperature in Discharge Protection Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Temperature	Overtemperature in Discharge Protection Threshold	U1	0	255	48	V_{REG18} / 359

Description: This parameter configures the threshold for the Overtemperature in Discharge Protection. The protection is triggered when the TS pin voltage is detected below this threshold.

This sets the threshold detected at the TS pin from 0 to 255 in units of V_{REG18} / 359.

10.2.3.8 Protections:Temperature:Overtemperature in Discharge Protection Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Temperature	Overtemperature in Discharge Protection Delay	U1	0	255	15	CHECK intervals

Description: This parameter configures the delay for the Overtemperature in Discharge Protection in units of numbers of CHECK intervals.

The settings are from 0 (fastest) to 255 CHECK intervals.

10.2.3.9 Protections:Temperature:Overtemperature in Discharge Protection Recovery

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Temperature	Overtemperature in Discharge Protection Recovery	U1	0	255	55	V_{REG18} / 359

Description: This parameter configures the recovery threshold for the Overtemperature in Discharge Protection. The protection recovers when the TS pin voltage is detected above this threshold.

This sets the threshold detected at the TS pin from 0 to 255 in units of V_{REG18} / 359.

10.2.3.10 Protections:Temperature:Undertemperature in Discharge Protection Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Temperature	Undertemperature in Discharge Protection Threshold	U1	0	255	147	V_{REG18} / 252

Description: This parameter configures the threshold for the Undertemperature in Discharge Protection. The protection is triggered when the TS pin voltage is detected above this threshold.

This sets the threshold detected at the TS pin from 0 to 255 in units of V_{REG18} / 252.

10.2.3.11 Protections:Temperature:Undertemperature in Discharge Protection Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Temperature	Undertemperature in Discharge Protection Delay	U1	0	255	15	CHECK intervals

Description: This parameter configures the delay for the Undertemperature in Discharge Protection in units of numbers of CHECK intervals.

The settings are from 0 (fastest) to 255 CHECK intervals.

10.2.3.12 Protections:Temperature:Undertemperature in Discharge Protection Recovery

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Temperature	Undertemperature in Discharge Protection Recovery	U1	0	255	134	V_{REG18} / 252

Description: This parameter configures the recovery threshold for the Undertemperature in Discharge Protection. The protection recovers when the TS pin voltage falls below this threshold.

This sets the threshold detected at the TS pin from 0 to 255 in units of V_{REG18} / 252.

10.2.3.13 Protections:Temperature:Internal Overtemperature Protection Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Temperature	Internal Overtemperature Protection Threshold	U1	25	150	105	°C

Description: This parameter configures the threshold for the Internal Overtemperature Protection.

The settings set the temperature threshold from 25°C to 150°C in 1°C steps.

10.2.3.14 Protections:Temperature:Internal Overtemperature Protection Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Temperature	Internal Overtemperature Protection Delay	U1	0	255	15	CHECK intervals

Description: This parameter configures the delay for the Internal Overtemperature Protection in units of numbers of CHECK intervals.

The settings are from 0 (fastest) to 255 CHECK intervals.

10.2.3.15 Protections:Temperature:Internal Overtemperature Protection Recovery

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Temperature	Internal Overtemperature Protection Recovery	U1	25	150	100	°C

Description: This parameter configures the recovery threshold for the Internal Overtemperature Protection.

The settings set the temperature recovery threshold from 25°C to 150°C in 1°C steps.

10.3 Power

10.3.1 Power:Configuration

10.3.1.1 Power:Configuration:Voltage CHECK Time

Class	Subclass	Name	Type	Min	Max	Default	Unit
Power	Configuration	Voltage CHECK Time	U1	0	255	5	Seconds

Description: This parameter sets how often the device checks voltages and temperatures while in NORMAL mode.

Units in seconds (unsigned), except a setting of 0 results in checks every 250 ms.

10.3.1.2 Power:Configuration:Body Diode Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Power	Configuration	Body Diode Threshold	U1	1	10	1	500 µV

Description: This register sets the threshold at which the device enables the FET driver to protect the body diode.

To minimize power dissipation in the FET body diode, the FET is turned on when reverse current is detected and the other FET is on. Current is detected by comparing the sense resistor voltage to the voltage threshold.

When discharge current is detected greater in magnitude than ***Power:Configuration:Body Diode Threshold*** and the DSG FET is on, the CHG FET is turned on.

When charge current is detected greater than ***Power:Configuration:Body Diode Threshold*** and the CHG FET is on, the DSG FET is turned on.

When in parallel FET mode (***Settings:FET:FET Options[SFET] = 0***), body diode protection is disabled and a FET is not turned on in response to reverse current.

Threshold = 500 µV × (setting)

Note

The minimum setting is 1 (500 µV), meaning 500 mA across 1 mΩ. The maximum setting is 10 (5 mV).

10.3.2 Power:Shutdown

10.3.2.1 Power:Shutdown:Shutdown Cell Voltage

Class	Subclass	Name	Type	Min	Max	Default	Unit
Power	Shutdown	Shutdown Cell Voltage	I2	0	5500	0x0	mV

Description: Configures the cell voltage threshold at which the device enters SHUTDOWN mode after a 10-second delay. This threshold does not apply to VC pins not configured for use with actual cells.

0 = Cell-Voltage-based shutdown disabled

All other values = Cell voltage shutdown threshold in mV (signed)

10.3.2.2 Power:Shutdown:Shutdown Stack Voltage

Class	Subclass	Name	Type	Min	Max	Default	Unit
Power	Shutdown	Shutdown Stack Voltage	U2	0	65535	0x0	mV

Description: Configures the stack voltage threshold at which the device enters SHUTDOWN mode after a 10-second delay.

0 = Top-of-Stack-Voltage-based shutdown disabled

All other values = Top-of-stack voltage shutdown threshold in mV (unsigned)

10.3.2.3 Power:Shutdown:Shutdown Temperature

Class	Subclass	Name	Type	Min	Max	Default	Unit
Power	Shutdown	Shutdown Temperature	U1	0	150	0x0	°C

Description: Configures the internal temperature threshold at which the device shuts down.

0 = Shutdown based on internal temperature disabled

All other values = Shutdown Internal Temperature threshold in °C (unsigned)

10.4 Security

10.4.1 Security:Settings

10.4.1.1 Security:Settings:Security Settings

Class	Subclass	Name	Type	Min	Max	Default	Unit
Security	Settings	Security Settings	H1	0x00	0x07	0x0	Hex

7	6	5	4	3	2	1	0
RSVD0_4	RSVD0_3	RSVD0_2	RSVD0_1	RSVD0_0	SEAL	LOCK_CFG	PERM_SEAL

Description: These bits configure the security settings of the device

Table 10-20. Security Settings Register Field Descriptions

Bit	Field	Default	Description
2	SEAL	0	Setting this bit causes the device to enter SEALED mode when reset (if saved in OTP) or exiting CONFIG_UPDATE mode. In production systems, set this bit for security purposes. 0 = Device does not default to SEALED mode. 1 = Device default state is SEALED.
1	LOCK_CFG	0	Setting this bit prevents entry into CONFIG_UPDATE mode. This prevents further modifications to the device configuration after CONFIG_UPDATE mode is exited. 0 = Configuration parameters can be changed in CONFIG_UPDATE mode. 1 = Configuration parameters cannot be changed, CONFIG_UPDATE mode cannot be entered.
0	PERM_SEAL	0	Setting this bit prevents unsealing the device once it is sealed. If this is not programmed to OTP, this setting is lost on a full reset and the device is again able to unseal. 0 = The device can be unsealed by sending the correct security keys. 1 = The device cannot be unsealed.

10.4.1.2 Security:Settings:Full Access Key Step 1

Class	Subclass	Name	Type	Min	Max	Default	Unit
Security	Settings	Full Access Key Step 1	H2	0x0000	0xFFFF	0x0414	Hex

15	14	13	12	11	10	9	8
FAKEY_15	FAKEY_14	FAKEY_13	FAKEY_12	FAKEY_11	FAKEY_10	FAKEY_9	FAKEY_8
7	6	5	4	3	2	1	0
FAKEY_7	FAKEY_6	FAKEY_5	FAKEY_4	FAKEY_3	FAKEY_2	FAKEY_1	FAKEY_0

Description:

This is the first word of the security key that must be sent to transition from SEALED to FULLACCESS mode. Do not choose a word that is identical to a subcommand address

Table 10-21. Full Access Key Step 1 Register Field Descriptions

Bit	Field	Default	Description
15–0	FAKEY_15–FAKEY_0	1044	

10.4.1.3 Security:Settings:Full Access Key Step 2

Class	Subclass	Name	Type	Min	Max	Default	Unit
Security	Settings	Full Access Key Step 2	H2	0x0000	0xFFFF	0x3672	Hex

15	14	13	12	11	10	9	8
FAKEY_15	FAKEY_14	FAKEY_13	FAKEY_12	FAKEY_11	FAKEY_10	FAKEY_9	FAKEY_8
7	6	5	4	3	2	1	0
FAKEY_7	FAKEY_6	FAKEY_5	FAKEY_4	FAKEY_3	FAKEY_2	FAKEY_1	FAKEY_0

Description:

This is the second word of the security key that must be sent to transition from SEALED to FULLACCESS mode. Do not choose a word that is identical to a subcommand address or the same as the first word.

It must be sent within 5 seconds of the first word of the key and with no other commands in between.

Table 10-22. Full Access Key Step 2 Register Field Descriptions

Bit	Field	Default	Description
15–0	FAKEY_15–FAKEY_0	13938	

10.4.2 Data Memory Summary

Data Memory Table

Class	Subclass	Address	Name	Type	Min Value	Max Value	Default	Units
Settings	Configuration	0x9000	Reserved	—	—	—	—	—
Settings	Configuration	0x9014	Power Config	H1	0x00	0xFF	0x01	Hex
Settings	Configuration	0x9015	REGOUT Config	H1	0x00	0xFF	0x08	Hex
Settings	Configuration	0x9016	I2C Address	H1	0x00	0x7F	0x08	Hex
Settings	Configuration	0x9017	I2C Config	H2	0x0000	0xFFFF	0x3400	Hex
Settings	Configuration	0x901A	TS Mode	H1	0x0000	0x0001	0x0000	Hex
Settings	Configuration	0x901B	Vcell Mode	H1	0x00	0x07	0x0	Hex
Settings	Configuration	0x901C	Default Alarm Mask	H2	0x0000	0xFFFF	0xC200	Hex
Settings	Configuration	0x901E	FET Options	H1	0x00	0xFF	0x18	Hex
Settings	Configuration	0x901F	Charge Detector Time	U1	0	255	1	100ms
Settings	Protection	0x9024	Enabled Protections A	H1	0x00	0xFF	0xA1	Hex
Settings	Protection	0x9025	Enabled Protections B	H1	0x00	0xFF	0x00	Hex
Settings	Protection	0x9026	DSG FET Protections A	H1	0x00	0xFF	0xFF	Hex
Settings	Protection	0x9027	CHG FET Protections A	H1	0x00	0xFF	0xEF	Hex
Settings	Protection	0x9028	Both FET Protections B	H1	0x00	0xFF	0x06	Hex
Settings	Protection	0x902C	Cell Open Wire Check Time	H1	0x10	0x1F	0x10	Hex
Protections	Cell Voltage	0x902E	Cell Undervoltage Protection Threshold	I2	0	5500	2500	mV
Protections	Cell Voltage	0x9030	Cell Undervoltage Protection Delay	U1	0	255	10	ADSCAN intervals
Protections	Cell Voltage	0x9031	Cell Undervoltage Protection Recovery Hysteresis	H1	0x00	0x03	0x02	Hex
Protections	Cell Voltage	0x9032	Cell Overvoltage Protection Threshold	I2	0	5500	4200	mV
Protections	Cell Voltage	0x9034	Cell Overvoltage Protection Delay	U1	0	255	10	ADSCAN intervals
Protections	Cell Voltage	0x9035	Cell Overvoltage Protection Recovery Hysteresis	H1	0x00	0x03	0x02	Hex
Protections	Current	0x9036	Overcurrent in Charge Protection Threshold	U1	2	62	2	2mV
Protections	Current	0x9037	Overcurrent in Charge Protection Delay	U1	0	255	58	Varying
Protections	Current	0x9038	Overcurrent in Discharge 1 Protection Threshold	U1	2	100	4	2mV
Protections	Current	0x9039	Overcurrent in Discharge 1 Protection Delay	U1	0	255	6	Varying
Protections	Current	0x903A	Overcurrent in Discharge 2 Protection Threshold	U1	2	100	3	2mV
Protections	Current	0x903B	Overcurrent in Discharge 2 Protection Delay	U1	0	255	19	Varying
Protections	Current	0x903C	Short Circuit in Discharge Protection Threshold	H1	0x00	0xFF	0x0	Varying
Protections	Current	0x903D	Short Circuit in Discharge Protection Delay	H1	0x00	0x0A	0x01	Varying
Protections	Current	0x903E	Latch Limit	H1	0x00	0x07	0x0	Varying
Protections	Current	0x903F	Recovery Time	U1	0	255	5	Seconds

Class	Subclass	Address	Name	Type	Min Value	Max Value	Default	Units
Protections	Temperature	0x9040	Overtemperature in Charge Protection Threshold	U1	0	255	55	V_{REG18}/359
Protections	Temperature	0x9041	Overtemperature in Charge Protection Delay	U1	0	255	15	CHECK intervals
Protections	Temperature	0x9042	Overtemperature in Charge Protection Recovery	U1	0	255	63	V_{REG18}/359
Protections	Temperature	0x9043	Undertemperature in Charge Protection Threshold	U1	0	255	147	V_{REG18}/252
Protections	Temperature	0x9044	Undertemperature in Charge Protection Delay	U1	0	255	15	CHECK intervals
Protections	Temperature	0x9045	Undertemperature in Charge Protection Recovery	U1	0	255	134	V_{REG18}/252
Protections	Temperature	0x9046	Overtemperature in Discharge Protection Threshold	U1	0	255	48	V_{REG18}/359
Protections	Temperature	0x9047	Overtemperature in Discharge Protection Delay	U1	0	255	15	CHECK intervals
Protections	Temperature	0x9048	Overtemperature in Discharge Protection Recovery	U1	0	255	55	V_{REG18}/359
Protections	Temperature	0x9049	Undertemperature in Discharge Protection Threshold	U1	0	255	147	V_{REG18}/252
Protections	Temperature	0x904A	Undertemperature in Discharge Protection Delay	U1	0	255	15	CHECK intervals
Protections	Temperature	0x904B	Undertemperature in Discharge Protection Recovery	U1	0	255	134	V_{REG18}/252
Protections	Temperature	0x904C	Internal Overtemperature Protection Threshold	U1	25	150	105	°C
Protections	Temperature	0x904D	Internal Overtemperature Protection Delay	U1	0	255	15	CHECK intervals
Protections	Temperature	0x904E	Internal Overtemperature Protection Recovery	U1	25	150	100	°C
Power	Configuration	0x9051	Voltage CHECK Time	U1	0	255	5	Seconds
Power	Configuration	0x9052	Body Diode Threshold	U1	1	10	1	500uV
Power	Shutdown	0x9053	Shutdown Cell Voltage	I2	0	5500	0x0	mV
Power	Shutdown	0x9055	Shutdown Stack Voltage	U2	0	65535	0x0	mV
Power	Shutdown	0x9057	Shutdown Temperature	U1	0	150	0x0	°C
Security	Settings	0x9059	Security Settings	H1	0x00	0x07	0x0	Hex
Security	Settings	0x905A	Full Access Key Step 1	H2	0x0000	0xFFFF	0x0414	Hex
Security	Settings	0x905C	Full Access Key Step 2	H2	0x0000	0xFFFF	0x3672	Hex

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2023	*	Initial Release

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