

**ABSTRACT**

The TPS62866EVM-051 facilitates the evaluation of the TPS62866 6-A, step-down converter with DCS-Control™ in a tiny 1.05-mm by 1.78-mm W CSP package with 0.35-mm pitch. The EVM outputs a 0.9-V output voltage with 1% accuracy from input voltages between 2.4 V and 5.5 V. The TPS62866 is a highly efficient and tiny solution for point-of-load (POL) converters for space-constrained applications, such as artificial intelligence chips, camera modules, solid state drives (SSDs), and optical modules.

**Table of Contents**

|  |   |
|--|---|
| 1 Introduction.....                    | 2 |
| 2 Setup.....                           | 2 |
| 3 TPS62866EVM-051 Test Results.....    | 3 |
| 4 Board Layout.....                    | 3 |
| 5 Schematic and List of Materials..... | 5 |
| 6 Software User Interface.....         | 6 |
| 7 Revision History.....                | 9 |

**List of Figures**

|  |   |
|--|---|
| Figure 4-1. Top Assembly.....                  | 3 |
| Figure 4-2. Top Layer.....                     | 3 |
| Figure 4-3. Signal Layer 1.....                | 3 |
| Figure 4-4. Signal Layer 2.....                | 3 |
| Figure 4-5. Signal Layer 3.....                | 4 |
| Figure 4-6. Signal Layer 4.....                | 4 |
| Figure 4-7. Bottom Layer.....                  | 4 |
| Figure 4-8. TPS62866EVM-051 Angled View.....   | 4 |
| Figure 4-9. TPS62866EVM-051 Overhead View..... | 4 |
| Figure 5-1. TPS62866EVM-051 Schematic.....     | 5 |
| Figure 6-1. Quick Connection Overview.....     | 6 |
| Figure 6-2. GUI Home Screen.....               | 7 |
| Figure 6-3. GUI Settings Screen.....           | 8 |
| Figure 6-4. GUI Register Map Screen.....       | 9 |

**List of Tables**

|   |   |
|---|---|
| Table 1-1. Performance Specification Summary..... | 2 |
| Table 5-1. TPS62866EVM-051 List of Materials..... | 5 |

## 1 Introduction

The TPS62866 is a synchronous, step-down converter in a 1.05- x 1.78- x 0.5-mm wafer chip-scale package (WCSP).

### 1.1 Performance Specification

[Table 1-1](#) provides a summary of the TPS62866EVM-051 performance specifications.

**Table 1-1. Performance Specification Summary**

| SPECIFICATION           | TEST CONDITIONS | MIN | TYP | MAX  | UNIT |
|-------------------------|-----------------|-----|-----|------|------|
| Input voltage           |                 | 2.4 | 5   | 5.5  | V    |
| Output voltage setpoint |                 |     | 0.9 |      | V    |
| Output current          |                 | 0   |     | 6000 | mA   |

## 1.2 Modifications

The EVM can support variance of the whole IC family. Additional input and output capacitors can be added.

## 2 Setup

This section describes how to properly use the TPS62866EVM-051.

### 2.1 Input/Output Connector Descriptions

**J1, Pin 1 and 2 – VIN** Positive input connection from the input supply for the EVM

**J1, Pin 3 and 4 – S+/S-** Input voltage sense connections. Measure the input voltage at this point.

**J1, Pin 5 and 6 – GND** Input return connection from the input supply for the EVM

**J2, Pin 1 and 2 – VOUT** Output voltage connection

**J2, Pin 3 and 4 – S+/S-** Output voltage sense connections. Measure the output voltage at this point.

**J2, Pin 5 and 6 – GND** Output return connection

**J3, Pin 5 – VBUS** The VBUS pin of this header is used to bias the SCL and SDA nodes of I<sup>2</sup>C interface via a resistor.

**J3, Pin 6 – GND** The GND pin of this header is used to connect the grounds of the IC and the I<sup>2</sup>C interface.

**J3, Pin 9 – SCL** The pin of this header should be connected to the SCL of the I<sup>2</sup>C interface.

**J3, Pin 10 – SDA** The pin of this header should be connected to the SDA of the I<sup>2</sup>C interface.

**JP1 – VID/PG** VID/ PG pin jumper. Always place the jumper across VID/ PG and LOW pins before start-up. This sets the output voltage and device address. After startup, VOUT reflects the value set on V<sub>OUT</sub> Register 1 if the jumper is placed across VID/ PG and LOW pins. VOUT follows the value set on V<sub>OUT</sub> Register 2 if the jumper is placed across VID/ PG and HIGH pins.

**JP2 – EN** EN pin input jumper. Place the jumper across ON and EN to turn on the IC. Place the jumper across OFF and EN to turn off the IC.

### 2.2 Setup

To operate the EVM, set jumpers JP1 and JP2 to the desired position per [Section 2.1](#). Connect the input supply to J1 and connect the load to J2.

### 3 TPS62866EVM-051 Test Results

The TPS62866EVM-051 was used to take all the data in the TPS62866 data sheet ([SLVSEI1](#)). See the device data sheet for the performance of this EVM.

### 4 Board Layout

This section provides the TPS62866EVM-051 board layout and illustrations in [Figure 4-1](#) through [Figure 4-7](#). The Gerbers are available on the EVM product page: [TPS62866EVM-051](#)

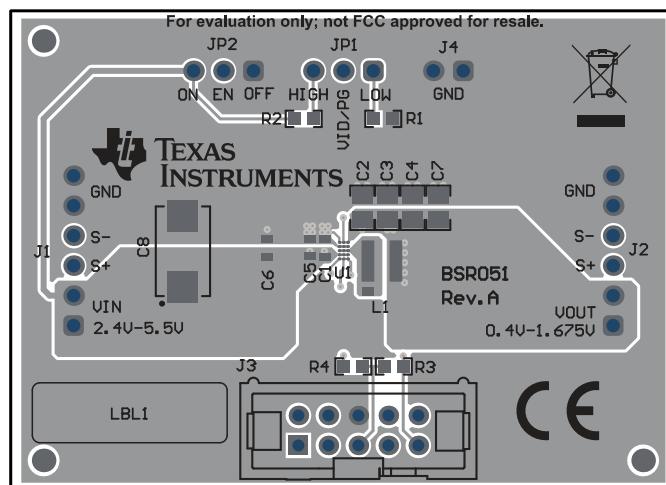


Figure 4-1. Top Assembly

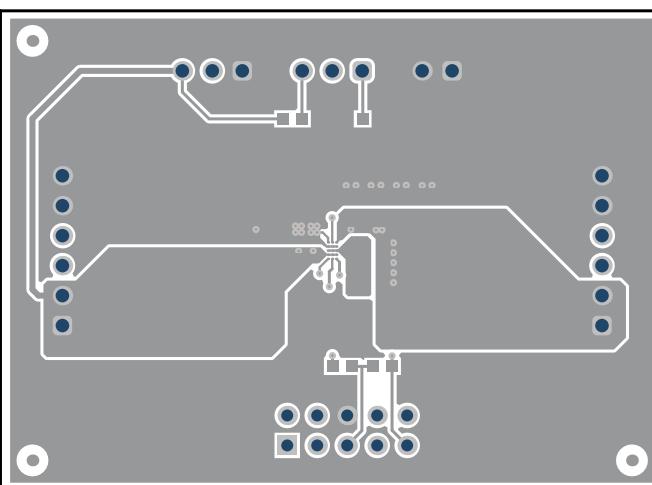


Figure 4-2. Top Layer

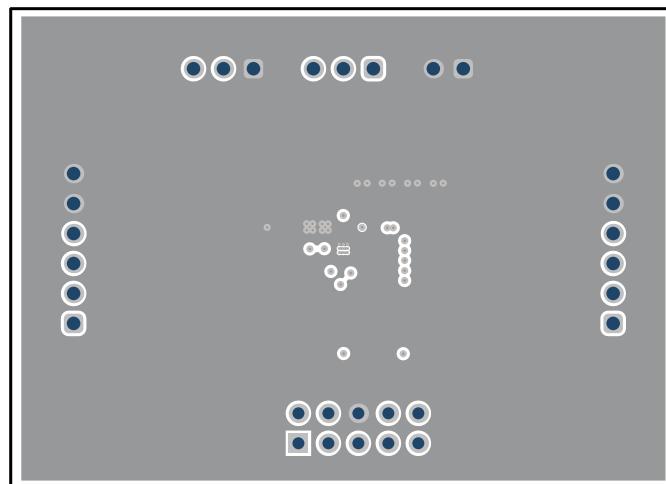


Figure 4-3. Signal Layer 1

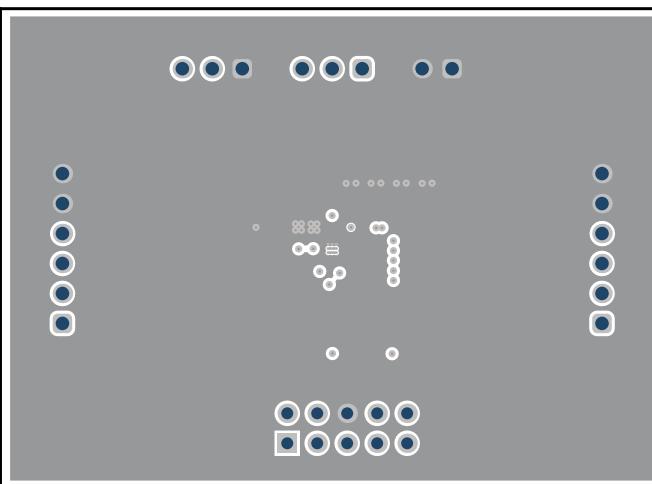


Figure 4-4. Signal Layer 2

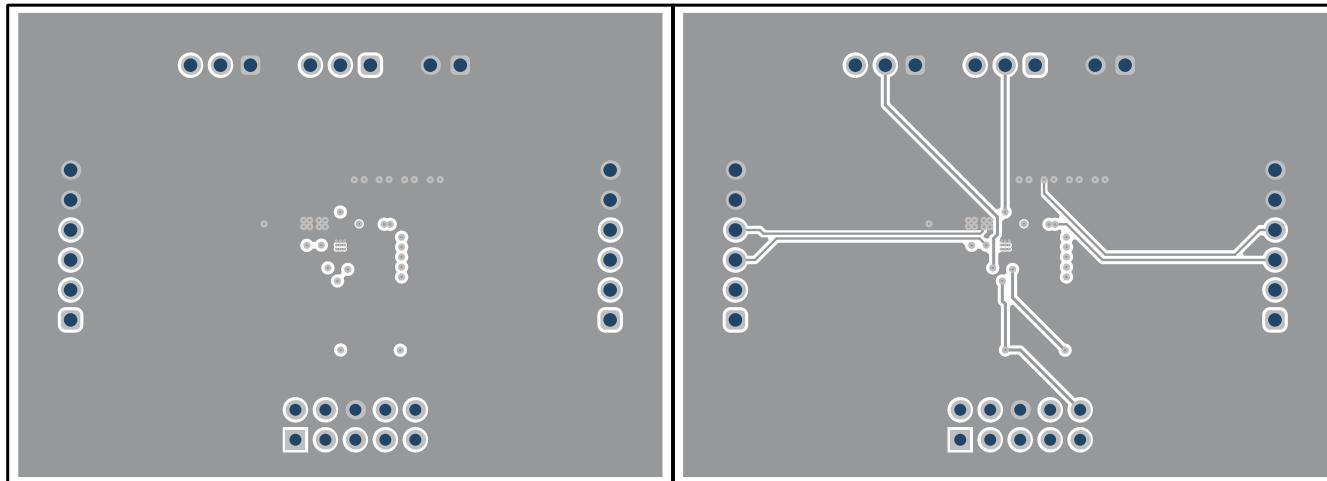


Figure 4-5. Signal Layer 3

Figure 4-6. Signal Layer 4

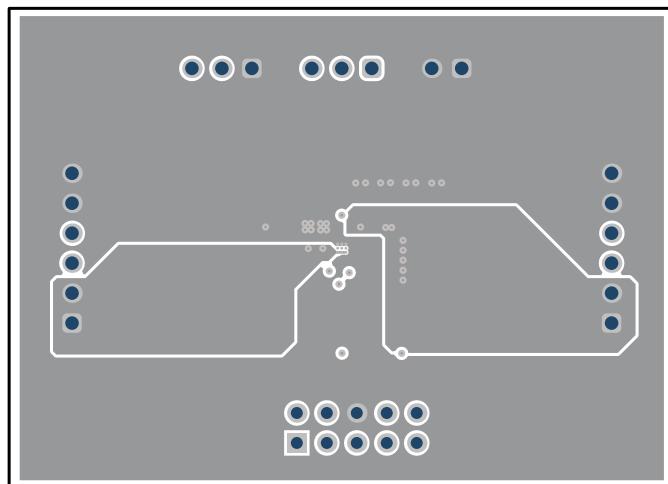


Figure 4-7. Bottom Layer



Figure 4-8. TPS62866EVM-051 Angled View



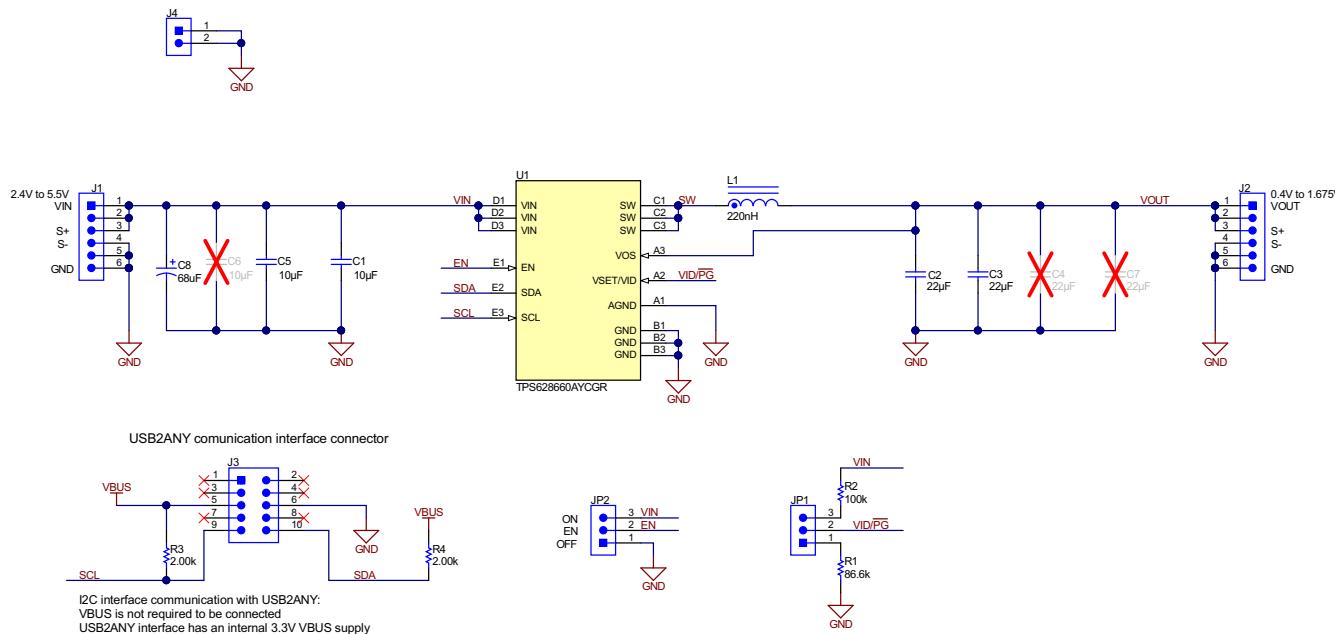
Figure 4-9. TPS62866EVM-051 Overhead View

## 5 Schematic and List of Materials

This section provides the TPS62866EVM-051 schematic and list of materials.

### 5.1 Schematic

Figure 5-1 illustrates the EVM schematic.



**Figure 5-1. TPS62866EVM-051 Schematic**

### 5.2 List of Materials

Table 5-1 lists a list of materials for this EVM.

**Table 5-1. TPS62866EVM-051 List of Materials**

| DESIGNATOR | QTY | DESCRIPTION   | PART NUMBER        | MANUFACTURER              |
|------------|-----|---|--------------------|---------------------------|
| C1, C5     | 2   | Capacitor, ceramic, 10 $\mu$ F, 6.3 V, $\pm 20\%$ , X7R, 0603   | CL10B106MQ8NRNC    | Samsung Electro-Mechanics |
| C2, C3     | 2   | Capacitor, ceramic, 22 $\mu$ F, 6.3 V, $\pm 20\%$ , X7R, 0805   | GRM21BZ70J226ME44L | Murata                    |
| C8         | 1   | Capacitor, tantalum, 68 $\mu$ F, 20 V, $\pm 10\%$ , 7343  | T495D686K020ATE150 | Kemet                     |
| L1         | 1   | Inductor, 220 nH, 16.8 A, 5.8 m $\Omega$ , SMD, 4040  | XAL4020-221MEB     | Coilcraft                 |
| R1         | 1   | Resistor, 86.6 k $\Omega$ , 1%, 0.1 W, 0603   | Std                | Std                       |
| R2         | 1   | Resistor, 100 k $\Omega$ , 1%, 0.1 W, 0603  | Std                | Std                       |
| R3, R4     | 2   | Resistor, 2.0 k $\Omega$ , 1%, 0.1 W, 0603  | Std                | Std                       |
| U1         | 1   | 6-A Step-Down Converter with I <sup>2</sup> C Interface and Wide Output Voltage Range, YCG0015ACAC (DSBGA-15) | TPS628660AYCGT     | Texas Instruments         |

## 6 Software User Interface

### 6.1 Software Setup

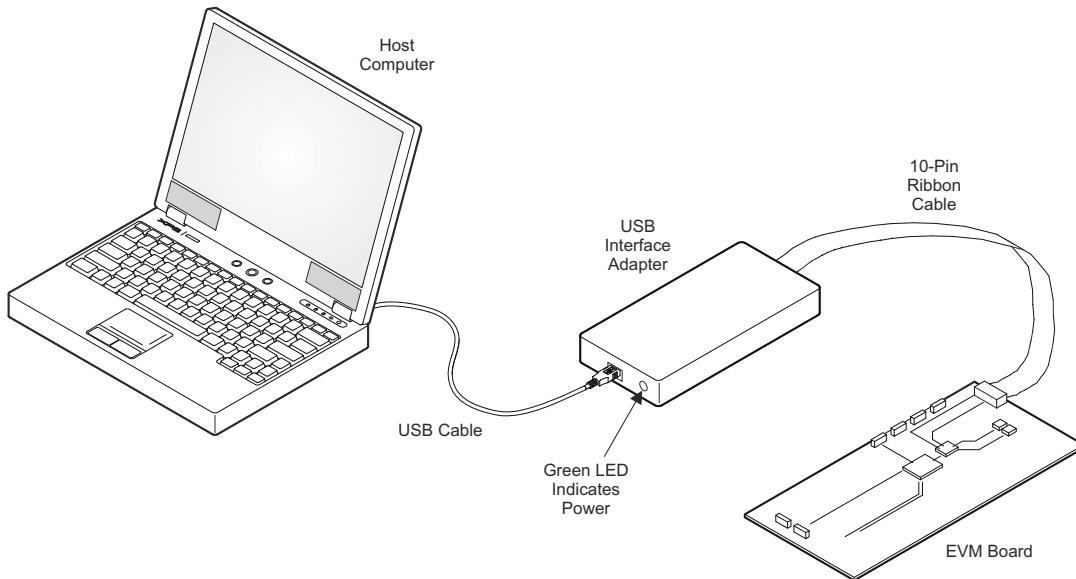
A graphical user interface (GUI) is available from the [TPS62866 design and development page](#), which allows simple and convenient programming of the device through the TI USB2ANY (<https://www.ti.com/tool/USB2ANY>) interface board. Alternatively, you can use any I<sup>2</sup>C-standardized programming tool or I<sup>2</sup>C host to configure the device. Mind the I<sup>2</sup>C pins specification, such as timing parameters and proper pullup resistors, specified in the [TPS62864/6 2.4-V to 5.5-V Input, 4-A and 6-A Synchronous Step-Down Converter with I<sup>2</sup>C Interface in W CSP Package Data Sheet](#).

### 6.2 Interface Hardware Setup

Connect the USB2ANY adapter to the PC using the supplied USB cable. Attach the EVM connector, J3 to the USB2ANY adapter using the supplied 10-pin ribbon cable. The ribbon cable connector is keyed to prevent incorrect installation.

Figure 6-1 shows a quick adapter connection overview.

**USB Interface Adaptor Quick Connection Diagram**



**Figure 6-1. Quick Connection Overview**

## 6.3 User Interface Operation

Upon start-up, the GUI automatically connects to the EVM. If not, then click on the "Connect" button in the lower-left corner of the GUI window. Ensure the I2C Slave Address is correct. The following sections give a short overview of the three main GUI screens.

### 6.3.1 Home Screen

The Home screen provides a short overview of the TPS6286x0 devices. To start evaluating the device, click the **Start** button. Click the **I2C Slave Address** button to change the address, and the default I2C address is 0x40. All the links related to the device are all indicated on the bottom portion of the window.

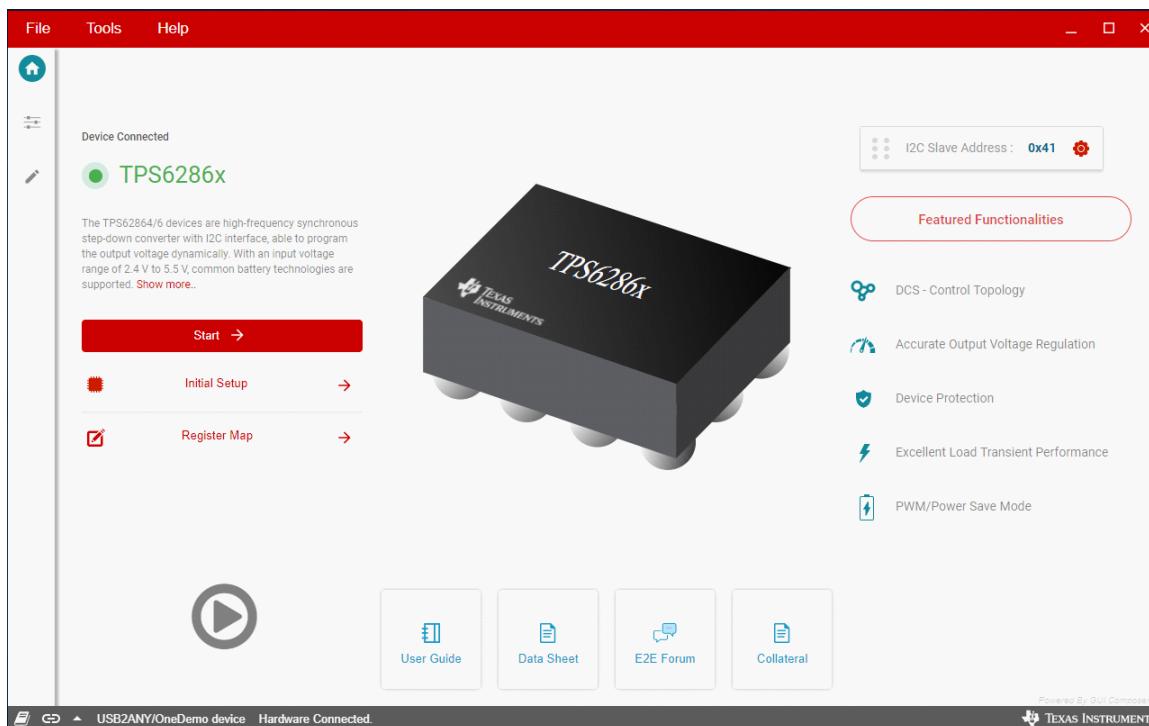
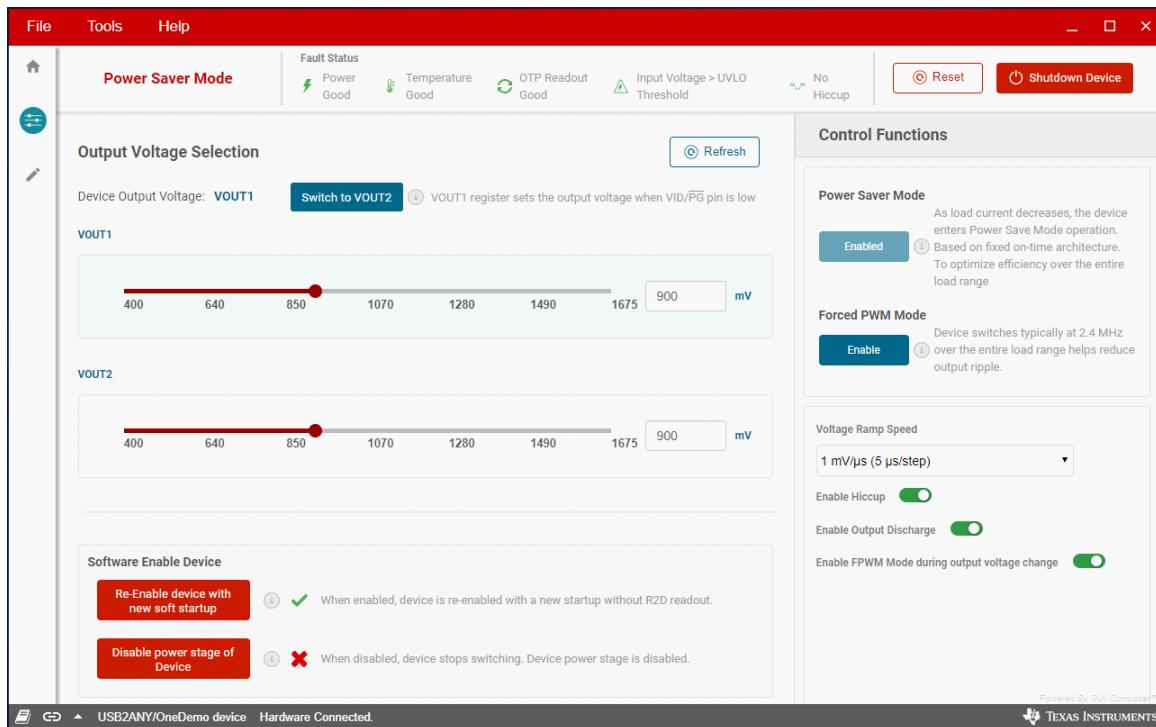


Figure 6-2. GUI Home Screen

### 6.3.2 Settings Screen

The Settings screen provides control over the VOUT and CONTROL Registers. The Status Register is available in this window as well. Real-time updates are possible if the Auto Read function is set to *As fast as possible* in the Register Map page.



**Figure 6-3. GUI Settings Screen**

### 6.3.3 Register Map Screen

The Register Map screen shows bit values of all parameters. In this section, single registers can be read or written to the device (if applicable). Refer to the register map in the [TPS62864/6 2.4-V to 5.5-V Input, 4-A and 6-A Synchronous Step-Down Converter with I<sub>2</sub>C Interface in W CSP Package Data Sheet](#) for a detailed description of the TPS62866 registers.

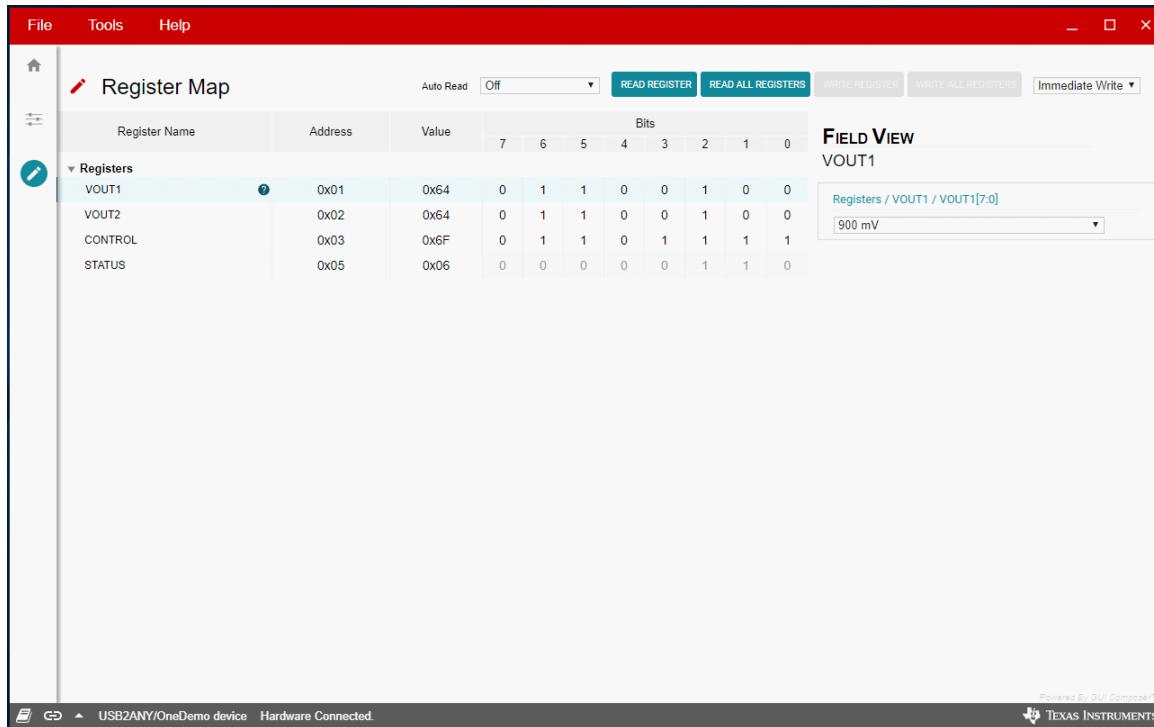


Figure 6-4. GUI Register Map Screen

## 7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

### Changes from Revision \* (July 2019) to Revision A (July 2021)

Page

- Updated the numbering format for tables, figures, and cross-references throughout the document..... 1
- Added *Software User Interface* section..... 6

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