Dual-Channel DCAP+ Multiphase Controller: TPS536C7B1, TPS53676

Technical Reference Manual

Literature Number: SLUUC19
JANUARY 2021

Table of Contents

List of Figures

List of Tables

This page intentionally left blank.

About This Manual

This Technical Reference Manual (TRM) details the integration, the environment, the functional description, and the programming models for each peripheral and subsystem in the device.

Do not consider the TRM a substitute for the datasheet, but rather as a companion guide to supplement the device-specific datasheet to understand the details to program the device. The primary purpose of the TRM is to abstract the programming details of the device from the datasheet. This separation allows the datasheet to outline the high-level features of the device without unnecessary information about register descriptions or programming models.

This document applies to the following TI device numbers: TPS536C7B1 and TPS53676. Unless otherwise mentioned, the information in this document applies to each of those device numbers. *TPS536xx* refers to both device numbers collectively.

Related Documentation From Texas Instruments

For product information, visit the Texas Instruments website at http://www.ti.com.

This page intentionally left blank.

Chapter 1

PMBus Interface

1.1 Overview

1.1.1 PMBus overview

TPS536xx is designed to be compatible with the timing and physical layer electrical characteristics of the Power Management Bus (PMBus) Specification, part I, revision 1.3 available at http://pmbus.org. The 100-kHz, 400-kHz, and 1000-kHz classes are supported. Input logic levels are designed to be compaitible with 1.8-V and 3.3-V logic. PMBus revision 1.3 is derived from the System Managmenet Bus (SMBus) revision 3.0, available at http://smbus.org/. The communication mechanism is based on the inter-integrated circuit I^2C protocol.

A master with clock stretching support is mandatory for communication with TPS536xx through the PMBus interface. TPS536xx does support the packet error check (PEC) protocol. If the system host supplies clock pulses for the PEC byte, PEC is used. If the CLK pulses are not present before a STOP, the PEC is not used. TPS536xx can be configured to require PEC for each transaction in systems which require high reliability of communication.

TPS536xx supports the SMB_ALERT# response protocol. The SMB_ALERT# response protocol is a mechanism by which a slave device can alert the master device that it is available for communication. The master device processes this event and simultaneously accesses all slave devices on the bus (that support the protocol) through the alert response address (ARA). Only the slave device that caused the alert acknowledges this request. The host device performs a modified receive byte operation to ascertain the slave devices address. At this point, the master device can use the PMBus status commands to query the slave device that caused the alert. By default, these devices implement the auto alert response, a manufacturer specific improvement to the SMB_ALERT# response protocol, intended to mitigate the issue of bus hogging. For more information on the SMBus alert response protocol, see the System Management Bus (SMBus) specification.

1.1.2 PMBus transaction types

Support for the following SMBus transaction types is mandatory. The use of PEC is optional.

Note that the SMBus Write Block and Read Block transaction types contain a repeated start condition, which may not be compatible with all I^2C master device IP.

- Write Byte / Read Byte
- Write Word / Read Word
- Write Block / Read Block
- Send Byte / Receive Byte
- Block-Write-Block-Read Process Call (for SMBALERT_MASK commands)

1.1.3 PMBus data formats

TPS536xx supports 3 data formats according to the PMBus specification. The data format for each command is listed along with its address and supported values.

- **ULINEAR16 format** uses a 16-bit unsigned integer. The default LSB size is 2^{-10} = 0.97656 mV
- **SLINEAR16 format** uses a 16-bit number representing a decimal. This number has two fields: the 5 MSB bits form an two's complement *exponent*, referred to as N, and the 11 LSB bits form a two's complement *mantissa*, referred to as M. The decimal number is represented as $D = M \times 2^N$
- **Unsigned binary format** uses direct bit maps with each command being subdivided into multiple fields that can have different meaning.

TPS536xx accepts writes to SLINEAR11 format commands with any desired exponent value. TI recommends using the default exponent listed for each command for writes to ensure consistent NVM store and restore behavior.

Telemetry commands in the SLINEAR11 format return data with variable exponent values according to the absolute value of the retured value. As a rule TPS536xx returns data in the SLINEAR11 format with the smallest possible exponent, to provide the highest possible command resolution. As a result the host must be able to support decoding of the SLINEAR11 format with any exponent value.

1.1.3.1 Example PMBus number format conversions

Example: Decode SLINEAR11 number E804h

E804h = 11101 00000000100b

Exponent = 11101b. N = -3 (5-bit two's complement)

Mantissa = 00000000100b. M = 4 (11-bit two's complement)

The decimal number $D = M \times 2^N = 4 \times 2^{-3} = 0.5$

Example: Encode 5.25 to SLINEAR11 with exponent -4

Exponent = -4 = 11100b (5-bit two's complement)

Mantissa = $5.25 / 2^N = 5.25 / 2^{-4} = 84d$ = 00001010100b (11-bit two's complement)

SLINEAR11 representation = 11100 00001010100b = E054h

Example: Encode 1.00 V to ULINEAR16 with VOUT_MODE = 16h

VOUT_MODE = 16h (Linear Absolute). Exponent (PARAMETER) = 10110b = -10 (5-bit two's complement)

$1.00 \text{ V} = 1.00 / 2^{-10} = 1024d = 0400h$

Example: Decode 03E6h in ULINEAR16 with VOUT_MODE = 16h

VOUT_MODE = 16h (Linear Absolute). Exponent (PARAMETER) = 10110b = -10 (5-bit two's complement)

$2^{-10} \times 03D6h = 0.9746$ V

1.1.3.2 Example system code for PMBus format conversion

Example code for handling the SLINEAR11 and ULINEAR16 formats at the system level is given below. Example code in C-like syntax is provided for reference only. Error checking code is not included. It is the responsibility of the system designer to verify and test all system code.

```
//Maps 5 bit linear exponent to LSB value (2^(twos complement of index))
const float LUT_linear_exponents[32] = {
    1.0,2.0,4.0,8.0,16.0,32.0,64.0,128.0,256.0,512.0,1024.0,2048.0,4096.0,8192.0,
    16384.0,32768.0,0.000152587890625,0.000030517578125,0.00006103515625,
    0.0001220703125,0.000244140625,0.00048828125,0.0009765625,0.001953125,0.00390625,
    0.0078125,0.015625,0.03125,0.0625,0.125,0.25,0.5
};
```

Figure 1-1. Linear exponent to LSB converstion (look-up table approach)

```
unsigned int float_to_slinear11(float number, signed int exponent)
{
    signed int mantissa;
    float lsb;

    //Decode the exponent and generate twos complement form
    if(exponent < 0) {
        lsb = LUT_linear_exponents[(exponent+32)];
    } else {
        lsb = LUT_linear_exponents[exponent];
    }

    //Decode mantissa based on exponent and generate twos complement form
    mantissa = (signed int)(number / lsb);

    //If numbers are negative, de-sign-extend to 5/11 bit numbers
    mantissa &= 0x07FF;
    exponent &= 0x1F;
    return (mantissa | (exponent << 11));
}
```

Figure 1-2. Floating point to SLINEAR11 conversion

```
float slinear11_to_float(unsigned int number)
{
    unsigned int exponent;
    int mantissa;
    float lsb;

    exponent = number >> 11;
    mantissa = number & 0x07FF;

    //Sign extend Mantissa to 32 bits (use your int size here)
    if (mantissa > 0x03FF) {
        mantissa |= 0xFFFFF800;
    }

    lsb = LUT_linear_exponents[exponent];

    return ((float)mantissa)*lsb;
}
```

Figure 1-3. SLINEAR11 to floating point conversion

```
unsigned int float_to_ulinear16(float number, unsigned char vout_mode)
{
    float lsb;
    lsb = LUT_linear_exponents[(vout_mode & 0x1F)];
    return (unsigned int)(number/lsb);
}
```

Figure 1-4. Floating point to ULINEAR16 conversion

```
float ulinear16_to_float(unsigned int number, unsigned char vout_mode)
{
    float lsb;
    lsb = LUT_linear_exponents[(vout_mode & 0x1F)];
    return ((float)number)*lsb;
}
```

Figure 1-5. ULINEAR16 to floating point conversion

1.1.4 PMBus transaction types

These devices are PMBus-compliant. Figure 1-6 through Figure 1-17 show the major communication protocols used. For full details on the PMBus communication protocols, please visit http://pmbus.org.

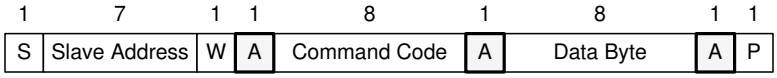

Figure 1-6. Write Byte Protocol

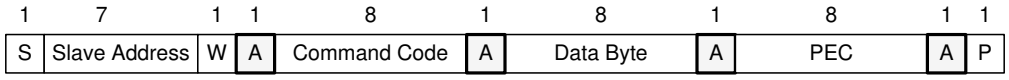

Figure 1-7. Write Byte Protocol with PEC

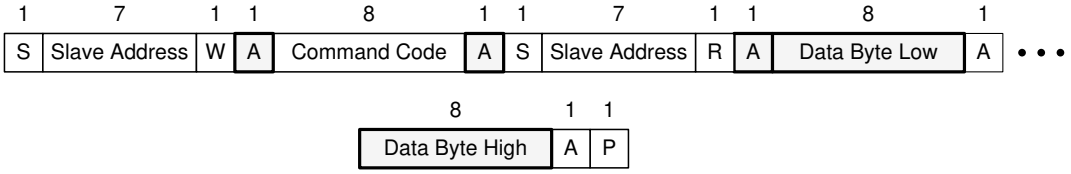

Figure 1-8. Write Word Protocol

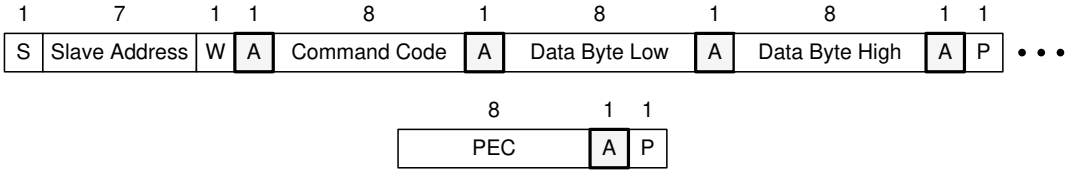

Figure 1-9. Write Word Protocol with PEC

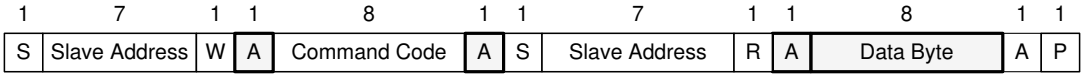

Figure 1-10. Read Byte Protocol

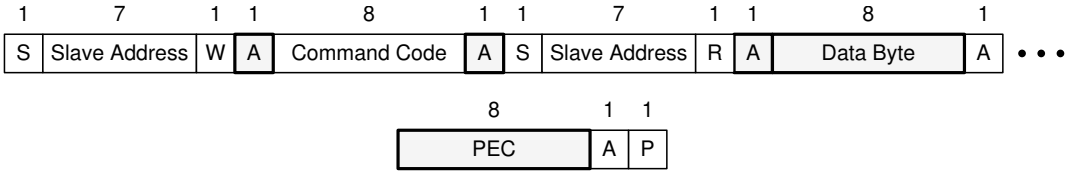

Figure 1-11. Read Byte Protocol with PEC

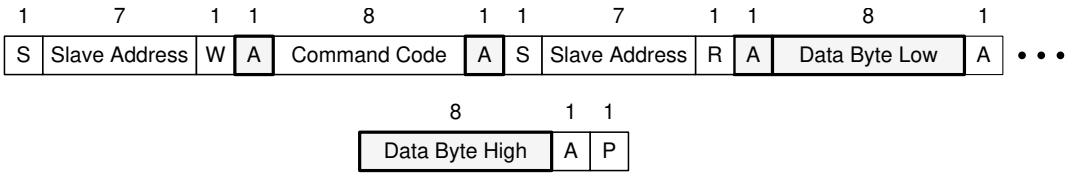

Figure 1-12. Read Word Protocol

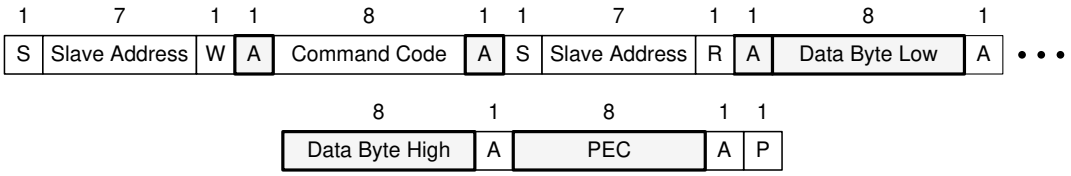

Figure 1-13. Read Word Protocol with PEC

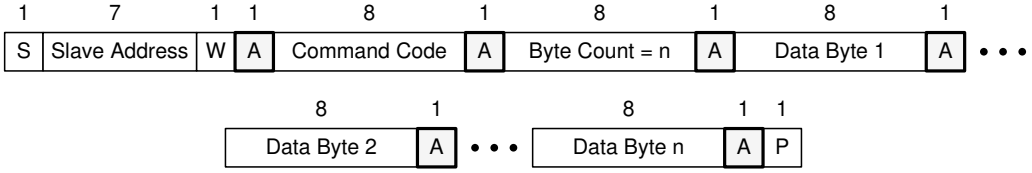

Figure 1-14. Block Write Protocol

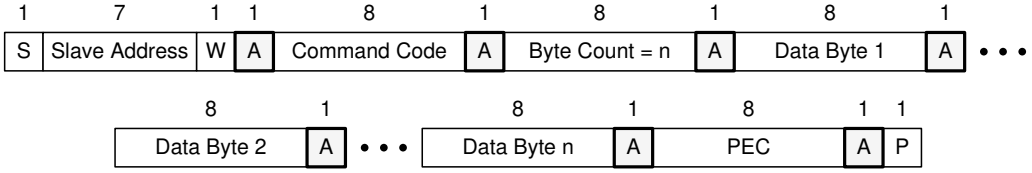

Figure 1-15. Block Write Protocol with PEC

Figure 1-16. Block Read Protocol

Figure 1-17. Block Read Protocol with PEC

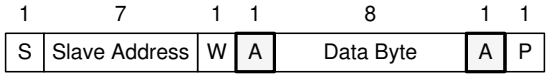

Figure 1-18. Send Byte Protocol

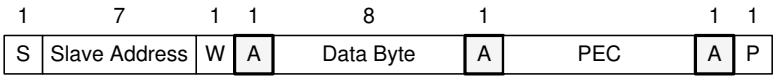

Figure 1-19. Send Byte Protocol with PEC

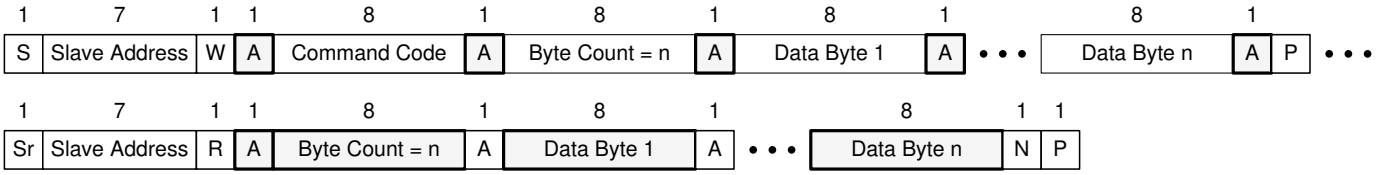

Figure 1-20. Block Write-Block Read Process Call

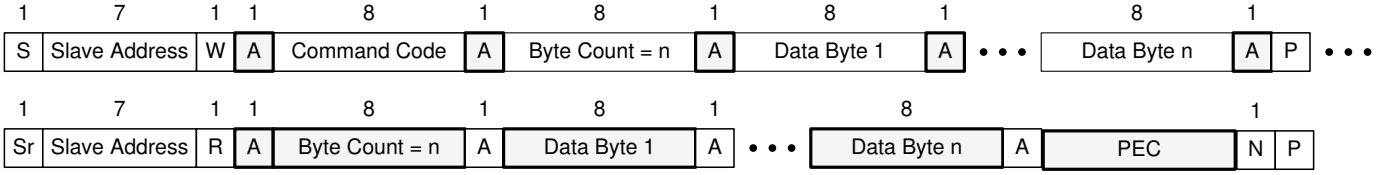

Figure 1-21. Block Write-Block Read Process Call with PEC

1.1.5 General information about device behavior and this document

1.1.5.1 Document convention for byte ordering in block commands

According to the SMBus specification, block commands are transmitted across the PMBus interface in ascending order. The description below shows the convention this document follows for documenting block commands.

This document follows the convention for byte ordering:

- Byte 0 (first byte sent) corresponds to bits 7:0
- Byte 1 (second byte sent) corresponds to bits 15:8
- Byte 2 (third byte sent) corresponds to bits 23:16
- … and so on.

Block Command Byte Ordering

47	46	45	44	43	42	41	40
RW	RW	RW	RW	RW	RW	RW	RW
Byte N							
39	38	37	36	35	34	33	32
RW	RW	RW	RW	RW	RW	RW	RW
Byte …							
31	30	29	28	27	26	25	24
RW	RW	RW	RW	RW	RW	RW	RW
Byte 3							
23	22	21	20	19	18	17	16
RW	RW	RW	RW	RW	RW	RW	RW
Byte 2							
15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
Byte 1							
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
Byte 0							

LEGEND: R/W = Read/Write; R = Read only

1.1.5.2 SLINEAR11 format commands behavior

Clarifications about the behavior of SLINEAR11 format commands:

- Linear exponent values are not stored in NVM backup. Each SLINEAR11 format command has an exponent value listed in the reset value field of its register description. Following a power-on-reset (POR) the device will re-calculate all SLINEAR11 commands according to their reset exponents. For example, if a command has the reset exponent 11110b (-2), writing the value E828h (5.0 with exponent -3), followed by an NVM store operation, results in the command being recalculated as F014h (5.0 with exponent -2) at the next power-on. For systems which perform write-store-read verification, TI recommends to write all linear commands with their reset exponent value, to avoid this confusion.
- NVM storage for most SLINEAR11 commands is limited to the values specified in each command description. During on-the-fly usage, these commands may accept higher resolution than can be stored in non-volatile memory. At the next POR, the nearest supported value in NVM will be selected.
- Some commands have only discrete values supported. When a value is written between two supported values, TPS536xx will accept the command and select the nearest supported value. It is always possible to read-back the exact value written. For example, if a SLINEAR11 command supports the values 1.0 and 2.0, and the user writes the value 1.3, the value 1.0 will be selected, but upon read-back, the returned value will still be 1.3 represented as an SLINEAR11 number. Following an NVM-store and POR event, the command would be recalculated to 1.0, and represented using the reset exponent stated in the command description.
- Read-only telemetry commands in the SLINEAR11 format use variable exponents. As a rule, TPS536xx selects the smallest possible exponent to report telemetry values to maximize the available resolution. Hence, the system host software must be designed to decode exponent values from SLINEAR11 commands.

1.1.5.3 Read-only access fields behavior

Fields which are marked as read-only or reserved in this document are still writeable, but do not have NVM backup, and these fields will be set to 0b following POR events. For example, if a byte command has bit 7 marked as read-only access, and the user writes the value FFh, the TPS536xx will return the value FFh if this command is read-back in the same power cycle; however, following a POR event, the value 7Fh will be returned.

1.1.5.4 Non-standard VOUT_MODE settings

TPS536xx does support VOUT_MODE values other than those explicitly mentioned in this document. In general, updating VOUT_MODE must be done through USER_NVM commands and a POR cycle, instead of individual PMBus commands on-the-fly. Contact your TI representative for more information.

1.1.5.5 Reserved slave addresses

Avoid using the SLAVE_ADDRESS command to configure TPS536xx for reserved addresses. The following addresses are reserved according to the SMBus version 3.0 specification: 0-12d, 40d, 55d, 72-75d, 97d, 120d-127d.

TPS536xx will respond to the SMBus all-call address 0d. TPS536xx will also respond to the ZONE write/read addresses, though ZONE access is NOT supported by this device.

1.2 PMBus Register Maps

1.2.1 (00h) PAGE

CMD Address	00h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
Paged:	No
Phased:	No
NVM Back-up:	No
Updates:	On-the-fly

The PAGE command provides the ability to configure, control and monitor multiple power rails via a single PMBus address. “Channel A” refers to PAGE 0, and “Channel B” refers to PAGE 1.

(00h) PAGE Register Map

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
PAGE							

LEGEND: R/W = Read/Write; R = Read only

Table 1-1. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:0	PAGE	RW	FFh	00h: All commands address PAGE 0 (Channel A) 01h: All commands address PAGE 1 (Channel B) FFh: Commands address PAGE 0 and PAGE 1. See the text below for more information.

Attempts to write PAGE to any value other than those explicitly listed above will be considered invalid/unsupported data and cause TPS536xx to respond by flagging the appropriate status bits, and notifying the host according to the PMBus 1.3.1 Part II specification, section 10.9.3.

Data Validity

The valid values of PAGE are derived based on the configuration of USER_DATA_03 (PHASE_CONFIG). If there are no phases assigned to PAGE =1, then 01h is considered invalid data. Though less common, it is also possible that no phases can be assigned to PAGE =0, in which case, 00h would be invalid data.

PAGE = FFh

Write operations to paged commands when PAGE = FFh address the individual page values. For example:

- Writing VOUT_COMMAND = 1.00 V with PAGE = FFh sets VOUT_COMMAND for both Channel A and Channel B to 1.0 V

There are several special cases for read operations to paged commands when PAGE = FFh. Unless otherwise specified in the individual command descriptions, read operations to paged commands, with PAGE =FFh will return the value for PAGE 0.

1.2.2 (01h) OPERATION

CMD Address	01h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
Paged:	Yes
Phased:	No
NVM Back-up:	No
Updates:	On-the-fly

The OPERATION command is used to enable or disable power conversion, in conjunction input from the enable pins, according to the configuration of the ON_OFF_CONFIG command. It is also used to set the output voltage to the upper or lower MARGIN levels.

(01h) OPERATION Register Map

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	R
ON OFF	SOFT OFF	CONTROL MARGIN				AVS TRANS	0

LEGEND: R/W = Read/Write; R = Read only

Table 1-2. Register Field Descriptions

Bit	Field	Access	Reset	Description
7	ON OFF	RW	0b	Enable/disable power conversion for the currently selected PAGE, when the ON_OFF_CONFIG command is configured to require input from the ON OFF bit for output control. Note that there may be several other requirements that must be satisfied before the power conversion can begin (e.g. input voltages above UVLO thresholds, enable pins high if required by ON_OFF_CONFIG , etc...). 0b: Disable power conversion 1b: Enable power conversion
6	SOFT OFF	RW	0b	Controls the converter shutdown response when ON_OFF_CONFIG is configured to require input from the ON_OFF bit to enable power conversion. SOFT_OFF controls the converter response to un-setting the ON_OFF bit, e.g. setting from 1b to 0b. 0b: Immediate Off. Power conversion stops immediately, without respect for the TOFF_FALL or TOFF_DELAY values. 1b: Soft Off. Power conversion continues for the TOFF_DELAY time, then the output voltage is ramped down to 0 V at a slew rate according to TOFF_FALL. Once the output voltage reaches 0 V, power conversions stops.
5:2	CONTROL MARGIN	RW	See text	Sets the margin state. Based on the NVM values of VOUT SRC CHA and VOUT SRC CHB from MFR_SPECIFIC_ED (MISC_OPTIONS), this command will be reset to either 0000b or 1100b following a power cycle. Changing the VOUT SRC CHx bits themselves does not change the output voltage control. 0000b, 0010b, 0011b: Margin OFF. Output voltage target is VOUT_COMMAND, OV/UV faults behave normally per their respective fault response settings 0 0101b: Margin Low (Ignore Fault).Output voltage target is VOUT_MARGIN_LOW. OV/UV faults are masked. 0110b: Margin Low (Act on Fault). Output voltage target is VOUT_MARGIN_LOW. OV/UV faults trigger per their respective fault response settings. 1001b: Margin High (Ignore Fault). Output voltage target is VOUT_MARGIN_HIGH. OV/UV faults are masked. 1010b: Margin High (Act on Fault). Output voltage target is VOUT_MARGIN_HIGH. OV/UV trigger per their respective fault response settings. 1100b: AVSBus controls the output voltage (**TPS53676 only**) Other: Invalid/Unsupported data.

Table 1-2. Register Field Descriptions (continued)

Bit	Field	Access	Reset	Description
1	AVS TRANS	RW	0b	**TPS53676 only** 0b: VOUT_COMMAND is NOT updated to the AVSBus target voltage when control is passed from AVSBus to PMBus. If the AVSBus target voltage and VOUT_COMMAND are different values, the output voltage transitions to the VOUT_COMMAND value at the slew rate defined by VOUT_TRANSITION_RATE. 1b: VOUT_COMMAND is updated to the AVSBus target output voltage before output voltage control is passed from AVSBus to PMBus.
0	Reserved	R	0b	Not used and always set to 0.

Attempts to write (01h) OPERATION to any value other than those listed above will be considered invalid/unsupported data and cause TPS536xx to respond by flagging the appropriate status bits, and notifying the host according to the PMBus 1.3.1 Part II specification, section 10.9.3.

1.2.3 (02h) ON_OFF_CONFIG

CMD Address	02h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
Paged:	Yes
Phased:	No
NVM Back-up:	EEPROM
Updates:	On-the-fly, but not recommended during power conversion. Polarity changes take effect only after NVM store/power cycle

The ON_OFF_CONFIG command configures the combination of enable pin input and serial bus commands needed to enable/disable power conversion. This includes how the unit responds when power is applied. Note for TPS536xx the CONTROL pin for Channel A may also be referred to as AVR_EN in the device documentation. Likewise, for TPS536xx the Channel B CONTROL pin may also be referred to as BVR_EN.

(02h) ON_OFF_CONFIG Register Map

7	6	5	4	3	2	1	0
R	R	R	RW	RW	RW	RW	RW
0	0	0	PU	CMD	CP	POLARITY	DELAY

LEGEND: R/W = Read/Write; R = Read only

Table 1-3. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:5	Reserved	R	000b	Not used and always set to 0.
4	PU	RW	NVM	0b: Unit starts power conversion any time the input power is present regardless of the state of the CONTROL/VR_EN pin 1b: Act on CONTROL/VR_EN and/or OPERATION command to start/stop power conversion
3	CMD	RW	NVM	0b: Ignore OPERATION Command to start/stop power conversion 1b: Act on OPERATION Command (and CONTROL pin if configured by CP) to start/stop power conversion.
2	CP	RW	NVM	0b: Ignore CONTROL pin to start/stop power conversion. 1b: Act on CONTROL pin (and OPERATION Command if configured by bit [3]) to start/stop power conversion.
1	POLARITY	RW	NVM	0b: CONTROL/VR_EN pin has active low polarity 1b: CONTROL/VR_EN pin has active high polarity
0	DELAY	RW	NVM	0b: When power conversion is commanded OFF by the CONTROL pin (must be configured to respect the CONTROL pin as above), continue regulating for the TOFF_DELAY time, then ramp the output voltage to 0 V, in the time defined by TOFF_FALL. 1b: When power conversion is commanded OFF by the CONTROL pin (must be configured to respect the CONTROL pin as above), stop power conversion immediately.

Attempts to write (02h) ON_OFF_CONFIG to any value other than those explicitly listed above will be considered invalid/unsupported data and cause TPS536xx to respond by flagging the appropriate status bits, and notifying the host according to the PMBus 1.3.1 Part II specification, section 10.9.3.

1.2.4 (03h) CLEAR_FAULTS

CMD Address	03h
Write Transaction:	Send Byte
Read Transaction:	N/A
Format:	Data-less
Paged:	Yes
Phased:	No
NVM Back-up:	No
Updates:	On-the-fly

CLEAR_FAULTS is a paged command used to clear any fault bits that have been set. This command simultaneously clears all bits in all status registers in the selected PAGE . At the same time, the device releases its SMB_ALERT# signal output, if SMB_ALERT# is asserted. CLEAR_FAULTS is a write-only command with no data.

The CLEAR_FAULTS command does not cause a unit that has latched off for a fault condition to restart. If the fault is still present when the bit is cleared, the fault bit immediately sets again and the host is notified by the usual means.

If the device responds to an Alert Response Address (ARA) from the host, it will clear SMB_ALERT# but not clear the offending status bit(s) (as it has successfully notified the host and then expects the host to handle the interrupt appropriately). The original fault and any from other sources that occur between the initial assertion of SMB_ALERT# and the device's successful response to the ARA are cleared (via CLEAR_FAULTS , OFF-ON toggle, or power reset) before any of these sources are allowed to re-trigger SMB_ALERT#. However, fault sources which only become active post-ARA trigger SMB_ALERT#.

(03h) CLEAR_FAULTS Register Map

7	6	5	4	3	2	1	0
W	W	W	W	W	W	W	W
CLEAR FAULTS							

LEGEND: R/W = Read/Write; R = Read only

1.2.5 (04h) PHASE

CMD Address	04h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
Paged:	Yes
Phased:	No
NVM Back-up:	No
Updates:	On-the-fly

The PHASE command provides the ability to configure, control, and monitor multiple phases on one PAGE . Each PHASE contains the Operating Memory (and at the option of the device manufacturer, User Store) for one phase output. The phase selected by the PHASE command will be used for all subsequent phase-dependent commands. The phase configuration needs to be established before any phase-dependent command can be successfully executed.

(04h) PHASE Register Map

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
PHASE							

LEGEND: R/W = Read/Write; R = Read only

Table 1-4. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:0	PHASE	RW	FFh	00h: All commands address Phase 1 01h: All commands address Phase 2 02h: All commands address Phase 3 03h: All commands address Phase 4 04h: All commands address Phase 5 05h: All commands address Phase 6 06h: All commands address Phase 7 07h: All commands address Phase 8 **(TPS536C7 only)** 08h: All commands address Phase 9 **(TPS536C7 only)** 09h: All commands address Phase 10 **(TPS536C7 only)** 0Ah: All commands address Phase 11 **(TPS536C7 only)** 0Bh: All commands address Phase 12 **(TPS536C7 only)** 08h-FEh: Unsupported/Invalid data FFh: Commands are addressed to all phases in the PAGE as a single entity. See the text below for more information.

The range of valid data for PHASE also depends on the phase configuration. Attempts to write (04h) PHASE to a value not supported by the current phase configuration will be considered invalid/unsupported data and cause TPS536xx to respond by flagging the appropriate status bits, and notifying the host according to the PMBus 1.3.1 Part II specification, section 10.9.3.

Note that the TPS536xx supports flexible phase configuration and allows some phases to be assigned to either channel, and fire in any position, via the USER_DATA_03 (PHASE_CONFIG) command. Refer to the USER_DATA_03 (PHASE_CONFIG) command for information about assigning phases to channels and firing positions.

PHASE = FFh

When PHASE = FFh, write operations to phased commands address the total PAGE as a single entity. For example:

- Writing IOUT_OC_FAULT_LIMIT = 40 A, with PHASE = FFh sets the total overcurrent limit for the active PAGE to 40 A. The per-phase overcurrent limits remain unchanged. That is, this operation limits the sum of the I_{SUM} to 40A, but does not change the current limit of any one individual phase.

PAGE = FFh

Note that when PAGE = FFh, the TPS536xx validates the value of the PHASE command, based on USER_DATA_03 (PHASE_CONFIG), to determine whether the new PHASE number exists in either page. For example, if PAGE = FFh, and PHASE is updated to PHASE = 4, the new value of 4 will be accepted if either page has a physical phase assigned to PHASE = 4.

As a consequence of this behavior, is possible to update PHASE setting with a value existing in one page and not the other. In this case, only the PHASE value for the page containing the new PHASE value is updated, and the other page is not.

1.2.6 (05h) PAGE_PLUS_WRITE

CMD Address	05h
Write Transaction:	Write Block
Read Transaction:	N/A
Format:	Variable
Paged:	No
Phased:	No
NVM Back-up:	Per command field
Updates:	Per command field

The PAGE_PLUS_WRITE command is used to set the page within a device, send a command, and send the data for the command in one packet. After this command is completed, the PAGE register shall have a value set to the PAGE value identified in the command.

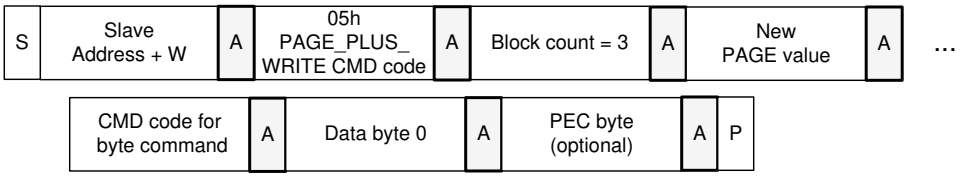

Figure 1-22. PAGE_PLUS_WRITE for byte command

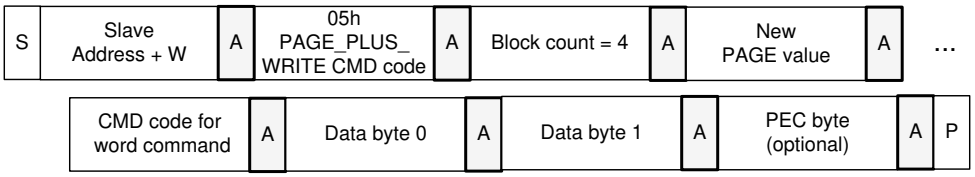

Figure 1-23. PAGE_PLUS_WRITE for word command

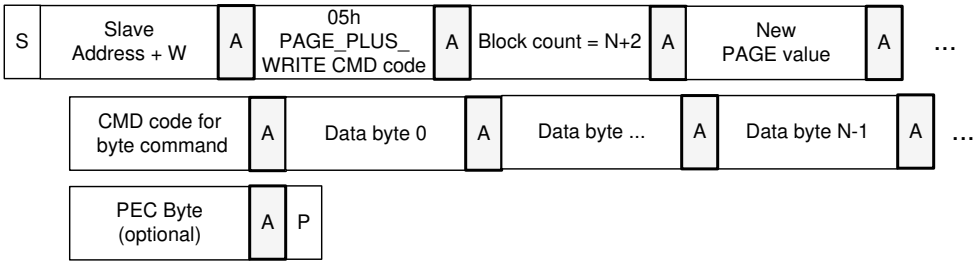

Figure 1-24. PAGE_PLUS_WRITE for block command

1.2.7 (06h) PAGE_PLUS_READ

CMD Address	06h
Write Transaction:	N/A
Read Transaction:	Block-Write/Block-Read Process Call
Format:	Variable
Paged:	No
Phased:	No
NVM Back-up:	Per command field
Updates:	Per command field

The PAGE_PLUS_READ command is used to set the page within a device, send a command, and read the data returned by the command in one packet. After this command is completed, the PAGE register will have a value set to the PAGE value identified in the command.

Note that nesting of block-write/block-read process call transactions is not allowed. As a result, TPS536xx does not allow the user to read the value of SMBALERT_MASK_WORD bits through PAGE_PLUS_READ.

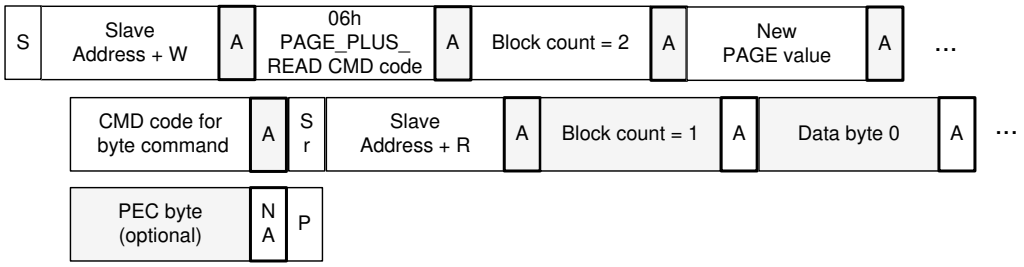

Figure 1-25. PAGE_PLUS_READ for byte command

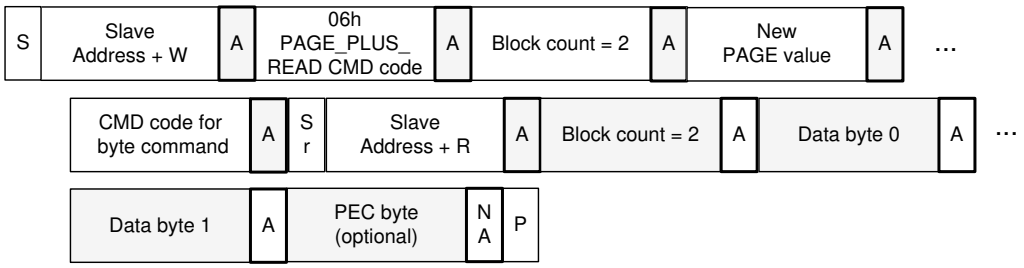

Figure 1-26. PAGE_PLUS_READ for word command

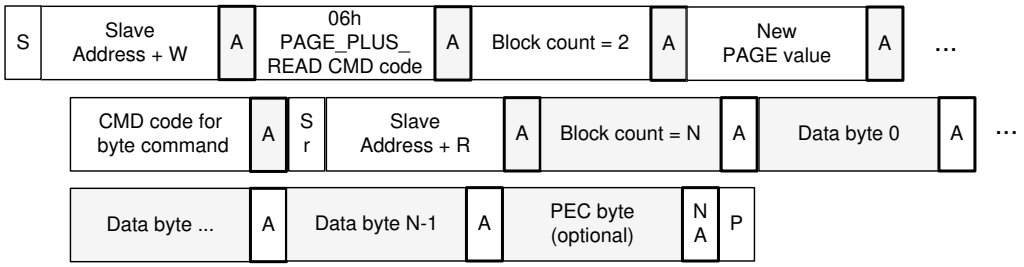

Figure 1-27. PAGE_PLUS_READ for block command

1.2.8 (10h) WRITE_PROTECT

CMD Address	10h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
Paged:	No
Phased:	No
NVM Back-up:	EEPROM
Updates:	On-the-fly

The WRITE_PROTECT command controls writing to the PMBus device. The intent of this command is to provide protection against accidental changes; it has one data byte, described below. This command does NOT provide protection against deliberate or malicious changes to a device's configuration or operation. All supported commands may have their parameters read, regardless of the WRITE_PROTECT settings.

(10h) WRITE_PROTECT Register Map

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
WRITE PROTECT							

LEGEND: R/W = Read/Write; R = Read only

Table 1-5. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:0	WRITE PROTECT	RW	NVM	00h: Enable writes to all commands 03h: Manufacturer-specific write protection is enabled. Refer to MFR_SPECIFIC_FB (MFR_SPECIFIC_WRITE_PROTECT) 20h: Disables all write access except to theWRITE_PROTECT , OPERATION , PAGE , ON_OFF_CONFIG , and VOUT_COMMAND commands. 40h: Disables all WRITES except to the WRITE_PROTECT , OPERATION and PAGE commands. 80h: Disables all WRITES except to the WRITE_PROTECT command. Other: Invalid/Unsupported data.

Attempts to write (10h) WRITE_PROTECT to any invalid value as specified above will be considered invalid/unsupported data and cause TPS536xx to respond by flagging the appropriate status bits, and notifying the host according to the PMBus 1.3.1 Part II specification, section 10.9.3.

Table 1-6. (10h) WRITE_PROTECT, (FBh) MFR_WRITE_PROTECT and (FAh) NVM_LOCK functionality

(FAh) NVM_LOCK	(10h) WRITE_PROTECT	(FBh) MFR_WRITE_PROTECT	Command Access
Writeable Unlocked	Writeable 00h (all commands writeable)	Writeable X (Don't care)	All commands writeable
Writeable Unlocked	Writeable 20h, 40h, 80h	Writeable X (Don't care)	Based on (10h) WRITE_PROTECT
Writeable Unlocked	Writeable 03h	Writeable Per MFR_WRITE_PROTECT command map	Based on (FBh) MFR_WRITE_PROTECT
Writeable Locked	Read-only 00h (all commands writeable)	Read-only X (Don't care)	All commands writeable
Writeable Locked	Read-only 20h, 40h, 80h	Read-only X (Don't care)	Based on (10h) WRITE_PROTECT
Writeable Locked	Read-only 03h	Read-only Per MFR_WRITE_PROTECT command map	Based on (FBh) MFR_WRITE_PROTECT

Table 1-6. (10h) WRITE_PROTECT, (FBh) MFR_WRITE_PROTECT and (FAh) NVM_LOCK functionality (continued)

(FAh) NVM_LOCK	(10h) WRITE_PROTECT	(FBh) MFR_WRITE_PROTECT	Command Access
Read-only (Incorrect Password Issued) Locked	Read-only 00h (all commands writeable)	Read-only X (Don't care)	All commands writeable
Read-only (Incorrect Password Issued) Locked	Read-only 20h, 40h, 80h	Read-only X (Don't care)	Based on (10h) WRITE_PROTECT
Read-only (Incorrect Password Issued) Locked	Read-only 03h	Read-only Per MFR_WRITE_PROTECT command map	Based on (FBh) MFR_WRITE_PROTECT

1.2.9 (11h) STORE_DEFAULT_ALL

CMD Address	11h
Write Transaction:	Send Byte
Read Transaction:	N/A
Format:	Data-less
Paged:	No
Phased:	No
NVM Back-up:	No
Updates:	Not recommended for on-the-fly-use, but not explicitly blocked

The STORE_DEFAULT_ALL command is provided for backward-compatibility, functions identically to STORE_USER_ALL . TPS536xx does not have different NVM areas for Default and User values.

(11h) STORE_DEFAULT_ALL Register Map

7	6	5	4	3	2	1	0
W	W	W	W	W	W	W	W
STORE DEFAULT ALL							

LEGEND: R/W = Read/Write; R = Read only

NVM Store operations are not recommended while the output voltages are in regulation, although the user is not explicitly prevented from doing so. During the NVM store operation, all faults are masked so as to ensure the operation is not interrupted, as interruption could result in a corrupted NVM. Hence, there is significant risk to issuing NVM store operations during power conversion. PMBus commands issued during this time may cause long clock stretch times, or simply be ignored. TI recommends disabling regulation, and waiting 100 ms minimum before continuing, following issuance of NVM store operations. In order to guarantee proper memory storage and retention, the user must ensure the 3.3V supply voltage is maintained for the entire duration of the NVM storage operation.

1.2.10 (12h) RESTORE_DEFAULT_ALL

CMD Address	12h
Write Transaction:	Send Byte
Read Transaction:	N/A
Format:	Data-less
Paged:	No
Phased:	No
NVM Back-up:	N/A
Updates:	Updates accepted only with power conversion disabled.

WARNING

TI does not recommend issuing NVM restore operations during power conversion. Depending on the data being restored, versus the current operating memory, proper output voltage behavior cannot be guaranteed during restore operations which occur while the unit is converting power. Disable power conversion before issuing this command.

The RESTORE_DEFAULT_ALL command is provided for backward-compatibility, it functions identically to RESTORE_USER_ALL . TPS536xx does not have different NVM areas for Default and User values.

(12h) RESTORE_DEFAULT_ALL Register Map

7	6	5	4	3	2	1	0
W	W	W	W	W	W	W	W
RESTORE DEFAULT ALL							

LEGEND: R/W = Read/Write; R = Read only

1.2.11 (15h) STORE_USER_ALL

CMD Address	15h
Write Transaction:	Send Byte
Read Transaction:	N/A
Format:	Data-less
Paged:	No
Phased:	No
NVM Back-up:	No
Updates:	Not recommended for on-the-fly-use, but not explicitly blocked

The STORE_USER_ALL command instructs the PMBus device to copy the entire contents of the operating memory to the matching locations in the non-volatile user store memory. Any items in Operating Memory that do not have matching locations in the User Store are ignored.

NVM Store operations are not recommended while the output voltages are in regulation, although the user is not explicitly prevented from doing so, as interruption could result in a corrupted NVM. During the NVM store operation, all faults are masked so as to ensure the operation is not interrupted. Hence, there is significant risk to issuing NVM store operations during power conversion. PMBus commands issued during this time may cause long clock stretch times, or simply be ignored. TI recommends disabling regulation, and waiting 100 ms minimum before continuing, following issuance of NVM store operations. In order to guarantee proper memory storage and retention, the user must ensure the 3.3V supply voltage is maintained for the entire duration of the NVM storage operation.

(15h) STORE_USER_ALL Register Map

7	6	5	4	3	2	1	0
W	W	W	W	W	W	W	W
STORE USER ALL							

LEGEND: R/W = Read/Write; R = Read only

1.2.12 (16h) RESTORE_USER_ALL

CMD Address	16h
Write Transaction:	Send Byte
Read Transaction:	N/A
Format:	Data-less
Paged:	No
Phased:	No
NVM Back-up:	No
Updates:	Updates accepted only with power conversion disabled.

WARNING

TI does not recommend issuing NVM restore operations during power conversion. Depending on the data being restored, versus the current operating memory, proper output voltage behavior cannot be guaranteed during restore operations which occur while the unit is converting power. Disable power conversion before issuing this command.

The RESTORE_USER_ALL command instructs the PMBus device to copy the entire contents of the non-volatile User Store memory to the matching locations in the Operating Memory. The values in the Operating Memory are overwritten by the value retrieved from the User Store. Any items in User Store that do not have matching locations in the Operating Memory are ignored.

(16h) RESTORE_USER_ALL Register Map

7	6	5	4	3	2	1	0
W	W	W	W	W	W	W	W
RESTORE USER ALL							

LEGEND: R/W = Read/Write; R = Read only

1.2.13 (19h) CAPABILITY

CMD Address	19h
Write Transaction:	N/A
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
Paged:	No
Phased:	No
NVM Back-up:	No
Updates:	N/A

This command provides a way for the host to determine the capabilities of this PMBus device. This command is read-only and has one data byte formatted as below.

(19h) CAPABILITY Register Map

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
PEC	SPEED		ALERT	FORMAT	AVSBUS	0	0

LEGEND: R/W = Read/Write; R = Read only

Table 1-7. Register Field Descriptions

Bit	Field	Access	Reset	Description
7	PEC	R	1b	0b: Packet Error Checking is not supported 1b: Packet Error Checking is supported.
6	SPEED	R	10b	00b: Maximum supported bus speed is 100kHz 01b: Maximum supported bus speed is 400kHz 10b: Maximum supported bus speed is 1MHz 11b: Reserved
5:4	ALERT	R	1b	0b: The devices does NOT have a SMB_ ALERT# pin and does not support the SMBus Alert Response Protocol
3	FORMAT	R	0b	0b: Numeric format is LINEAR or DIRECT. 1b: Numeric data is in IEEE Half Precision Floating Point Format . Not currently supported.
2	AVSBUS	R	0b (TPS536C7) or 1b (TPS53676)	0b: AVSBus is NOT supported 1b: AVSBus is supported
1:0	Reserved	R	00b	Reserved and always set to 0

Attempts to write (19h) CAPABILITY to any value will be considered invalid/unsupported data and cause TPS536xx to respond by flagging the appropriate status bits, and notifying the host according to the PMBus 1.3.1 Part II specification, section 10.9.3.

1.2.14 (1Bh) SMBALERT_MASK_WORD

CMD Address	1Bh
Write Transaction:	N/A
Read Transaction:	Block-Write/Block-Read Process Call
Format:	Unsigned Binary (1 byte)
Paged:	Yes
Phased:	No
NVM Back-up:	EEPROM
Updates:	On-the-fly

SMBALERT_MASK bits for the STATUS_WORD command.

Note: The VOUT, IOUT, INPUT, and MFR fields within the STATUS_WORD do not have individual mask bits, as these bits will be asserted whenever an SMBALERT source in STATUS_VOUT , STATUS_IOUT , STATUS_INPUT , and STATUS_MFR are asserted respectively. PGOOD is an exception in that it does not appear in any other status registers.

(1Bh) SMBALERT_MASK_WORD Register Map

7	6	5	4	3	2	1	0.
R	R	R	R	R	R	R	R
0	0	0	0	mPGOOD	0	0	0

LEGEND: R/W = Read/Write; R = Read only

Table 1-8. Register Field Descriptions

Bit	Field	Access	Reset	Description
3	mPGOOD	R	1b	**This mask bit is hardcoded to 1b** 0b: SMBALERT may assert due to this condition. 1b: SMBALERT may NOT assert due to this condition.
2:0	Reserved	R	0	Reserved

1.2.15 (1Bh) SMBALERT_MASK_VOUT

CMD Address	1Bh
Write Transaction:	Write Word Low byte = 7Ah (STATUS_VOUT) High byte = Mask value
Read Transaction:	Block-Write/Block-Read Process Call
Format:	Unsigned Binary (1 byte)
Paged:	Yes
Phased:	No
NVM Back-up:	EEPROM
Updates:	On-the-fly

SMBALERT_MASK bits for the STATUS_VOUT command.

(1Bh) SMBALERT_MASK_VOUT Register Map

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	R	R
mVOUT OVF	mVOUT OVW	mVOUT UVW	mVOUT UVF	mVOUT MINMAX	mTON MAX	0	0

LEGEND: R/W = Read/Write; R = Read only

Table 1-9. Register Field Descriptions

Bit	Field	Access	Reset	Description
7	mVOUT OVF	RW	NVM	0b: SMBALERT may assert due to this condition. 1b: SMBALERT may NOT assert due to this condition.
6	mVOUT OVW	RW	NVM	0b: SMBALERT may assert due to this condition. 1b: SMBALERT may NOT assert due to this condition.
5	mVOUT UVW	RW	NVM	0b: SMBALERT may assert due to this condition. 1b: SMBALERT may NOT assert due to this condition.
4	mVOUT UVF	RW	NVM	0b: SMBALERT may assert due to this condition. 1b: SMBALERT may NOT assert due to this condition.
3	mVOUT MINMAX	RW	NVM	0b: SMBALERT may assert due to this condition. 1b: SMBALERT may NOT assert due to this condition.
2	mTON MAX	RW	NVM	0b: SMBALERT may assert due to this condition. 1b: SMBALERT may NOT assert due to this condition.
1:0	Not supported	R	0b	Not supported and always set to 0b

1.2.16 (1Bh) SMBALERT_MASK_IOUT

CMD Address	1Bh
Write Transaction:	Write Word Low byte = 7Bh (STATUS_IOUT) High byte = Mask value
Read Transaction:	Block-Write/Block-Read Process Call
Format:	Unsigned Binary (1 byte)
Paged:	Yes
Phased:	No
NVM Back-up:	EEPROM
Updates:	On-the-fly

SMBALERT_MASK bits for STATUS_IOUT .

(1Bh) SMBALERT_MASK_IOUT Register Map

7	6	5	4	3	2	1	0
RW	R	RW	RW	RW	R	R	R
mIOUT OCF	0	mIOUT OCW	mIOUT UCF	mCUR SHAREF	0	0	0

LEGEND: R/W = Read/Write; R = Read only

Table 1-10. Register Field Descriptions

Bit	Field	Access	Reset	Description
7	mIOUT OCF	RW	NVM	0b: SMBALERT may assert due to this condition. 1b: SMBALERT may NOT assert due to this condition.
6	Reserved	R	0b	Reserved
5	mIOUT OCW	RW	NVM	0b: SMBALERT may assert due to this condition. 1b: SMBALERT may NOT assert due to this condition.
4	mIOUT UCF	RW	NVM	0b: SMBALERT may assert due to this condition. 1b: SMBALERT may NOT assert due to this condition.
3	mCUR SHAREF	RW	NVM	0b: SMBALERT may assert due to this condition. 1b: SMBALERT may NOT assert due to this condition.
2:0	Reserved	RW	0b	Reserved

1.2.17 (1Bh) SMBALERT_MASK_INPUT

CMD Address	1Bh
Write Transaction:	Write Word Low byte = 7Ch (STATUS_INPUT) High byte = Mask value
Read Transaction:	Block-Write/Block-Read Process Call
Format:	Unsigned Binary (1 byte)
Paged:	No
Phased:	No
NVM Back-up:	EEPROM
Updates:	On-the-fly

SMBALERT_MASK bits for STATUS_INPUT .

(1Bh) SMBALERT_MASK_INPUT Register Map

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
mVIN OVF	mVIN OVW	mVIN UVW	mVIN UVF	mLOW VIN	mIIN OCF	mIIN OCW	mPIN OPW

LEGEND: R/W = Read/Write; R = Read only

Table 1-11. Register Field Descriptions

Bit	Field	Access	Reset	Description
7	mVIN OVF	RW	NVM	0b: SMBALERT may assert due to this condition. 1b: SMBALERT may NOT assert due to this condition.
6	mVIN OVW	RW	NVM	0b: SMBALERT may assert due to this condition. 1b: SMBALERT may NOT assert due to this condition.
5	mVIN UVW	RW	NVM	0b: SMBALERT may assert due to this condition. 1b: SMBALERT may NOT assert due to this condition.
4	mVIN UVF	RW	NVM	0b: SMBALERT may assert due to this condition. 1b: SMBALERT may NOT assert due to this condition.
3	mLOW VIN	RW	NVM	0b: SMBALERT may assert due to this condition. 1b: SMBALERT may NOT assert due to this condition.
2	mIIN OCF	RW	NVM	0b: SMBALERT may assert due to this condition. 1b: SMBALERT may NOT assert due to this condition.
1	mIIN OCW	RW	NVM	0b: SMBALERT may assert due to this condition. 1b: SMBALERT may NOT assert due to this condition.
0	mPIN OPW	RW	NVM	0b: SMBALERT may assert due to this condition. 1b: SMBALERT may NOT assert due to this condition.

1.2.18 (1Bh) SMBALERT_MASK_TEMPERATURE

CMD Address	1Bh (with CMD byte = 7Dh)
Write Transaction:	Write Word Low byte = 7Dh (STATUS_TEMPERATURE) High byte = Mask value
Read Transaction:	Block-Write/Block-Read Process Call
Format:	Unsigned Binary (1 byte)
Paged:	Yes
Phased:	No
NVM Back-up:	EEPROM
Updates:	On-the-fly

SMBALERT_MASK bits for STATUS_TEMPERATURE

(1Bh) SMBALERT_MASK_TEMPERATURE Register Map

7	6	5	4	3	2	1	0
RW	RW	R	R	R	R	R	R
mOTF	mOTW	0	0	0	0	0	0

LEGEND: R/W = Read/Write; R = Read only

Table 1-12. Register Field Descriptions

Bit	Field	Access	Reset	Description
7	mOTF	RW	NVM	0b: SMBALERT may assert due to this condition. 1b: SMBALERT may NOT assert due to this condition.
6	mOTW	RW	NVM	0b: SMBALERT may assert due to this condition. 1b: SMBALERT may NOT assert due to this condition.
5:0	Not supported	R	0d	Not supported and always set to 000000b

1.2.19 (1Bh) SMBALERT_MASK_CML

CMD Address	1Bh
Write Transaction:	Write Word Low byte = 7Eh (STATUS_CML) High byte = Mask value
Read Transaction:	Block-Write/Block-Read Process Call
Format:	Unsigned Binary (1 byte)
Paged:	No
Phased:	No
NVM Back-up:	EEPROM
Updates:	On-the-fly

SMBALERT_MASK bits for STATUS_CML

(1Bh) SMBALERT_MASK_CML Register Map

7	6	5	4	3	2	1	0
RW	RW	RW	RW	R	R	RW	RW
mIVC	mIVD	mPEC	mMEM	0	0	mCOMM	mCML OTHER

LEGEND: R/W = Read/Write; R = Read only

Table 1-13. Register Field Descriptions

Bit	Field	Access	Reset	Description
7	IVC	RW	NVM	0b: SMBALERT may assert due to this condition. 1b: SMBALERT may NOT assert due to this condition.
6	IVD	RW	NVM	0b: SMBALERT may assert due to this condition. 1b: SMBALERT may NOT assert due to this condition.
5	PEC	RW	NVM	0b: SMBALERT may assert due to this condition. 1b: SMBALERT may NOT assert due to this condition.
4	MEM	RW	NVM	0b: SMBALERT may assert due to this condition. 1b: SMBALERT may NOT assert due to this condition.
3:2	Not supported	R	00b	Reserved
1	COMM	RW	NVM	0b: SMBALERT may assert due to this condition. 1b: SMBALERT may NOT assert due to this condition.
0	CML OTHER	RW	NVM	0b: SMBALERT may assert due to this condition. 1b: SMBALERT may NOT assert due to this condition.

1.2.20 (1Bh) SMBALERT_MASK_MFR

CMD Address	1Bh
Write Transaction:	Write Word Low byte = 80h (STATUS_MFR_SPECIFIC) High byte = Mask value
Read Transaction:	Block-Write/Block-Read Process Call
Format:	Unsigned Binary (1 byte)
Paged:	Yes
Phased:	No
NVM Back-up:	EEPROM
Updates:	On-the-fly

SMBALERT_MASK bits for STATUS_MFR.

(1Bh) SMBALERT_MASK_MFR Register Map

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	R	R	RW
mPOR	mEXT	mVR SETTLED	mPHERR	mRESET	0	0	mPSFLT

LEGEND: R/W = Read/Write; R = Read only

Table 1-14. Register Field Descriptions

Bit	Field	Access	Reset	Description
7	mPOR	RW	NVM	0b: SMBALERT may assert due to this condition. 1b: SMBALERT may NOT assert due to this condition.
6	mEXT	RW	NVM	0b: SMBALERT may assert due to this condition. 1b: SMBALERT may NOT assert due to this condition.
5	mVR SETTLE	RW	NVM	0b: SMBALERT may assert due to this condition. 1b: SMBALERT may NOT assert due to this condition.
4	mPHERR	RW	NVM	0b: SMBALERT may assert due to this condition. 1b: SMBALERT may NOT assert due to this condition.
3	mRESET	RW	NVM	0b: SMBALERT may assert due to this condition. 1b: SMBALERT may NOT assert due to this condition.
2:1	Reserved	RW	0	Reserved
0	mPSFLT	RW	NVM	0b: SMBALERT may assert due to this condition. 1b: SMBALERT may NOT assert due to this condition.

1.2.21 (20h) VOUT_MODE

CMD Address	20h
Write Transaction:	N/A
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
Paged:	Yes
Phased:	No
NVM Back-up:	EEPROM
Updates:	N/A

WARNING

The VOUT_MODE command is writeable, but TI does not recommend modifying it from its default value. All device documentation, including the datasheet refers to this command as read-only.

The data byte for the VOUT_MODE command is one byte that consists of a three bit Mode and a five bit Parameter as shown in Figure 6. The three bit Mode sets whether the device uses the ULINEAR16, Half-precision IEEE 754 floating point, VID or DIRECT modes for output voltage related commands. The five bit Parameter provides more information about the selected mode, such as which manufacturer's VID codes are being used.

The default VOUT_MODE for TPS536xx is the **Absolute, ULINEAR16 mode with exponent = -10**. TI does not recommend changing this format.

(20h) VOUT_MODE Register Map

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
REL	MODE		PARAM				

LEGEND: R/W = Read/Write; R = Read only

Table 1-15. Register Field Descriptions

Bit	Field	Access	Reset	Description
7	REL	R	0b	0b: Absolute Data Format 1b: Relative Data Format. Note relative data format and VID mode may not be used together.
6:5	MODE	R	00b	00b: Linear Format (ULINEAR16, SLINEAR16) 01b: VID Format (refer to the table below). Note relative data format and VID mode may not be used together.
4:0	PARAM	R	10110b	Linear exponent N = -10, 0.9765625 mV per LSB

1.2.22 (21h) VOUT_COMMAND

CMD Address	21h
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	ULINEAR16, Absolute
Paged:	Yes
Phased:	No
NVM Back-up:	EEPROM
Updates:	on-the-fly (will not be accepted when AVSBus has control of the output voltage).

VOUT_COMMAND causes the device to set its output voltage to the commanded value with two data bytes. Output voltage changes due to VOUT_COMMAND occur at the rate specified by VOUT_TRANSITION_RATE.

(21h) VOUT_COMMAND Register Map

15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
VOUT COMMAND (High Byte)							
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VOUT COMMAND (Low Byte)							

LEGEND: R/W = Read/Write; R = Read only

Table 1-16. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:0	VOUT COMMAND	RW	NVM or Pinstrap (Ch A only)	Sets the output voltage target via the PMBus interface in ULINEAR16 format.

Data Validity:

Writes to VOUT_COMMAND for which the resulting value, including any offset from VOUT_TRIM is greater than the current VOUT_MAX , or less than the current VOUT_MIN , cause the reference DAC to move to the value specified by VOUT_MIN or VOUT_MAX respectively. Note that no status bit or SMB_ALERT# condition will be triggered by this operation.

Note that the data validity mentioned in the table is outside the recommended output voltage ranges for using an external resistive divider in the voltage feedback sense lines. Refer to the product datasheet for recommended output voltage values for each combination of VOUT_MAX , VOUT_SCALE_LOOP and the use of an external resistor divider.

Table 1-17. VOUT_COMMAND/VOUT_MARGIN + VOUT_TRIM data validity (Linear Format)

VOUT SCALE LOOP	VOUT MAX De-coded value	External Divider	Valid VOUT COMMAND / MARGIN + VOUT TRIM Values
1.0	0.000 V to 1.870 V	None	0.000V to 1.870 V
1.0	1.870 V to 3.740 V	None	0.000 V to 3.740 V
0.5	3.740 V to 5.500 V	2:1	0.000 V to 5.500 V

Attempts to write (21h) VOUT_COMMAND to any value outside those specified as valid, will be considered invalid/unsupported data and cause TPS536xx to respond by flagging the appropriate status bits, and notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

Note also that the user is prevented from VOUT_MAX changing VOUT_MAX from less than 1.87 V to greater than 1.87 V during operation. This could cause unwanted disturbance on the output voltage due to architectural limitations of TPS536xx.

Boot voltage (V_{BOOT}) behavior:

At power-up, the reset value of VOUT_COMMAND for channel A (PAGE = 0) is derived from either pin-detection on the VBOOT_CHA pin, or from the NVM area, depending on the PD BOOT bit in the MFR SPECIFIC_EE (PIN_DETECT_OVERRIDE) command. When PD BOOT = 0b, the default value of VOUT_COMMAND is restored from NVM at boot-up. When PD BOOT = 1b, the default value of VOUT_COMMAND is derived from pin-detection on the VBOOT_CHA. The boot voltage for channel B (PAGE=1) is always derived from NVM and cannot be configured otherwise.

This default value, whether derived from pin detection, or NVM becomes the "default" output voltage (also referred to as V_{BOOT}), and is stored in operating memory separately from the current value of VOUT_COMMAND . A control bit in MFR_SPECIFIC_ED (MISC_OPTIONS), RSTOSD, controls the boot behavior for subsequent enable cycles.

1.2.23 (22h) VOUT_TRIM

CMD Address	22h
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	SLINEAR16, Absolute
Paged:	Yes
Phased:	No
NVM Back-up:	EEPROM
Updates:	on-the-fly

VOUT_TRIM is used to apply a fixed offset voltage to the output voltage command value. Output voltage changes due to VOUT_TRIM occur at the rate specified by VOUT_TRANSITION_RATE .

(22h) VOUT_TRIM Register Map

15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
VOUT TRIM (High Byte)							
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VOUT TRIM (Low Byte)							

LEGEND: R/W = Read/Write; R = Read only

Table 1-18. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:0	VOUT TRIM	RW	NVM	Output voltage offset. SLINEAR16 (two's complement) format

Limited NVM back-up

Only 8 bits of NVM backup are provided for this command. Per the PMBus spedcification, the VOUT_TRIM command follows the VOUT_MODE exponent, in SLINEAR16 format only. Use the TRIM EXT field in MFR_SPECIFIC_ED (MISC_OPTIONS) to extend the range of VOUT_TRIM at the expense of resolution. Note that VOUT_TRIM may not cause the output voltage to exceed the limits set by VOUT_MIN and VOUT_MAX .

Table 1-19. VOUT_COMMAND/VOUT_MARGIN + VOUT_TRIM data validity (Linear Format)

TRIM EXT (binary)	NVM-backed VOUT_TRIM bits	NVM stored LSB (linear exponent)	Effective trim range
00b	15, 6:0	2^{-10}	-125 mV to +124 mV
01b	15, 7:1	2^{-9}	-250 mV to +248 mV
10b	15, 8:2	2^{-8}	-500 mV to +496 mV
11b	15, 9:3	2^{-7}	-1000 mV to +992 mV

Data Validity

Referring to the data validity table in VOUT_COMMAND (reproduced below), the output voltage value (including any offset from VOUT_TRIM , VOUT_COMMAND , VOUT_MARGIN_HIGH, VOUT_MARGIN_LOW) may not exceed the values supported by the DAC hardware.

Table 1-20. VOUT_COMMAND/VOUT_MARGIN + VOUT_TRIM data validity (Linear Format)

VOUT SCALE LOOP	VOUT MAX Decoded value	External Divider	Valid VOUT COMMAND / MARGIN + VOUT TRIM Values
1.0	0.000 V to 1.870 V	None	0.000V to 1.870 V

Table 1-20. VOUT_COMMAND/VOUT_MARGIN + VOUT_TRIM data validity (Linear Format) (continued)

VOUT SCALE LOOP	VOUT MAX Decoded value	External Divider	Valid VOUT COMMAND / MARGIN + VOUT TRIM Values
1.0	1.870 V to 3.740 V	None	0.000 V to 3.740 V
0.5	3.740 V to 5.500 V	1:1	0.000 V to 5.500 V

The minimum and maximum valid data values for VOUT_TRIM follow the description in VOUT_COMMAND . Attempts to write (22h) VOUT_TRIM to any value outside those specified as valid, will be considered invalid/ unsupported data and cause TPS536xx to respond by flagging the appropriate status bits, and notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

Writes to VOUT_TRIM for which the resulting output voltage is greater than the current VOUT_MAX , or less than the current VOUT_MIN , cause the reference DAC to move to the value specified by VOUT_MIN or VOUT_MAX respectively. No status bits will be set.

1.2.24 (24h) VOUT_MAX

CMD Address	24h
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	ULINEAR16, Absolute
Paged:	Yes
Phased:	No
NVM Back-up:	EEPROM
Updates:	On-the-fly. Disable power conversion to change between DAC ranges.

The VOUT_MAX command sets an upper limit on the output voltage the unit can command regardless of any other commands or combinations. The intent of this command is to provide a safeguard against a user accidentally setting the output voltage to a possibly destructive level. If the host attempts to program the output voltage above this limit, the output voltage moves to the VOUT_MAX value, and stops.

During power conversion, setting the VOUT_MAX less than the current VOUT_COMMAND does not cause the output voltage to change immediately, though it take effect automatically if a new target is received or a phase/add/drop event occurs.

(24h) VOUT_MAX Register Map

15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
VOUT MAX (High Byte)							
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VOUT MAX (Low Byte)							

LEGEND: R/W = Read/Write; R = Read only

Table 1-21. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:0	VOUT MAX	RW	NVM	Maximum output voltage. ULINEAR16 format. Refer to the description below for data validity.

Reset behavior

When the MFR_SPECIFIC_EE (PIN_DETECT_OVERRIDE) command indicates that the channel A boot voltage is determined by NVM, the VOUT_MAX will be restored from the corresponding NVM location. When the MFR_SPECIFIC_EE (PIN_DETECT_OVERRIDE) command indicates that the channel A boot voltage is determined by pin detection, the VOUT_MAX value is determined according to the table below.

Table 1-22. VOUT_MAX reset value when using pinstrap for VBOOT

VBOOT pinstrap value	VOUT_SCALE_LOOP	VOUT_MAX reset value
0.00 to 1.870 V	1.00	1.870 V
1.880 to 2.770 V	1.00	3.740 V
3.300 V	1.00	5.50 V
5.000 V	0.50	5.50 V

Data Validity

Due to internal limitations of the TPS536xx reference DAC, which uses the value of VOUT_MAX to select one of two ranges corresponding to range and resolution, any change to VOUT_MAX made during power conversion

must not cause the reference DAC to change range. The boundary point is 1.870 V. When TPS536xx is not converting power, VOUT_MAX may be programmed to any supported value.

Whenever possible TI recommends to use the lowest DAC range, corresponding to VOUT_MAX ≤ 1.87 V. This maximizes the signal level present to internal circuits of the device.

Table 1-23. VOUT_MAX data validity (during power conversion)

Power Conversion Active	VOUT_SCALE_LOOP	External Divider	Minimum	Maximum
Yes	1.0	None	0.000 V	1.870 V
Yes	1.0	None	0.000 V	3.740 V
Yes	0.5	2:1	0.000 V	5.500 V
No	X	None	0.000 V	5.500 V

Attempts to write (24h) VOUT_MAX to any value outside those specified as valid, will be considered invalid/unsupported data and cause TPS536xx to respond by flagging the appropriate status bits, and notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

1.2.25 (25h) VOUT_MARGIN_HIGH

CMD Address	25h
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	ULINEAR16, Absolute
Paged:	Yes
Phased:	No
NVM Back-up:	No
Updates:	On-the-fly.

The VOUT_MARGIN_HIGH command loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to "Margin High." Output voltage transitions during margin operations occur at the slew rate defined by VOUT_TRANSITION_RATE .

When the MARGIN bits in the OPERATION command indicate "Margin High," the output voltage is updated to the value of VOUT_MARGIN_HIGH + VOUT_TRIM .

(25h) VOUT_MARGIN_HIGH Register Map

15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
VOUT MARGH (High Byte)							
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VOUT MARGH (Low Byte)							

LEGEND: R/W = Read/Write; R = Read only

Table 1-24. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:0	VOUT MARGH	RW	00h	Margin High output voltage. ULINEAR16 absolute per the setting of VOUT_MODE.

The minimum and maximum valid data values for VOUT_MARGIN_HIGH follow the description in VOUT_COMMAND . That is, the total combined output voltage, including VOUT_MARGIN_HIGH and VOUT_TRIM , follow the values allowed by the current VOUT_MAX setting.

Attempts to write (25h) VOUT_MARGIN_HIGH to any value outside those specified as valid, will be considered invalid/unsupported data and cause TPS536xx to respond by flagging the appropriate status bits, and notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

1.2.26 (26h) VOUT_MARGIN_LOW

CMD Address	26h
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	ULINEAR16, Absolute
Paged:	Yes
Phased:	No
NVM Back-up:	No
Updates:	On-the-fly.

The VOUT_MARGIN_LOW command loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to "Margin Low." Output voltage transitions during margin operation occur at the slew rate defined by VOUT_TRANSITION_RATE .

When the MARGIN bits in the OPERATION command indicate "Margin Low," the output voltage is updated to the value of VOUT_MARGIN_LOW + VOUT_TRIM.

(26h) VOUT_MARGIN_LOW Register Map

15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
VOUT MARGL (High Byte)							
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VOUT MARGL (Low Byte)							

LEGEND: R/W = Read/Write; R = Read only

Table 1-25. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:0	VOUT MARGL	RW	00h	Margin Low output voltage. ULINEAR16 absolute per the setting of VOUT_MODE .

The minimum and maximum valid data values for VOUT_MARGIN_LOW follow the description in VOUT_COMMAND . Attempts to write (26h) VOUT_MARGIN_LOW to any value outside those specified as valid, will be considered invalid/unsupported data and cause TPS536xx to respond by flagging the appropriate status bits, and notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

1.2.27 (27h) VOUT_TRANSITION_RATE

CMD Address	27h
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	SLINEAR11
Paged:	Yes
Phased:	No
NVM Back-up:	Yes
Updates:	On-the-fly

The VOUT_TRANSITION_RATE sets the slew rate at which any output voltage changes during normal power conversion occur, excluding turn-on or turn-off. The units are mV/us.

The output voltage transition rate may be updated via AVSBus when AVSBus controls the output voltage. Another option in MFR_SPECIFIC_ED (MISC_OPTIONS) VOTR DOWN CHx provides the anility to use a different slew rate for rising and falling transitions.

(27h) VOUT_TRANSITION_RATE Register Map

15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
VOTR EXP					VOTR MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VOTR MAN							

LEGEND: R/W = Read/Write; R = Read only

Table 1-26. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:11	VOTR EXP	RW	11100b	Linear format two's complement exponent. Exponent = -4, LSB = 0.0625 mV/µs.
10:0	VOTR MAN	RW	NVM	Linear format two's complement mantissa. See the table below. Note, the value programmed in this register specifies the **MINIMUM** transition rate across corners, the actual target slew rate is slightly higher to compensate.

Per the TPS536xx product specification, the following slew rates are supported (see the table below). Note that every binary value between the minimum and maximum values is writeable, and readable, but that the actual output voltage range slew rate is set to the nearest supported value.

Table 1-27. Supported VOUT_TRANSITION_RATE values

VOUT_TRANSITION_RATE (decoded)	Minimum output voltage slew rate (mV/µs)	Nominal SLINEAR11 value (hex)
VOTR < 0.3125	Invalid/Unsupported	Invalid/Unsupported
0.3125 ≤ VOTR < 0.46875 mV/µs	0.3125	E005h
0.46875 ≤ VOTR < 0.78125 mV/µs	0.625	E00Ah
0.78125 ≤ VOTR < 1.09375 mV/µs	0.9375	E00Fh
1.09375 ≤ VOTR < 1.40625 mV/µs	1.25	E014h
1.40625 ≤ VOTR < 1.71875 mV/µs	1.5625	E019h
1.71875 ≤ VOTR < 2.03125 mV/µs	1.875	E01Eh
2.03125 ≤ VOTR < 2.34375 mV/µs	2.1875	E023h
2.34375 ≤ VOTR < 3.75 mV/µs	2.5	E028h
3.75 ≤ VOTR < 7.5 mV/µs	5	E050h

Table 1-27. Supported VOUT_TRANSITION_RATE values (continued)

VOUT_TRANSITION_RATE (decoded)	Minimum output voltage slew rate (mV/µs)	Nominal SLINEAR11 value (hex)
7.5 ≤ VOTR < 12.5 mV/µs	10	E0A0h
12.5 ≤ VOTR < 17.5 mV/µs	15	E0F0h
17.5 ≤ VOTR < 22.5 mV/µs	20	E140h
22.5 ≤ VOTR < 27.5 mV/µs	25	E190h
27.5 ≤ VOTR < 32.5 mV/µs	30	E1E0h
32.5 ≤ VOTR < 37.5 mV/µs	35	E230h
37.5 ≤ VOTR ≤ 40 mV/µs	40	E280h
VOTR > 40 mV/µs	Invalid/Unsupported	Invalid/Unsupported

Attempts to write (27h) VOUT_TRANSITION_RATE to any value outside those specified as valid, will be considered invalid/unsupported data and cause TPS536xx to respond by flagging the appropriate status bits, and notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

1.2.28 (28h) VOUT_DROOP

CMD Address	28h
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	SLINEAR11
Paged:	Yes
Phased:	No
Updates:	on-the-fly
NVM Back-up:	EEPROM

The VOUT_DROOP command sets the rate, in mV/A (mΩ) at which the output voltage decreases (or increases) with increasing (or decreasing) output current for use with adaptive voltage positioning. This may also referred to as the DC Load Line (DCLL).

(28h) VOUT_DROOP Register Map

15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
VDROOP EXP					VDROOP MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VDROOP MAN							

LEGEND: R/W = Read/Write; R = Read only

Table 1-28. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:11	VDROOP EXP	RW	11001b	Linear format two's complement exponent. N = -7
10:0	VDROOP MAN	RW	NVM	Linear format two's complement mantissa.

Table 1-29. Supported Values

VOUT_DROOP (decoded)	Effective DC LoadLine (mΩ)	Nominal SLINEAR11 (hex)
0 mΩ ≤ VDROOP < 0.00390625 mΩ	0.0000000	B800h
0.00390625 mΩ ≤ VDROOP < 0.01171875 mΩ	0.0078125	C801h
0.01171875 mΩ ≤ VDROOP < 0.01953125 mΩ	0.0156250	C802h
0.01953125 mΩ ≤ VDROOP < 0.02734375 mΩ	0.0234375	C803h
0.02734375 mΩ ≤ VDROOP < 0.03515625 mΩ	0.0312500	C804h
0.03515625 mΩ ≤ VDROOP < 0.04296875 mΩ	0.0390625	C805h
0.04296875 mΩ ≤ VDROOP < 0.05078125 mΩ	0.0468750	C806h
0.05078125 mΩ ≤ VDROOP < 0.05859375 mΩ	0.0546875	C807h
0.05859375 mΩ ≤ VDROOP < 0.06640625 mΩ	0.0625000	C808h
0.06640625 mΩ ≤ VDROOP < 0.07421875 mΩ	0.0703125	C809h
0.07421875 mΩ ≤ VDROOP < 0.08203125 mΩ	0.0781250	C80Ah
0.08203125 mΩ ≤ VDROOP < 0.08984375 mΩ	0.0859375	C80Bh
0.08984375 mΩ ≤ VDROOP < 0.09765625 mΩ	0.0937500	C80Ch
0.09765625 mΩ ≤ VDROOP < 0.10546875 mΩ	0.1015625	C80Dh
0.10546875 mΩ ≤ VDROOP < 0.11328125 mΩ	0.1093750	C80Eh
0.11328125 mΩ ≤ VDROOP < 0.12109375 mΩ	0.1171875	C80Fh

Table 1-29. Supported Values (continued)

VOUT_DROOP (decoded)	Effective DC LoadLine (mΩ)	Nominal SLINEAR11 (hex)
0.12109375 mΩ ≤ VDROOP < 0.12890625 mΩ	0.1250000	C810h
0.12890625 mΩ ≤ VDROOP < 0.13671875 mΩ	0.1328125	C811h
0.13671875 mΩ ≤ VDROOP < 0.14453125 mΩ	0.1406250	C812h
0.14453125 mΩ ≤ VDROOP < 0.15234375 mΩ	0.1484375	C813h
0.15234375 mΩ ≤ VDROOP < 0.16015625 mΩ	0.1562500	C814h
0.16015625 mΩ ≤ VDROOP < 0.16796875 mΩ	0.1640625	C815h
0.16796875 mΩ ≤ VDROOP < 0.17578125 mΩ	0.1718750	C816h
0.17578125 mΩ ≤ VDROOP < 0.18359375 mΩ	0.1796875	C817h
0.18359375 mΩ ≤ VDROOP < 0.19140625 mΩ	0.1875000	C818h
0.19140625 mΩ ≤ VDROOP < 0.19921875 mΩ	0.1953125	C819h
0.19921875 mΩ ≤ VDROOP < 0.20703125 mΩ	0.2031250	C81Ah
0.20703125 mΩ ≤ VDROOP < 0.21484375 mΩ	0.2109375	C81Bh
0.21484375 mΩ ≤ VDROOP < 0.22265625 mΩ	0.2187500	C81Ch
0.22265625 mΩ ≤ VDROOP < 0.23046875 mΩ	0.2265625	C81Dh
0.23046875 mΩ ≤ VDROOP < 0.23828125 mΩ	0.2343750	C81Eh
0.23828125 mΩ ≤ VDROOP < 0.24609375 mΩ	0.2421875	C81Fh
0.24609375 mΩ ≤ VDROOP < 0.25390625 mΩ	0.2500000	C820h
0.25390625 mΩ ≤ VDROOP < 0.26171875 mΩ	0.2578125	C821h
0.26171875 mΩ ≤ VDROOP < 0.26953125 mΩ	0.2656250	C822h
0.26953125 mΩ ≤ VDROOP < 0.27734375 mΩ	0.2734375	C823h
0.27734375 mΩ ≤ VDROOP < 0.28515625 mΩ	0.2812500	C824h
0.28515625 mΩ ≤ VDROOP < 0.29296875 mΩ	0.2890625	C825h
0.29296875 mΩ ≤ VDROOP < 0.30078125 mΩ	0.2968750	C826h
0.30078125 mΩ ≤ VDROOP < 0.30859375 mΩ	0.3046875	C827h
0.30859375 mΩ ≤ VDROOP < 0.31640625 mΩ	0.3125000	C828h
0.31640625 mΩ ≤ VDROOP < 0.32421875 mΩ	0.3203125	C829h
0.32421875 mΩ ≤ VDROOP < 0.33203125 mΩ	0.3281250	C82Ah
0.33203125 mΩ ≤ VDROOP < 0.33984375 mΩ	0.3359375	C82Bh
0.33984375 mΩ ≤ VDROOP < 0.34765625 mΩ	0.3437500	C82Ch
0.34765625 mΩ ≤ VDROOP < 0.35546875 mΩ	0.3515625	C82Dh
0.35546875 mΩ ≤ VDROOP < 0.36328125 mΩ	0.3593750	C82Eh
0.36328125 mΩ ≤ VDROOP < 0.37109375 mΩ	0.3671875	C82Fh
0.37109375 mΩ ≤ VDROOP < 0.37890625 mΩ	0.3750000	C830h
0.37890625 mΩ ≤ VDROOP < 0.38671875 mΩ	0.3828125	C831h
0.38671875 mΩ ≤ VDROOP < 0.39453125 mΩ	0.3906250	C832h
0.39453125 mΩ ≤ VDROOP < 0.40234375 mΩ	0.3984375	C833h
0.40234375 mΩ ≤ VDROOP < 0.41015625 mΩ	0.4062500	C834h
0.41015625 mΩ ≤ VDROOP < 0.41796875 mΩ	0.4140625	C835h
0.41796875 mΩ ≤ VDROOP < 0.42578125 mΩ	0.4218750	C836h
0.42578125 mΩ ≤ VDROOP < 0.43359375 mΩ	0.4296875	C837h
0.43359375 mΩ ≤ VDROOP < 0.44140625 mΩ	0.4375000	C838h
0.44140625 mΩ ≤ VDROOP < 0.44921875 mΩ	0.4453125	C839h
0.44921875 mΩ ≤ VDROOP < 0.45703125 mΩ	0.4531250	C83Ah
0.45703125 mΩ ≤ VDROOP < 0.46484375 mΩ	0.4609375	C83Bh
0.46484375 mΩ ≤ VDROOP < 0.47265625 mΩ	0.4687500	C83Ch

Table 1-29. Supported Values (continued)

VOUT_DROOP (decoded)	Effective DC LoadLine (mΩ)	Nominal SLINEAR11 (hex)
0.47265625 mΩ ≤ VDROOP < 0.48046875 mΩ	0.4765625	C83Dh
0.48046875 mΩ ≤ VDROOP < 0.48828125 mΩ	0.4843750	C83Eh
0.48828125 mΩ ≤ VDROOP < 0.49609375 mΩ	0.4921875	C83Fh
0.49609375 mΩ ≤ VDROOP < 0.50390625 mΩ	0.5000000	C840h
0.50390625 mΩ ≤ VDROOP < 0.51171875 mΩ	0.5078125	C841h
0.51171875 mΩ ≤ VDROOP < 0.51953125 mΩ	0.5156250	C842h
0.51953125 mΩ ≤ VDROOP < 0.52734375 mΩ	0.5234375	C843h
0.52734375 mΩ ≤ VDROOP < 0.53515625 mΩ	0.5312500	C844h
0.53515625 mΩ ≤ VDROOP < 0.54296875 mΩ	0.5390625	C845h
0.54296875 mΩ ≤ VDROOP < 0.55078125 mΩ	0.5468750	C846h
0.55078125 mΩ ≤ VDROOP < 0.55859375 mΩ	0.5546875	C847h
0.55859375 mΩ ≤ VDROOP < 0.56640625 mΩ	0.5625000	C848h
0.56640625 mΩ ≤ VDROOP < 0.57421875 mΩ	0.5703125	C849h
0.57421875 mΩ ≤ VDROOP < 0.58203125 mΩ	0.5781250	C84Ah
0.58203125 mΩ ≤ VDROOP < 0.58984375 mΩ	0.5859375	C84Bh
0.58984375 mΩ ≤ VDROOP < 0.59765625 mΩ	0.5937500	C84Ch
0.59765625 mΩ ≤ VDROOP < 0.60546875 mΩ	0.6015625	C84Dh
0.60546875 mΩ ≤ VDROOP < 0.61328125 mΩ	0.6093750	C84Eh
0.61328125 mΩ ≤ VDROOP < 0.62109375 mΩ	0.6171875	C84Fh
0.62109375 mΩ ≤ VDROOP < 0.62890625 mΩ	0.6250000	C850h
0.62890625 mΩ ≤ VDROOP < 0.63671875 mΩ	0.6328125	C851h
0.63671875 mΩ ≤ VDROOP < 0.64453125 mΩ	0.6406250	C852h
0.64453125 mΩ ≤ VDROOP < 0.65234375 mΩ	0.6484375	C853h
0.65234375 mΩ ≤ VDROOP < 0.66015625 mΩ	0.6562500	C854h
0.66015625 mΩ ≤ VDROOP < 0.66796875 mΩ	0.6640625	C855h
0.66796875 mΩ ≤ VDROOP < 0.67578125 mΩ	0.6718750	C856h
0.67578125 mΩ ≤ VDROOP < 0.68359375 mΩ	0.6796875	C857h
0.68359375 mΩ ≤ VDROOP < 0.69140625 mΩ	0.6875000	C858h
0.69140625 mΩ ≤ VDROOP < 0.69921875 mΩ	0.6953125	C859h
0.69921875 mΩ ≤ VDROOP < 0.70703125 mΩ	0.7031250	C85Ah
0.70703125 mΩ ≤ VDROOP < 0.71484375 mΩ	0.7109375	C85Bh
0.71484375 mΩ ≤ VDROOP < 0.72265625 mΩ	0.7187500	C85Ch
0.72265625 mΩ ≤ VDROOP < 0.73046875 mΩ	0.7265625	C85Dh
0.73046875 mΩ ≤ VDROOP < 0.73828125 mΩ	0.7343750	C85Eh
0.73828125 mΩ ≤ VDROOP < 0.74609375 mΩ	0.7421875	C85Fh
0.74609375 mΩ ≤ VDROOP < 0.75390625 mΩ	0.7500000	C860h
0.75390625 mΩ ≤ VDROOP < 0.76171875 mΩ	0.7578125	C861h
0.76171875 mΩ ≤ VDROOP < 0.76953125 mΩ	0.7656250	C862h
0.76953125 mΩ ≤ VDROOP < 0.77734375 mΩ	0.7734375	C863h
0.77734375 mΩ ≤ VDROOP < 0.78515625 mΩ	0.7812500	C864h
0.78515625 mΩ ≤ VDROOP < 0.79296875 mΩ	0.7890625	C865h
0.79296875 mΩ ≤ VDROOP < 0.80078125 mΩ	0.7968750	C866h
0.80078125 mΩ ≤ VDROOP < 0.80859375 mΩ	0.8046875	C867h
0.80859375 mΩ ≤ VDROOP < 0.81640625 mΩ	0.8125000	C868h
0.81640625 mΩ ≤ VDROOP < 0.82421875 mΩ	0.8203125	C869h

Table 1-29. Supported Values (continued)

VOUT_DROOP (decoded)	Effective DC LoadLine (mΩ)	Nominal SLINEAR11 (hex)
0.82421875 mΩ ≤ VDROOP < 0.83203125 mΩ	0.8281250	C86Ah
0.83203125 mΩ ≤ VDROOP < 0.83984375 mΩ	0.8359375	C86Bh
0.83984375 mΩ ≤ VDROOP < 0.84765625 mΩ	0.8437500	C86Ch
0.84765625 mΩ ≤ VDROOP < 0.85546875 mΩ	0.8515625	C86Dh
0.85546875 mΩ ≤ VDROOP < 0.86328125 mΩ	0.8593750	C86Eh
0.86328125 mΩ ≤ VDROOP < 0.87109375 mΩ	0.8671875	C86Fh
0.87109375 mΩ ≤ VDROOP < 0.87890625 mΩ	0.8750000	C870h
0.87890625 mΩ ≤ VDROOP < 0.88671875 mΩ	0.8828125	C871h
0.88671875 mΩ ≤ VDROOP < 0.89453125 mΩ	0.8906250	C872h
0.89453125 mΩ ≤ VDROOP < 0.90234375 mΩ	0.8984375	C873h
0.90234375 mΩ ≤ VDROOP < 0.91015625 mΩ	0.9062500	C874h
0.91015625 mΩ ≤ VDROOP < 0.91796875 mΩ	0.9140625	C875h
0.91796875 mΩ ≤ VDROOP < 0.92578125 mΩ	0.9218750	C876h
0.92578125 mΩ ≤ VDROOP < 0.93359375 mΩ	0.9296875	C877h
0.93359375 mΩ ≤ VDROOP < 0.94140625 mΩ	0.9375000	C878h
0.94140625 mΩ ≤ VDROOP < 0.94921875 mΩ	0.9453125	C879h
0.94921875 mΩ ≤ VDROOP < 0.95703125 mΩ	0.9531250	C87Ah
0.95703125 mΩ ≤ VDROOP < 0.96484375 mΩ	0.9609375	C87Bh
0.96484375 mΩ ≤ VDROOP < 0.97265625 mΩ	0.9687500	C87Ch
0.97265625 mΩ ≤ VDROOP < 0.98046875 mΩ	0.9765625	C87Dh
0.98046875 mΩ ≤ VDROOP < 0.98828125 mΩ	0.9843750	C87Eh
0.98828125 mΩ ≤ VDROOP < 0.99609375 mΩ	0.9921875	C87Fh
0.99609375 mΩ ≤ VDROOP < 1.0078125 mΩ	1.0000000	C880h
1.0078125 mΩ ≤ VDROOP < 1.0234375 mΩ	1.0156250	C882h
1.0234375 mΩ ≤ VDROOP < 1.0390625 mΩ	1.0312500	C884h
1.0390625 mΩ ≤ VDROOP < 1.0546875 mΩ	1.0468750	C886h
1.0546875 mΩ ≤ VDROOP < 1.0703125 mΩ	1.0625000	C888h
1.0703125 mΩ ≤ VDROOP < 1.0859375 mΩ	1.0781250	C88Ah
1.0859375 mΩ ≤ VDROOP < 1.1015625 mΩ	1.0937500	C88Ch
1.1015625 mΩ ≤ VDROOP < 1.1171875 mΩ	1.1093750	C88Eh
1.1171875 mΩ ≤ VDROOP < 1.1328125 mΩ	1.1250000	C890h
1.1328125 mΩ ≤ VDROOP < 1.1484375 mΩ	1.1406250	C892h
1.1484375 mΩ ≤ VDROOP < 1.1640625 mΩ	1.1562500	C894h
1.1640625 mΩ ≤ VDROOP < 1.1796875 mΩ	1.1718750	C896h
1.1796875 mΩ ≤ VDROOP < 1.1953125 mΩ	1.1875000	C898h
1.1953125 mΩ ≤ VDROOP < 1.2109375 mΩ	1.2031250	C89Ah
1.2109375 mΩ ≤ VDROOP < 1.2265625 mΩ	1.2187500	C89Ch
1.2265625 mΩ ≤ VDROOP < 1.2421875 mΩ	1.2343750	C89Eh
1.2421875 mΩ ≤ VDROOP < 1.2578125 mΩ	1.2500000	C8A0h
1.2578125 mΩ ≤ VDROOP < 1.2734375 mΩ	1.2656250	C8A2h
1.2734375 mΩ ≤ VDROOP < 1.2890625 mΩ	1.2812500	C8A4h
1.2890625 mΩ ≤ VDROOP < 1.3046875 mΩ	1.2968750	C8A6h
1.3046875 mΩ ≤ VDROOP < 1.3203125 mΩ	1.3125000	C8A8h
1.3203125 mΩ ≤ VDROOP < 1.3359375 mΩ	1.3281250	C8AAh
1.3359375 mΩ ≤ VDROOP < 1.3515625 mΩ	1.3437500	C8ACh

Table 1-29. Supported Values (continued)

VOUT_DROOP (decoded)	Effective DC LoadLine (mΩ)	Nominal SLINEAR11 (hex)
1.3515625 mΩ ≤ VDROOP < 1.3671875 mΩ	1.3593750	C8AEh
1.3671875 mΩ ≤ VDROOP < 1.3828125 mΩ	1.3750000	C8B0h
1.3828125 mΩ ≤ VDROOP < 1.3984375 mΩ	1.3906250	C8B2h
1.3984375 mΩ ≤ VDROOP < 1.4140625 mΩ	1.4062500	C8B4h
1.4140625 mΩ ≤ VDROOP < 1.4296875 mΩ	1.4218750	C8B6h
1.4296875 mΩ ≤ VDROOP < 1.4453125 mΩ	1.4375000	C8B8h
1.4453125 mΩ ≤ VDROOP < 1.4609375 mΩ	1.4531250	C8BAh
1.4609375 mΩ ≤ VDROOP < 1.4765625 mΩ	1.4687500	C8BCh
1.4765625 mΩ ≤ VDROOP < 1.4921875 mΩ	1.4843750	C8BEh
1.4921875 mΩ ≤ VDROOP < 1.5078125 mΩ	1.5000000	C8C0h
1.5078125 mΩ ≤ VDROOP < 1.5234375 mΩ	1.5156250	C8C2h
1.5234375 mΩ ≤ VDROOP < 1.5390625 mΩ	1.5312500	C8C4h
1.5390625 mΩ ≤ VDROOP < 1.5546875 mΩ	1.5468750	C8C6h
1.5546875 mΩ ≤ VDROOP < 1.5703125 mΩ	1.5625000	C8C8h
1.5703125 mΩ ≤ VDROOP < 1.5859375 mΩ	1.5781250	C8CAh
1.5859375 mΩ ≤ VDROOP < 1.6015625 mΩ	1.5937500	C8CCh
1.6015625 mΩ ≤ VDROOP < 1.6171875 mΩ	1.6093750	C8CEh
1.6171875 mΩ ≤ VDROOP < 1.6328125 mΩ	1.6250000	C8D0h
1.6328125 mΩ ≤ VDROOP < 1.6484375 mΩ	1.6406250	C8D2h
1.6484375 mΩ ≤ VDROOP < 1.6640625 mΩ	1.6562500	C8D4h
1.6640625 mΩ ≤ VDROOP < 1.6796875 mΩ	1.6718750	C8D6h
1.6796875 mΩ ≤ VDROOP < 1.6953125 mΩ	1.6875000	C8D8h
1.6953125 mΩ ≤ VDROOP < 1.7109375 mΩ	1.7031250	C8DAh
1.7109375 mΩ ≤ VDROOP < 1.7265625 mΩ	1.7187500	C8DCh
1.7265625 mΩ ≤ VDROOP < 1.7421875 mΩ	1.7343750	C8DEh
1.7421875 mΩ ≤ VDROOP < 1.7578125 mΩ	1.7500000	C8E0h
1.7578125 mΩ ≤ VDROOP < 1.7734375 mΩ	1.7656250	C8E2h
1.7734375 mΩ ≤ VDROOP < 1.7890625 mΩ	1.7812500	C8E4h
1.7890625 mΩ ≤ VDROOP < 1.8046875 mΩ	1.7968750	C8E6h
1.8046875 mΩ ≤ VDROOP < 1.8203125 mΩ	1.8125000	C8E8h
1.8203125 mΩ ≤ VDROOP < 1.8359375 mΩ	1.8281250	C8EAh
1.8359375 mΩ ≤ VDROOP < 1.8515625 mΩ	1.8437500	C8ECh
1.8515625 mΩ ≤ VDROOP < 1.8671875 mΩ	1.8593750	C8EEh
1.8671875 mΩ ≤ VDROOP < 1.8828125 mΩ	1.8750000	C8F0h
1.8828125 mΩ ≤ VDROOP < 1.8984375 mΩ	1.8906250	C8F2h
1.8984375 mΩ ≤ VDROOP < 1.9140625 mΩ	1.9062500	C8F4h
1.9140625 mΩ ≤ VDROOP < 1.9296875 mΩ	1.9218750	C8F6h
1.9296875 mΩ ≤ VDROOP < 1.9453125 mΩ	1.9375000	C8F8h
1.9453125 mΩ ≤ VDROOP < 1.9609375 mΩ	1.9531250	C8FAh
1.9609375 mΩ ≤ VDROOP < 1.9765625 mΩ	1.9687500	C8FCh
1.9765625 mΩ ≤ VDROOP < 1.9921875 mΩ	1.9843750	C8FEh
1.9921875 mΩ ≤ VDROOP < 2.015625 mΩ	2.0000000	C900h
2.015625 mΩ ≤ VDROOP < 2.046875 mΩ	2.0312500	C904h
2.046875 mΩ ≤ VDROOP < 2.078125 mΩ	2.0625000	C908h
2.078125 mΩ ≤ VDROOP < 2.109375 mΩ	2.0937500	C90Ch

Table 1-29. Supported Values (continued)

VOUT_DROOP (decoded)	Effective DC LoadLine (mΩ)	Nominal SLINEAR11 (hex)
2.109375 mΩ ≤ VDROOP < 2.140625 mΩ	2.1250000	C910h
2.140625 mΩ ≤ VDROOP < 2.171875 mΩ	2.1562500	C914h
2.171875 mΩ ≤ VDROOP < 2.203125 mΩ	2.1875000	C918h
2.203125 mΩ ≤ VDROOP < 2.234375 mΩ	2.2187500	C91Ch
2.234375 mΩ ≤ VDROOP < 2.265625 mΩ	2.2500000	C920h
2.265625 mΩ ≤ VDROOP < 2.296875 mΩ	2.2812500	C924h
2.296875 mΩ ≤ VDROOP < 2.328125 mΩ	2.3125000	C928h
2.328125 mΩ ≤ VDROOP < 2.359375 mΩ	2.3437500	C92Ch
2.359375 mΩ ≤ VDROOP < 2.390625 mΩ	2.3750000	C930h
2.390625 mΩ ≤ VDROOP < 2.421875 mΩ	2.4062500	C934h
2.421875 mΩ ≤ VDROOP < 2.453125 mΩ	2.4375000	C938h
2.453125 mΩ ≤ VDROOP < 2.484375 mΩ	2.4687500	C93Ch
2.484375 mΩ ≤ VDROOP < 2.515625 mΩ	2.5000000	C940h
2.515625 mΩ ≤ VDROOP < 2.546875 mΩ	2.5312500	C944h
2.546875 mΩ ≤ VDROOP < 2.578125 mΩ	2.5625000	C948h
2.578125 mΩ ≤ VDROOP < 2.609375 mΩ	2.5937500	C94Ch
2.609375 mΩ ≤ VDROOP < 2.640625 mΩ	2.6250000	C950h
2.640625 mΩ ≤ VDROOP < 2.671875 mΩ	2.6562500	C954h
2.671875 mΩ ≤ VDROOP < 2.703125 mΩ	2.6875000	C958h
2.703125 mΩ ≤ VDROOP < 2.734375 mΩ	2.7187500	C95Ch
2.734375 mΩ ≤ VDROOP < 2.765625 mΩ	2.7500000	C960h
2.765625 mΩ ≤ VDROOP < 2.796875 mΩ	2.7812500	C964h
2.796875 mΩ ≤ VDROOP < 2.828125 mΩ	2.8125000	C968h
2.828125 mΩ ≤ VDROOP < 2.859375 mΩ	2.8437500	C96Ch
2.859375 mΩ ≤ VDROOP < 2.890625 mΩ	2.8750000	C970h
2.890625 mΩ ≤ VDROOP < 2.921875 mΩ	2.9062500	C974h
2.921875 mΩ ≤ VDROOP < 2.953125 mΩ	2.9375000	C978h
2.953125 mΩ ≤ VDROOP < 2.984375 mΩ	2.9687500	C97Ch
2.984375 mΩ ≤ VDROOP < 3.015625 mΩ	3.0000000	C980h
3.015625 mΩ ≤ VDROOP < 3.046875 mΩ	3.0312500	C984h
3.046875 mΩ ≤ VDROOP < 3.078125 mΩ	3.0625000	C988h
3.078125 mΩ ≤ VDROOP < 3.109375 mΩ	3.0937500	C98Ch
3.109375 mΩ ≤ VDROOP < 3.140625 mΩ	3.1250000	C990h
3.140625 mΩ ≤ VDROOP < 3.171875 mΩ	3.1562500	C994h
3.171875 mΩ ≤ VDROOP < 3.203125 mΩ	3.1875000	C998h
3.203125 mΩ ≤ VDROOP < 3.234375 mΩ	3.2187500	C99Ch
3.234375 mΩ ≤ VDROOP < 3.265625 mΩ	3.2500000	C9A0h
3.265625 mΩ ≤ VDROOP < 3.296875 mΩ	3.2812500	C9A4h
3.296875 mΩ ≤ VDROOP < 3.328125 mΩ	3.3125000	C9A8h
3.328125 mΩ ≤ VDROOP < 3.359375 mΩ	3.3437500	C9ACh
3.359375 mΩ ≤ VDROOP < 3.390625 mΩ	3.3750000	C9B0h
3.390625 mΩ ≤ VDROOP < 3.421875 mΩ	3.4062500	C9B4h
3.421875 mΩ ≤ VDROOP < 3.453125 mΩ	3.4375000	C9B8h
3.453125 mΩ ≤ VDROOP < 3.484375 mΩ	3.4687500	C9BCh
3.484375 mΩ ≤ VDROOP < 3.515625 mΩ	3.5000000	C9C0h

Table 1-29. Supported Values (continued)

VOUT_DROOP (decoded)	Effective DC LoadLine (mΩ)	Nominal SLINEAR11 (hex)
3.515625 mΩ ≤ VDROOP < 3.546875 mΩ	3.5312500	C9C4h
3.546875 mΩ ≤ VDROOP < 3.578125 mΩ	3.5625000	C9C8h
3.578125 mΩ ≤ VDROOP < 3.609375 mΩ	3.5937500	C9CCh
3.609375 mΩ ≤ VDROOP < 3.640625 mΩ	3.6250000	C9D0h
3.640625 mΩ ≤ VDROOP < 3.671875 mΩ	3.6562500	C9D4h
3.671875 mΩ ≤ VDROOP < 3.703125 mΩ	3.6875000	C9D8h
3.703125 mΩ ≤ VDROOP < 3.734375 mΩ	3.7187500	C9DCh
3.734375 mΩ ≤ VDROOP < 3.765625 mΩ	3.7500000	C9E0h
3.765625 mΩ ≤ VDROOP < 3.796875 mΩ	3.7812500	C9E4h
3.796875 mΩ ≤ VDROOP < 3.828125 mΩ	3.8125000	C9E8h
3.828125 mΩ ≤ VDROOP < 3.859375 mΩ	3.8437500	C9ECh
3.859375 mΩ ≤ VDROOP < 3.890625 mΩ	3.8750000	C9F0h
3.890625 mΩ ≤ VDROOP < 3.921875 mΩ	3.9062500	C9F4h
3.921875 mΩ ≤ VDROOP < 3.953125 mΩ	3.9375000	C9F8h
3.953125 mΩ ≤ VDROOP < 3.984375 mΩ	3.9687500	C9FCh
3.984375 mΩ ≤ VDROOP < 4.03125 mΩ	4.0000000	CA00h
4.03125 mΩ ≤ VDROOP < 4.09375 mΩ	4.0625000	CA08h
4.09375 mΩ ≤ VDROOP < 4.15625 mΩ	4.1250000	CA10h
4.15625 mΩ ≤ VDROOP < 4.21875 mΩ	4.1875000	CA18h
4.21875 mΩ ≤ VDROOP < 4.28125 mΩ	4.2500000	CA20h
4.28125 mΩ ≤ VDROOP < 4.34375 mΩ	4.3125000	CA28h
4.34375 mΩ ≤ VDROOP < 4.40625 mΩ	4.3750000	CA30h
4.40625 mΩ ≤ VDROOP < 4.46875 mΩ	4.4375000	CA38h
4.46875 mΩ ≤ VDROOP < 4.53125 mΩ	4.5000000	CA40h
4.53125 mΩ ≤ VDROOP < 4.59375 mΩ	4.5625000	CA48h
4.59375 mΩ ≤ VDROOP < 4.65625 mΩ	4.6250000	CA50h
4.65625 mΩ ≤ VDROOP < 4.71875 mΩ	4.6875000	CA58h
4.71875 mΩ ≤ VDROOP < 4.78125 mΩ	4.7500000	CA60h
4.78125 mΩ ≤ VDROOP < 4.84375 mΩ	4.8125000	CA68h
4.84375 mΩ ≤ VDROOP < 4.90625 mΩ	4.8750000	CA70h
4.90625 mΩ ≤ VDROOP < 4.96875 mΩ	4.9375000	CA78h
4.96875 mΩ ≤ VDROOP < 5.03125 mΩ	5.0000000	CA80h
5.03125 mΩ ≤ VDROOP < 5.09375 mΩ	5.0625000	CA88h
5.09375 mΩ ≤ VDROOP < 5.15625 mΩ	5.1250000	CA90h
5.15625 mΩ ≤ VDROOP < 5.21875 mΩ	5.1875000	CA98h
5.21875 mΩ ≤ VDROOP < 5.28125 mΩ	5.2500000	CAA0h
5.28125 mΩ ≤ VDROOP < 5.34375 mΩ	5.3125000	CAA8h
5.34375 mΩ ≤ VDROOP < 5.40625 mΩ	5.3750000	CAB0h
5.40625 mΩ ≤ VDROOP < 5.46875 mΩ	5.4375000	CAB8h
5.46875 mΩ ≤ VDROOP < 5.53125 mΩ	5.5000000	CAC0h
5.53125 mΩ ≤ VDROOP < 5.59375 mΩ	5.5625000	CAC8h
5.59375 mΩ ≤ VDROOP < 5.65625 mΩ	5.6250000	CAD0h
5.65625 mΩ ≤ VDROOP < 5.71875 mΩ	5.6875000	CAD8h
5.71875 mΩ ≤ VDROOP < 5.78125 mΩ	5.7500000	CAE0h
5.78125 mΩ ≤ VDROOP < 5.84375 mΩ	5.8125000	CAE8h

Table 1-29. Supported Values (continued)

VOUT_DROOP (decoded)	Effective DC LoadLine (mΩ)	Nominal SLINEAR11 (hex)
5.84375 mΩ ≤ VDROOP < 5.90625 mΩ	5.8750000	CAF0h
5.90625 mΩ ≤ VDROOP < 5.96875 mΩ	5.9375000	CAF8h
5.96875 mΩ ≤ VDROOP < 6.03125 mΩ	6.0000000	CB00h
6.03125 mΩ ≤ VDROOP < 6.09375 mΩ	6.0625000	CB08h
6.09375 mΩ ≤ VDROOP < 6.15625 mΩ	6.1250000	CB10h
6.15625 mΩ ≤ VDROOP < 6.21875 mΩ	6.1875000	CB18h
6.21875 mΩ ≤ VDROOP < 6.28125 mΩ	6.2500000	CB20h
6.28125 mΩ ≤ VDROOP < 6.34375 mΩ	6.3125000	CB28h
6.34375 mΩ ≤ VDROOP < 6.40625 mΩ	6.3750000	CB30h
6.40625 mΩ ≤ VDROOP < 6.46875 mΩ	6.4375000	CB38h
6.46875 mΩ ≤ VDROOP < 6.53125 mΩ	6.5000000	CB40h
6.53125 mΩ ≤ VDROOP < 6.59375 mΩ	6.5625000	CB48h
6.59375 mΩ ≤ VDROOP < 6.65625 mΩ	6.6250000	CB50h
6.65625 mΩ ≤ VDROOP < 6.71875 mΩ	6.6875000	CB58h
6.71875 mΩ ≤ VDROOP < 6.78125 mΩ	6.7500000	CB60h
6.78125 mΩ ≤ VDROOP < 6.84375 mΩ	6.8125000	CB68h
6.84375 mΩ ≤ VDROOP < 6.90625 mΩ	6.8750000	CB70h
6.90625 mΩ ≤ VDROOP < 6.96875 mΩ	6.9375000	CB78h
6.96875 mΩ ≤ VDROOP < 7.03125 mΩ	7.0000000	CB80h
7.03125 mΩ ≤ VDROOP < 7.09375 mΩ	7.0625000	CB88h
7.09375 mΩ ≤ VDROOP < 7.15625 mΩ	7.1250000	CB90h
7.15625 mΩ ≤ VDROOP < 7.21875 mΩ	7.1875000	CB98h
7.21875 mΩ ≤ VDROOP < 7.28125 mΩ	7.2500000	CBA0h
7.28125 mΩ ≤ VDROOP < 7.34375 mΩ	7.3125000	CBA8h
7.34375 mΩ ≤ VDROOP < 7.40625 mΩ	7.3750000	CBB0h
7.40625 mΩ ≤ VDROOP < 7.46875 mΩ	7.4375000	CBB8h
7.46875 mΩ ≤ VDROOP < 7.53125 mΩ	7.5000000	CBC0h
7.53125 mΩ ≤ VDROOP < 7.59375 mΩ	7.5625000	CBC8h
7.59375 mΩ ≤ VDROOP < 7.65625 mΩ	7.6250000	CBD0h
7.65625 mΩ ≤ VDROOP < 7.71875 mΩ	7.6875000	CBD8h
7.71875 mΩ ≤ VDROOP < 7.78125 mΩ	7.7500000	CBE0h
7.78125 mΩ ≤ VDROOP < 7.84375 mΩ	7.8125000	CBE8h
7.84375 mΩ ≤ VDROOP < 7.90625 mΩ	7.8750000	CBF0h
7.90625 mΩ ≤ VDROOP < 7.96875 mΩ	7.9375000	CBF8h
7.96875 mΩ ≤ VDROOP ≤ 8 mΩ	8.0000000	D200h
VOUT_DROOP > 8 mΩ	Invalid/Unsupported	N/A

Attempts to write (28h) VOUT_DROOP to any value outside those specified as valid, will be considered invalid/unsupported data and cause TPS536xx to respond by flagging the appropriate status bits, and notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

1.2.29 (29h) VOUT_SCALE_LOOP

CMD Address	29h
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	SLINEAR11
Paged:	Yes
Phased:	No
Updates:	Updates accepted only with power conversion disabled.
NVM Back-up:	EEPROM

VOUT_SCALE_LOOP allows PMBus devices to map between the commanded voltage, and the voltage at the control circuit input.

(29h) VOUT_SCALE_LOOP Register Map

15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
VOSL EXP					VOSL MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VOSL MAN							

LEGEND: R/W = Read/Write; R = Read only

Table 1-30. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:11	VSOL EXP	RW	11101b	Linear format two's complement exponent.
10:0	VOSL MAN	RW	NVM	Linear format two's complement mantissa.

Data Validity:

Every binary value between the minimum and maximum supported values is writeable and readable. However not every combination is supported in hardware. Refer to the table below:

Table 1-31. Accepted values

VOUT_SCALE_LOOP (decoded)	Effective Scaling Factor	Nominal SLINEAR11 (hex)
Less than 0.500	Invalid/Unsupported data	Invalid/Unsupported data
0.500 ≤ VOSL < 0.750	0.5	E804h
0.750 ≤ VOSL ≤ 1.00	1.0	E808h
Greater than 1.00	Invalid/Unsupported data	Invalid/Unsupported data

Attempts to write (29h) VOUT_SCALE_LOOP to any value outside those specified as valid, will be considered invalid/unsupported data and cause TPS536xx to respond by flagging the appropriate status bits, and notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

Changing VOUT_SCALE_LOOP :

The VOUT_SCALE_LOOP may not be changed during power conversion.

When VOUT_SCALE_LOOP is changed while power conversion is disabled, the TPS536xx does not attempt to convert output voltage related commands in memory (e.g. VOUT_COMMAND , etc..) to support the new VOUT_SCALE_LOOP . It is the responsibility of the user to ensure that valid data is programmed based on desired value of VOUT_SCALE_LOOP . In most cases, this means programming VOUT_SCALE_LOOP before

any other output voltage related commands, then programming all output voltage related commands supported by the unit.

1.2.30 (2Bh) VOUT_MIN

CMD Address	2Bh
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	ULINEAR16
Paged:	Yes
Phased:	No
Updates:	on-the-fly
NVM Back-up:	EEPROM

The VOUT_MIN command sets a lower limit on the output voltage the unit can command regardless of any other commands or combinations. The intent of this command is to provide a safeguard against a user accidentally setting the output voltage to a level which will render the load inoperable. If the host attempts to program the output voltage less than this value, the output voltage moves to the VOUT_MIN value and stops.

During power conversion, setting the VOUT_MIN greater than the current VOUT_COMMAND does not cause the output voltage target to change immediately, although it will take effect if a new voltage target is received or if a phase add/drop event occurs.

(2Bh) VOUT_MIN Register Map

15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
VOUT MIN (High Byte)							
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VOUT MIN (Low Byte)							

LEGEND: R/W = Read/Write; R = Read only

Table 1-32. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:0	VOUT MIN	RW	NVM	Minimum output voltage. ULINEAR16 format.

Data Validity

The minimum and maximum valid data values for VOUT_MIN follow those of VOUT_MAX . Attempts to write (2Bh) VOUT_MIN to any value outside those specified as valid, will be considered invalid/unsupported data and cause TPS536xx to respond by flagging the appropriate status bits, and notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

1.2.31 (33h) FREQUENCY_SWITCH

CMD Address	33h
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	SLINEAR11
Paged:	Yes
Phased:	No
Updates:	on-the-fly
NVM Back-up:	EEPROM

FREQUENCY_SWITCH sets the switching frequency of the active channel, in kHz.

(33h) FREQUENCY_SWITCH Register Map

15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
FSW EXP					FSW MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
FSW MAN							

LEGEND: R/W = Read/Write; R = Read only

Table 1-33. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:11	FSW EXP	RW	00000b	Linear format two's complement exponent. Exponent = 0, LSB = 1 kHz.
10:0	FSW MAN	RW	NVM	Linear format two's complement mantissa. Refer to the table below.

Table 1-34. Supported Switching Frequency Settings

FREQUENCY_SWITCH (decoded)	Effective Switching Frequency (kHz)	Nominal SLINEAR11 (hex)
Less than 300 kHz	Invalid/Unsupported	Invalid/Unsupported
300 ≤ FSW < 325 kHz	300	012Ch
325 ≤ FSW < 375 kHz	350	015Eh
375 ≤ FSW < 425 kHz	400	0190h
425 ≤ FSW < 475 kHz	450	01C2h
475 ≤ FSW < 525 kHz	500	01F4h
525 ≤ FSW < 575 kHz	550	0226h
575 ≤ FSW < 625 kHz	600	0258h
625 ≤ FSW < 675 kHz	650	028Ah
675 ≤ FSW < 725 kHz	700	02BCh
725 ≤ FSW < 775 kHz	750	02EEh
775 ≤ FSW < 825 kHz	800	0320h
825 ≤ FSW < 875 kHz	850	0352h
875 ≤ FSW < 950 kHz	900	0384h
950 ≤ FSW < 1025 kHz	1000	03E8h
1025 ≤ FSW < 1075 kHz	1050	0A0Dh
1075 ≤ FSW < 1125 kHz	1100	0A26h
1125 ≤ FSW < 1175 kHz	1150	0A3Fh
1175 ≤ FSW < 1225 kHz	1200	0A58h
1225 ≤ FSW < 1275 kHz	1250	0A71h

Table 1-34. Supported Switching Frequency Settings (continued)

FREQUENCY_SWITCH (decoded)	Effective Switching Frequency (kHz)	Nominal SLINEAR11 (hex)
1275 ≤ FSW < 1325 kHz	1300	0A8Ah
1325 ≤ FSW < 1375 kHz	1350	0AA3h
1375 ≤ FSW < 1425 kHz	1400	0ABCh
1425 ≤ FSW < 1475 kHz	1450	0AD5h
1475 ≤ FSW < 1525 kHz	1500	0AEEh
1525 ≤ FSW < 1575 kHz	1550	0B07h
1575 ≤ FSW < 1625 kHz	1600	0B20h
1625 ≤ FSW < 1675 kHz	1650	0B39h
1675 ≤ FSW < 1725 kHz	1700	0B52h
1725 ≤ FSW < 1775 kHz	1750	0B6Bh
1775 ≤ FSW < 1850 kHz	1800	0B84h
1850 ≤ FSW < 1950 kHz	1900	0BB6h
1950 ≤ FSW ≤ 2000 kHz	2000	0BE8h
Greater than 2000 kHz	Invalid/Unsupported	Invalid/Unsupported

Attempts to write (33h) FREQUENCY_SWITCH to any value outside those specified as valid, will be considered invalid/unsupported data and cause TPS536xx to respond by flagging the appropriate status bits, and notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

1.2.32 (34h) POWER_MODE

CMD Address	34h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
Paged:	Yes
Phased:	No
NVM Back-up:	No
Updates:	On-the-fly

The POWER_MODE command changes the operating power state of the TPS536xx.

(34h) POWER_MODE Register Map

7	6	5	4	3	2	1	0
R	R	R	R	R	RW	RW	RW
0	0	0	0	0	PWR MODE		

LEGEND: R/W = Read/Write; R = Read only

Table 1-35. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:3	Reserved	R	0	Reserved.
2:0	PWR MODE	RW	See below	000b:Maximum Efficiency (enable phase shedding and allow DCM for all phases) 011b: Maximum Power (disable phase shedding and all phases run in FCCM mode) 100b: Manufacturer Defined. Enable Phase shedding and allow DCM for only the 1 phase operation, otherwise CCM. Others: Invalid/unsupported.

At power-up, (34h) POWER_MODE is initialized to either 00h or 03h based on the DPS EN bit in USER_DATA_07 (PHASE_SHED_CONFIG), regardless of the AUTO_DCM selections in MFR_SPECIFIC_ED (MISC_OPTIONS) .

1.2.33 (35h) VIN_ON

CMD Address	35h
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	SLINEAR11
Paged:	No
Phased:	No
NVM Back-up:	EEPROM
Updates:	On-the-fly

VIN_ON command sets the value of the input voltage, in Volts, at which level the unit starts power conversion.

(35h) VIN_ON Register Map

15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
VON EXP					VON MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VON MAN							

LEGEND: R/W = Read/Write; R = Read only

Table 1-36. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:11	VON EXP	RW	11110b	Linear format two's complement exponent, -2.
10:0	VON MAN	RW	NVM	Linear format two's complement mantissa. Refer to the text below for more information.

Attempts to write (35h) VIN_ON to any value outside those specified as valid, are considered invalid/unsupported data and cause TPS536xx to respond by flagging the appropriate status bits, and notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

Command Resolution and NVM Store/Restore Behavior

The (35h) VIN_ON command is implemented using the TPS536xx internal telemetry system. As a result, the value of this command may be programmed with very high resolution using the linear format. However, the TPS536xx provides only limited NVM-backed options for this command. Following a power-cycle or NVM Store/Restore operation, the value is restored to one of the values in the table below, according to the value present during the last NVM store operation. Refer to the table below. During operation, updates to this command with higher resolution than the options in the NVM supported table, are supported, and accepted as long as they fall between the minimum and maximum supported values given.

Table 1-37. NVM-supported Values

VIN_ON (decoded) during last NVM Store	Reset Value (decoded) Turn-on Voltage (V)	Nominal SLINEAR11 (hex)
Less than 4.25 V	Invalid/unsupported	Invalid/unsupported
4.25 ≤ VON < 4.375 V	4.25	F011h
4.375 ≤ VON < 4.625 V	4.5	F012h
4.625 ≤ VON < 4.875 V	4.75	F013h
4.875 ≤ VON < 5.125 V	5	F014h
5.125 ≤ VON < 5.375 V	5.25	F015h
5.375 ≤ VON < 5.625 V	5.5	F016h

Table 1-37. NVM-supported Values (continued)

VIN_ON (decoded) during last NVM Store	Reset Value (decoded) Turn-on Voltage (V)	Nominal SLINEAR11 (hex)
5.625 ≤ VON < 5.875 V	5.75	F017h
5.875 ≤ VON < 6.125 V	6	F018h
6.125 ≤ VON < 6.375 V	6.25	F019h
6.375 ≤ VON < 6.625 V	6.5	F01Ah
6.625 ≤ VON < 6.875 V	6.75	F01Bh
6.875 ≤ VON < 7.125 V	7	F01Ch
7.125 ≤ VON < 7.375 V	7.25	F01Dh
7.375 ≤ VON < 7.625 V	7.5	F01Eh
7.625 ≤ VON < 7.875 V	7.75	F01Fh
7.875 ≤ VON < 8.125 V	8	F020h
8.125 ≤ VON < 8.375 V	8.25	F021h
8.375 ≤ VON < 8.625 V	8.5	F022h
8.625 ≤ VON < 8.875 V	8.75	F023h
8.875 ≤ VON < 9.125 V	9	F024h
9.125 ≤ VON < 9.375 V	9.25	F025h
9.375 ≤ VON < 9.625 V	9.5	F026h
9.625 ≤ VON < 9.875 V	9.75	F027h
9.875 ≤ VON < 10.125 V	10	F028h
10.125 ≤ VON < 10.375 V	10.25	F029h
10.375 ≤ VON < 10.625 V	10.5	F02Ah
10.625 ≤ VON < 10.875 V	10.75	F02Bh
10.875 ≤ VON < 11.125 V	11	F02Ch
11.125 ≤ VON < 11.375 V	11.25	F02Dh
11.375 ≤ VON ≤ 11.5 V	11.5	F02Eh
greater than 11.5 V	Invalid/unsupported	Invalid/unsupported

1.2.34 (36h) VIN_OFF

CMD Address	36h
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	SLINEAR11
Paged:	No
Phased:	No
NVM Back-up:	EEPROM
Updates:	On-the-fly

Note

VIN_OFF is a shadow command for VIN_UV_FAULT_LIMIT. Updates to VIN_UV_FAULT_LIMIT update VIN_OFF. Updates to VIN_OFF update VIN_UV_FAULT_LIMIT.

VIN_OFF command sets the value of the input voltage, in Volts, at which level the unit stops power conversion. Updates to VIN_OFF also update VIN_UV_FAULT_LIMIT . Likewise, updates to VIN_UV_FAULT_LIMIT also update VIN_OFF . VIN_OFF and VIN_UV_FAULT_LIMIT are forced to have the same value at all times. This procedure allows the TPS536xx to support the latch-off response to low input voltage faults, while avoiding corner cases loosely defined by the PMBus specification.

(36h) VIN_OFF Register Map

15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
VOFF EXP					VOFF MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VOFF MAN							

LEGEND: R/W = Read/Write; R = Read only

Table 1-38. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:11	VOFF EXP	RW	11110b	Linear format two's complement exponent.
10:0	VOFF MAN	RW	NVM	Linear format two's complement mantissa. Refer to the text below.

Attempts to write (36h) VIN_OFF to any value outside those specified as valid, will be considered invalid/ unsupported data and cause TPS536xx to respond by flagging the appropriate status bits, and notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

Command Resolution and NVM Store/Restore Behavior

The (36h) VIN_OFF command is implemented using the TPS536xx internal telemetry system. As a result the value of this command may be programmed with very high resolution using the linear format. However, the TPS536xx provides only limited NVM-backed options for this command. Following a power-cycle or NVM Store/ Restore operation, the value will be restored to one of the values in the table below, according to the value present during the last NVM store operation. Refer to the table below. During operation, updates to this command with higher resolution than the options in the NVM supported table, will be supported, and accepted as long as they fall between the minimum and maximum supported values given.

Table 1-39. NVM-Supported Values

VIN_OFF (decoded) during last NVM Store	VIN_OFF Reset value (decoded) following Reset/Restore (V)	Nominal SLINEAR11 (hex)
Less than 4 V	Invalid/Unsupported	Invalid/Unsupported
4 ≤ VOFF < 4.125 V	4.00	F010h
4.125 ≤ VOFF < 4.375 V	4.25	F011h
4.375 ≤ VOFF < 4.625 V	4.50	F012h
4.625 ≤ VOFF < 4.875 V	4.75	F013h
4.875 ≤ VOFF < 5.125 V	5.00	F014h
5.125 ≤ VOFF < 5.375 V	5.25	F015h
5.375 ≤ VOFF < 5.625 V	5.50	F016h
5.625 ≤ VOFF < 5.875 V	5.75	F017h
5.875 ≤ VOFF < 6.125 V	6.00	F018h
6.125 ≤ VOFF < 6.375 V	6.25	F019h
6.375 ≤ VOFF < 6.625 V	6.50	F01Ah
6.625 ≤ VOFF < 6.875 V	6.75	F01Bh
6.875 ≤ VOFF < 7.125 V	7.00	F01Ch
7.125 ≤ VOFF < 7.375 V	7.25	F01Dh
7.375 ≤ VOFF < 7.625 V	7.50	F01Eh
7.625 ≤ VOFF < 7.875 V	7.75	F01Fh
7.875 ≤ VOFF < 8.125 V	8.00	F020h
8.125 ≤ VOFF < 8.375 V	8.25	F021h
8.375 ≤ VOFF < 8.625 V	8.50	F022h
8.625 ≤ VOFF < 8.875 V	8.75	F023h
8.875 ≤ VOFF < 9.125 V	9.00	F024h
9.125 ≤ VOFF < 9.375 V	9.25	F025h
9.375 ≤ VOFF < 9.625 V	9.50	F026h
9.625 ≤ VOFF < 9.875 V	9.75	F027h
9.875 ≤ VOFF < 10.125 V	10.00	F028h
10.125 ≤ VOFF < 10.375 V	10.25	F029h
10.375 ≤ VOFF < 10.625 V	10.50	F02Ah
10.625 ≤ VOFF < 10.875 V	10.75	F02Bh
10.875 ≤ VOFF < 11.125 V	11.00	F02Ch
11.125 ≤ VOFF ≤ 11.25 V	11.25	F02Dh
Greater than 11.25 V	Invalid/unsupported	Invalid/Unsupported

Because VIN_OFF and VIN_UV_FAULT_LIMIT are forced to the same threshold, if during power conversion, if the sensed power stage input voltage (VIN_CSNIN pins) falls below the VIN_OFF threshold, the LOW_VIN/ VIN_UV_FAULT conditions are triggered. Note this fault condition is masked until the sensed input voltage exceeds VIN_ON for the first time.

This results cause TPS536xx to :

- Respond per the settings in VIN_UV_FAULT_RESPONSE
- Set the OFF and VIN_UV bits in the STATUS_BYTE
- Set the INPUT bit in the STATUS_WORD
- Set the VIN_UVF bit in STATUS_INPUT
- Notify the host per PMBus 1.3.1 Part II specification, section 10.2.

1.2.35 (38h) IOUT_CAL_GAIN

CMD Address	38h
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	SLINEAR11
Paged:	Yes
Phased:	No
NVM Back-up:	EEPROM
Updates:	On-the-fly

IOUT_CAL_GAIN is used to compensate for set the ratio of the voltage at the current sense pins to the sensed current for the READ_IOUT command. Each PAGE has an IOUT_CAL_GAIN value. One gain setting applies to all phases in the channel. The units are mΩ.

(38h) IOUT_CAL_GAIN Register Map

15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
IOCG EXP					IOCG MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
IOCG MAN							

LEGEND: R/W = Read/Write; R = Read only

Table 1-40. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:11	IOCG EXP	RW	11001b	Linear format, two's complement exponent.
10:0	IOCG MAN	RW	NVM	Linear format, two's complement mantissa.

Attempts to write (38h) IOUT_CAL_GAIN to any value outside those specified as valid, will be considered invalid/unsupported data and cause TPS536xx to respond by flagging the appropriate status bits, and notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

Command Resolution and NVM Store/Restore Behavior

The (38h) IOUT_CAL_GAIN command is implemented using the TPS536xx internal telemetry system. As a result the value of this command may be programmed with very high resolution using the linear format. However, the TPS536xx provides only limited NVM-backed options for this command. Following a power-cycle or NVM Store/Restore operation, the value will be restored to one of the values in the table below, according to the value present during the last NVM store operation. Refer to the table below. During operation, updates to this command with higher resolution than the options in the NVM supported table, will be supported, and accepted as long as they fall between the minimum and maximum supported values given.

Table 1-41. Hardware Supported Values

IOUT_CAL_GAIN (decoded) during last NVM Store	Reset Value (decoded) IMON Calibration Gain (mΩ)	Nominal SLINEAR11 (hex)
Less than 4.5 mΩ	Invalid/unsupported	Invalid/unsupported
4.5 ≤ IOCG < 4.50390625 mΩ	4.5000000	CA40h
4.50390625 ≤ IOCG < 4.51171875 mΩ	4.5078125	CA41h
4.51171875 ≤ IOCG < 4.51953125 mΩ	4.5156250	CA42h
4.51953125 ≤ IOCG < 4.52734375 mΩ	4.5234375	CA43h
4.52734375 ≤ IOCG < 4.53515625 mΩ	4.5312500	CA44h

Table 1-41. Hardware Supported Values (continued)

IOUT_CAL_GAIN (decoded) during last NVM Store	Reset Value (decoded) IMON Calibration Gain (mΩ)	Nominal SLINEAR11 (hex)
4.53515625 ≤ IOCG < 4.54296875 mΩ	4.5390625	CA45h
4.54296875 ≤ IOCG < 4.55078125 mΩ	4.5468750	CA46h
4.55078125 ≤ IOCG < 4.55859375 mΩ	4.5546875	CA47h
4.55859375 ≤ IOCG < 4.56640625 mΩ	4.5625000	CA48h
4.56640625 ≤ IOCG < 4.57421875 mΩ	4.5703125	CA49h
4.57421875 ≤ IOCG < 4.58203125 mΩ	4.5781250	CA4Ah
4.58203125 ≤ IOCG < 4.58984375 mΩ	4.5859375	CA4Bh
4.58984375 ≤ IOCG < 4.59765625 mΩ	4.5937500	CA4Ch
4.59765625 ≤ IOCG < 4.60546875 mΩ	4.6015625	CA4Dh
4.60546875 ≤ IOCG < 4.61328125 mΩ	4.6093750	CA4Eh
4.61328125 ≤ IOCG < 4.62109375 mΩ	4.6171875	CA4Fh
4.62109375 ≤ IOCG < 4.62890625 mΩ	4.6250000	CA50h
4.62890625 ≤ IOCG < 4.63671875 mΩ	4.6328125	CA51h
4.63671875 ≤ IOCG < 4.64453125 mΩ	4.6406250	CA52h
4.64453125 ≤ IOCG < 4.65234375 mΩ	4.6484375	CA53h
4.65234375 ≤ IOCG < 4.66015625 mΩ	4.6562500	CA54h
4.66015625 ≤ IOCG < 4.66796875 mΩ	4.6640625	CA55h
4.66796875 ≤ IOCG < 4.67578125 mΩ	4.6718750	CA56h
4.67578125 ≤ IOCG < 4.68359375 mΩ	4.6796875	CA57h
4.68359375 ≤ IOCG < 4.69140625 mΩ	4.6875000	CA58h
4.69140625 ≤ IOCG < 4.69921875 mΩ	4.6953125	CA59h
4.69921875 ≤ IOCG < 4.70703125 mΩ	4.7031250	CA5Ah
4.70703125 ≤ IOCG < 4.71484375 mΩ	4.7109375	CA5Bh
4.71484375 ≤ IOCG < 4.72265625 mΩ	4.7187500	CA5Ch
4.72265625 ≤ IOCG < 4.73046875 mΩ	4.7265625	CA5Dh
4.73046875 ≤ IOCG < 4.73828125 mΩ	4.7343750	CA5Eh
4.73828125 ≤ IOCG < 4.74609375 mΩ	4.7421875	CA5Fh
4.74609375 ≤ IOCG < 4.75390625 mΩ	4.7500000	CA60h
4.75390625 ≤ IOCG < 4.76171875 mΩ	4.7578125	CA61h
4.76171875 ≤ IOCG < 4.76953125 mΩ	4.7656250	CA62h
4.76953125 ≤ IOCG < 4.77734375 mΩ	4.7734375	CA63h
4.77734375 ≤ IOCG < 4.78515625 mΩ	4.7812500	CA64h
4.78515625 ≤ IOCG < 4.79296875 mΩ	4.7890625	CA65h
4.79296875 ≤ IOCG < 4.80078125 mΩ	4.7968750	CA66h
4.80078125 ≤ IOCG < 4.80859375 mΩ	4.8046875	CA67h
4.80859375 ≤ IOCG < 4.81640625 mΩ	4.8125000	CA68h
4.81640625 ≤ IOCG < 4.82421875 mΩ	4.8203125	CA69h
4.82421875 ≤ IOCG < 4.83203125 mΩ	4.8281250	CA6Ah
4.83203125 ≤ IOCG < 4.83984375 mΩ	4.8359375	CA6Bh
4.83984375 ≤ IOCG < 4.84765625 mΩ	4.8437500	CA6Ch
4.84765625 ≤ IOCG < 4.85546875 mΩ	4.8515625	CA6Dh
4.85546875 ≤ IOCG < 4.86328125 mΩ	4.8593750	CA6Eh
4.86328125 ≤ IOCG < 4.87109375 mΩ	4.8671875	CA6Fh
4.87109375 ≤ IOCG < 4.87890625 mΩ	4.8750000	CA70h

Table 1-41. Hardware Supported Values (continued)

IOUT_CAL_GAIN (decoded) during last NVM Store	Reset Value (decoded) IMON Calibration Gain (mΩ)	Nominal SLINEAR11 (hex)
4.87890625 ≤ IOCG < 4.88671875 mΩ	4.8828125	CA71h
4.88671875 ≤ IOCG < 4.89453125 mΩ	4.8906250	CA72h
4.89453125 ≤ IOCG < 4.90234375 mΩ	4.8984375	CA73h
4.90234375 ≤ IOCG < 4.91015625 mΩ	4.9062500	CA74h
4.91015625 ≤ IOCG < 4.91796875 mΩ	4.9140625	CA75h
4.91796875 ≤ IOCG < 4.92578125 mΩ	4.9218750	CA76h
4.92578125 ≤ IOCG < 4.93359375 mΩ	4.9296875	CA77h
4.93359375 ≤ IOCG < 4.94140625 mΩ	4.9375000	CA78h
4.94140625 ≤ IOCG < 4.94921875 mΩ	4.9453125	CA79h
4.94921875 ≤ IOCG < 4.95703125 mΩ	4.9531250	CA7Ah
4.95703125 ≤ IOCG < 4.96484375 mΩ	4.9609375	CA7Bh
4.96484375 ≤ IOCG < 4.97265625 mΩ	4.9687500	CA7Ch
4.97265625 ≤ IOCG < 4.98046875 mΩ	4.9765625	CA7Dh
4.98046875 ≤ IOCG < 4.98828125 mΩ	4.9843750	CA7Eh
4.98828125 ≤ IOCG < 4.99609375 mΩ	4.9921875	CA7Fh
4.99609375 ≤ IOCG < 5.00390625 mΩ	5.0000000	CA80h
5.00390625 ≤ IOCG < 5.01171875 mΩ	5.0078125	CA81h
5.01171875 ≤ IOCG < 5.01953125 mΩ	5.0156250	CA82h
5.01953125 ≤ IOCG < 5.02734375 mΩ	5.0234375	CA83h
5.02734375 ≤ IOCG < 5.03515625 mΩ	5.0312500	CA84h
5.03515625 ≤ IOCG < 5.04296875 mΩ	5.0390625	CA85h
5.04296875 ≤ IOCG < 5.05078125 mΩ	5.0468750	CA86h
5.05078125 ≤ IOCG < 5.05859375 mΩ	5.0546875	CA87h
5.05859375 ≤ IOCG < 5.06640625 mΩ	5.0625000	CA88h
5.06640625 ≤ IOCG < 5.07421875 mΩ	5.0703125	CA89h
5.07421875 ≤ IOCG < 5.08203125 mΩ	5.0781250	CA8Ah
5.08203125 ≤ IOCG < 5.08984375 mΩ	5.0859375	CA8Bh
5.08984375 ≤ IOCG < 5.09765625 mΩ	5.0937500	CA8Ch
5.09765625 ≤ IOCG < 5.10546875 mΩ	5.1015625	CA8Dh
5.10546875 ≤ IOCG < 5.11328125 mΩ	5.1093750	CA8Eh
5.11328125 ≤ IOCG < 5.12109375 mΩ	5.1171875	CA8Fh
5.12109375 ≤ IOCG < 5.12890625 mΩ	5.1250000	CA90h
5.12890625 ≤ IOCG < 5.13671875 mΩ	5.1328125	CA91h
5.13671875 ≤ IOCG < 5.14453125 mΩ	5.1406250	CA92h
5.14453125 ≤ IOCG < 5.15234375 mΩ	5.1484375	CA93h
5.15234375 ≤ IOCG < 5.16015625 mΩ	5.1562500	CA94h
5.16015625 ≤ IOCG < 5.16796875 mΩ	5.1640625	CA95h
5.16796875 ≤ IOCG < 5.17578125 mΩ	5.1718750	CA96h
5.17578125 ≤ IOCG < 5.18359375 mΩ	5.1796875	CA97h
5.18359375 ≤ IOCG < 5.19140625 mΩ	5.1875000	CA98h
5.19140625 ≤ IOCG < 5.19921875 mΩ	5.1953125	CA99h
5.19921875 ≤ IOCG < 5.20703125 mΩ	5.2031250	CA9Ah
5.20703125 ≤ IOCG < 5.21484375 mΩ	5.2109375	CA9Bh
5.21484375 ≤ IOCG < 5.22265625 mΩ	5.2187500	CA9Ch

Table 1-41. Hardware Supported Values (continued)

IOUT_CAL_GAIN (decoded) during last NVM Store	Reset Value (decoded) IMON Calibration Gain (mΩ)	Nominal SLINEAR11 (hex)
5.22265625 ≤ IOCG < 5.23046875 mΩ	5.2265625	CA9Dh
5.23046875 ≤ IOCG < 5.23828125 mΩ	5.2343750	CA9Eh
5.23828125 ≤ IOCG < 5.24609375 mΩ	5.2421875	CA9Fh
5.24609375 ≤ IOCG < 5.25390625 mΩ	5.2500000	CAA0h
5.25390625 ≤ IOCG < 5.26171875 mΩ	5.2578125	CAA1h
5.26171875 ≤ IOCG < 5.26953125 mΩ	5.2656250	CAA2h
5.26953125 ≤ IOCG < 5.27734375 mΩ	5.2734375	CAA3h
5.27734375 ≤ IOCG < 5.28515625 mΩ	5.2812500	CAA4h
5.28515625 ≤ IOCG < 5.29296875 mΩ	5.2890625	CAA5h
5.29296875 ≤ IOCG < 5.30078125 mΩ	5.2968750	CAA6h
5.30078125 ≤ IOCG < 5.30859375 mΩ	5.3046875	CAA7h
5.30859375 ≤ IOCG < 5.31640625 mΩ	5.3125000	CAA8h
5.31640625 ≤ IOCG < 5.32421875 mΩ	5.3203125	CAA9h
5.32421875 ≤ IOCG < 5.33203125 mΩ	5.3281250	CAAAh
5.33203125 ≤ IOCG < 5.33984375 mΩ	5.3359375	CAABh
5.33984375 ≤ IOCG < 5.34765625 mΩ	5.3437500	CAACh
5.34765625 ≤ IOCG < 5.35546875 mΩ	5.3515625	CAADh
5.35546875 ≤ IOCG < 5.36328125 mΩ	5.3593750	CAAEh
5.36328125 ≤ IOCG < 5.37109375 mΩ	5.3671875	CAAFh
5.37109375 ≤ IOCG < 5.37890625 mΩ	5.3750000	CAB0h
5.37890625 ≤ IOCG < 5.38671875 mΩ	5.3828125	CAB1h
5.38671875 ≤ IOCG < 5.39453125 mΩ	5.3906250	CAB2h
5.39453125 ≤ IOCG < 5.40234375 mΩ	5.3984375	CAB3h
5.40234375 ≤ IOCG < 5.41015625 mΩ	5.4062500	CAB4h
5.41015625 ≤ IOCG < 5.41796875 mΩ	5.4140625	CAB5h
5.41796875 ≤ IOCG < 5.42578125 mΩ	5.4218750	CAB6h
5.42578125 ≤ IOCG < 5.43359375 mΩ	5.4296875	CAB7h
5.43359375 ≤ IOCG < 5.44140625 mΩ	5.4375000	CAB8h
5.44140625 ≤ IOCG < 5.44921875 mΩ	5.4453125	CAB9h
5.44921875 ≤ IOCG < 5.45703125 mΩ	5.4531250	CABAh
5.45703125 ≤ IOCG < 5.46484375 mΩ	5.4609375	CABBh
5.46484375 ≤ IOCG < 5.47265625 mΩ	5.4687500	CABCh
5.47265625 ≤ IOCG < 5.48046875 mΩ	5.4765625	CABDh
5.48046875 ≤ IOCG < 5.48828125 mΩ	5.4843750	CABEh
5.48828125 ≤ IOCG < 5.4921875 mΩ	5.4921875	CABFh
Greater than 5.4921875 mΩ	Invalid/unsupported	Invalid/unsupported

1.2.36 (39h) IOUT_CAL_OFFSET

CMD Address	39h
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	SLINEAR11
Paged:	Yes
Phased:	Yes
NVM Back-up:	EEPROM
Updates:	On-the-fly

IOUT_CAL_OFFSET is used to compensate for offset errors in the READ_IOUT command. Each PHASE in the controller has an IOUT_CAL_OFFSET value. The units are amperes.

The effective offset for the per-PAGE current reading is equal to the sum of the active phases in that channel. For example, if 2 phases are active, the effective offset for the total current reading is equal to the sum of the offsets applied to those two phases.

(39h) IOUT_CAL_OFFSET Register Map

15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
IOCOS EXP					IOCOS MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
IOCOS MAN							

LEGEND: R/W = Read/Write; R = Read only

Table 1-42. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:11	IOCOS EXP	RW	11101b	Linear format, two's complement exponent.
10:0	IOCOS MAN	RW	NVM	Linear format, two's complement mantissa.

Attempts to write (39h) IOUT_CAL_OFFSET to any value outside those specified as valid, will be considered invalid/unsupported data and cause TPS536xx to respond by flagging the appropriate status bits, and notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

Command resolution and NVM store/restore behavior

The (39h) IOUT_CAL_OFFSET command is implemented using the TPS536xx internal telemetry system. As a result the value of this command may be programmed with very high resolution using the linear format. However, the TPS536xx provides only limited NVM-backed options for this command. Following a power-cycle or NVM Store/Restore operation, the value will be restored to one of the values in the table below, according to the value present during the last NVM store operation. Refer to the table below. During operation, updates to this command with higher resolution than the options in the NVM supported table, will be supported, and accepted as long as they fall between the minimum and maximum supported values given.

Table 1-43. NVM Supported Values

IOUT_CAL_OFFSET (decoded) during last NVM Store	Reset Value (decoded) IMON Calibration Offset (A)	Nominal SLINEAR11 (hex)
Less than -4 A	Invalid/unsupported	Invalid/unsupported
-4 ≤ IOCOS < -3.9375 A	-4.000	EFE0h
-3.9375 ≤ IOCOS < -3.8125 A	-3.875	EFE1h

Table 1-43. NVM Supported Values (continued)

IOUT_CAL_OFFSET (decoded) during last NVM Store	Reset Value (decoded) IMON Calibration Offset (A)	Nominal SLINEAR11 (hex)
-3.8125 ≤ IOCOS < -3.6875 A	-3.750	EFE2h
-3.6875 ≤ IOCOS < -3.5625 A	-3.625	EFE3h
-3.5625 ≤ IOCOS < -3.4375 A	-3.500	EFE4h
-3.4375 ≤ IOCOS < -3.3125 A	-3.375	EFE5h
-3.3125 ≤ IOCOS < -3.1875 A	-3.250	EFE6h
-3.1875 ≤ IOCOS < -3.0625 A	-3.125	EFE7h
-3.0625 ≤ IOCOS < -2.9375 A	-3.000	EFE8h
-2.9375 ≤ IOCOS < -2.8125 A	-2.875	EFE9h
-2.8125 ≤ IOCOS < -2.6875 A	-2.750	EFEAh
-2.6875 ≤ IOCOS < -2.5625 A	-2.625	EFEBh
-2.5625 ≤ IOCOS < -2.4375 A	-2.500	EFECh
-2.4375 ≤ IOCOS < -2.3125 A	-2.375	EFEDh
-2.3125 ≤ IOCOS < -2.1875 A	-2.250	EFEEh
-2.1875 ≤ IOCOS < -2.0625 A	-2.125	EFEFh
-2.0625 ≤ IOCOS < -1.9375 A	-2.000	EFF0h
-1.9375 ≤ IOCOS < -1.8125 A	-1.875	EFF1h
-1.8125 ≤ IOCOS < -1.6875 A	-1.750	EFF2h
-1.6875 ≤ IOCOS < -1.5625 A	-1.625	EFF3h
-1.5625 ≤ IOCOS < -1.4375 A	-1.500	EFF4h
-1.4375 ≤ IOCOS < -1.3125 A	-1.375	EFF5h
-1.3125 ≤ IOCOS < -1.1875 A	-1.250	EFF6h
-1.1875 ≤ IOCOS < -1.0625 A	-1.125	EFF7h
-1.0625 ≤ IOCOS < -0.9375 A	-1.000	EFF8h
-0.9375 ≤ IOCOS < -0.8125 A	-0.875	EFF9h
-0.8125 ≤ IOCOS < -0.6875 A	-0.750	EFFAh
-0.6875 ≤ IOCOS < -0.5625 A	-0.625	EFFBh
-0.5625 ≤ IOCOS < -0.4375 A	-0.500	EFFCh
-0.4375 ≤ IOCOS < -0.3125 A	-0.375	EFFDh
-0.3125 ≤ IOCOS < -0.1875 A	-0.250	EFFEh
-0.1875 ≤ IOCOS < -0.0625 A	-0.125	EFFFh
-0.0625 ≤ IOCOS < 0.0625 A	0.000	B800h
0.0625 ≤ IOCOS < 0.1875 A	0.125	E801h
0.1875 ≤ IOCOS < 0.3125 A	0.250	E802h
0.3125 ≤ IOCOS < 0.4375 A	0.375	E803h
0.4375 ≤ IOCOS < 0.5625 A	0.500	E804h
0.5625 ≤ IOCOS < 0.6875 A	0.625	E805h
0.6875 ≤ IOCOS < 0.8125 A	0.750	E806h
0.8125 ≤ IOCOS < 0.9375 A	0.875	E807h
0.9375 ≤ IOCOS < 1.0625 A	1.000	E808h
1.0625 ≤ IOCOS < 1.1875 A	1.125	E809h
1.1875 ≤ IOCOS < 1.3125 A	1.250	E80Ah
1.3125 ≤ IOCOS < 1.4375 A	1.375	E80Bh
1.4375 ≤ IOCOS < 1.5625 A	1.500	E80Ch
1.5625 ≤ IOCOS < 1.6875 A	1.625	E80Dh

Table 1-43. NVM Supported Values (continued)

IOUT_CAL_OFFSET (decoded) during last NVM Store	Reset Value (decoded) IMON Calibration Offset (A)	Nominal SLINEAR11 (hex)
1.6875 ≤ IOCOS < 1.8125 A	1.750	E80Eh
1.8125 ≤ IOCOS < 1.9375 A	1.875	E80Fh
1.9375 ≤ IOCOS < 2.0625 A	2.000	E810h
2.0625 ≤ IOCOS < 2.1875 A	2.125	E811h
2.1875 ≤ IOCOS < 2.3125 A	2.250	E812h
2.3125 ≤ IOCOS < 2.4375 A	2.375	E813h
2.4375 ≤ IOCOS < 2.5625 A	2.500	E814h
2.5625 ≤ IOCOS < 2.6875 A	2.625	E815h
2.6875 ≤ IOCOS < 2.8125 A	2.750	E816h
2.8125 ≤ IOCOS < 2.9375 A	2.875	E817h
2.9375 ≤ IOCOS < 3.0625 A	3.000	E818h
3.0625 ≤ IOCOS < 3.1875 A	3.125	E819h
3.1875 ≤ IOCOS < 3.3125 A	3.250	E81Ah
3.3125 ≤ IOCOS < 3.4375 A	3.375	E81Bh
3.4375 ≤ IOCOS < 3.5625 A	3.500	E81Ch
3.5625 ≤ IOCOS < 3.6875 A	3.625	E81Dh
3.6875 ≤ IOCOS < 3.75 A	3.750	E81Eh
Greater than 3.75 A	Invalid/Unsupported	Invalid/unsupported

Phased command behavior:

PHASE = 00h to (highest order phase assigned to the current page): Writes to (39h) IOUT_CAL_OFFSET modify the current sense offset for individual phases. Reads to (39h) IOUT_CAL_OFFSET return the configured current sense offset for individual phases.

PHASE = 80h or FFh: Writes to (39h) IOUT_CAL_OFFSET modify the current sense offset for all individual phases. Reads to (39h) IOUT_CAL_OFFSET return the configured current sense offset for PHASE =0.

1.2.37 (40h) VOUT_OV_FAULT_LIMIT

CMD Address	40h
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	ULINEAR16 Absolute
Paged:	Yes
Phased:	No
NVM Back-up:	EEPROM
Updates:	On-the-fly. Command may be NACK but still updated on the valid channel, if PAGE = FFh and data received is valid for only one channel.

The VOUT_OV_FAULT_LIMIT command sets the value of the output voltage measured at the sense or output pins that causes an output overvoltage fault. TPS536xx supports a two-stage overvoltage protection. The VOUT_OV_FAULT_LIMIT sets an over-voltage threshold relative to the current VOUT_COMMAND . Updates to VOUT_COMMAND cause the hex value of VOUT_OV_FAULT_LIMIT to be re-calculated, but do not change the actual offset threshold selected.

For example, if VOUT_COMMAND = 1.0 V, write VOUT_OV_FAULT_LIMIT = 1.128 V to select the +128 mV tracking over-voltage fault threshold. If the VOUT_COMMAND is changed to 1.1 V, the +128 mV threshold selection is not changed, but TPS536xx reports the VOUT_OV_FAULT_LIMIT as 1.1+128mV = 1.228 V.

Note: All calculations assume Zero Load-Line and zero VOUT_TRIM . Updates to VOUT_DROOP or READ_IOUT or VOUT_TRIM do not affect this command. However, this fault detection occurs in the analog domain, and does in fact include all offsets and droop compensation. All calculations assume VOUT_SCALE_LOOP = 1.0. For example, selecting the +128 mV threshold, with VOUT_SCALE_LOOP = 0.5 results in an actual threshold of +256 mV (+128 mV as measured at the TPS536xx VSP pins).

Following an overvoltage fault condition, the TPS536xx responds according to VOUT_OV_FAULT_RESPONSE.

(40h) VOUT_OV_FAULT_LIMIT Register Map

15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
VOUT OVF (High Byte)							
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VOUT OVF (Low Byte)							

LEGEND: R/W = Read/Write; R = Read only

Table 1-44. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:0	VOUT OVF	RW	See Below.	Sets the overvoltage fault limit. ULINEAR16 format. When VBOOT = 0V, the device automatically selects the widest threshold (+448 mV) regardless if the value stored in NVM.

Hardware Support and Value Mapping

The hardware for VOUT_OV_FAULT_LIMIT is implemented as a fixed offset relative to the current output voltage target. This includes droop and any offsets applied. TPS536xx calculates the threshold to select based on the VOUT_OV_FAULT_LIMIT value it receives, when this command is updated.

Table 1-45. Supported Value Mapping (Absolute Format)

VOUT_OV_FAULT_LIMIT value programmed (decoded)	Selected Tracking OV threshold (mV)
VOUT_COMMAND + (less than 32 mV)	Invalid/Unsupported

Table 1-45. Supported Value Mapping (Absolute Format) (continued)

VOUT_OV_FAULT_LIMIT value programmed (decoded)	Selected Tracking OV threshold (mV)
VOUT_COMMAND + 32 mV	32
VOUT_COMMAND + 64 mV	64
VOUT_COMMAND + 96 mV	96
VOUT_COMMAND + 128 mV	128
VOUT_COMMAND + 160 mV	160
VOUT_COMMAND + 192 mV	192
VOUT_COMMAND + 224 mV	224
VOUT_COMMAND + 256 mV	256
VOUT_COMMAND + 288 mV	288
VOUT_COMMAND + 320 mV	320
VOUT_COMMAND + 352 mV	352
VOUT_COMMAND + 384 mV	384
VOUT_COMMAND + 416 mV	416
VOUT_COMMAND + 448 mV	448
VOUT_COMMAND + (greater than 448 mV)	Invalid/Unsupported

Attempts to write (40h) VOUT_OV_FAULT_LIMIT to any value outside those specified as valid, will be considered invalid/unsupported data and cause TPS536xx to respond by flagging the appropriate status bits, and notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

1.2.38 (41h) VOUT_OV_FAULT_RESPONSE

CMD Address	41h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
Paged:	Yes
Phased:	No
NVM Back-up:	EEPROM
Updates:	On-the-fly. Do not change during a fault shutdown event.

The VOUT_OV_FAULT_RESPONSE instructs the device on what action to take in response to an output overvoltage fault. Upon triggering the over-voltage fault, the controller TPS536xx responds according to the data byte below, and the following actions are taken:

- Set the VOUT_OV_FAULT bit in the STATUS_BYTE ,
- Set the VOUT bit in the STATUS_WORD ,
- Set the VOUT_OVF bit in the STATUS_VOUT register
- Notify the host per PMBus 1.3.1 Part II specification, section 10.2.

(41h) VOUT_OV_FAULT_RESPONSE Register Map

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	R	R	R
VO OV RESP		VO OV RETRY			0	0	0

LEGEND: R/W = Read/Write; R = Read only

Table 1-46. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:6	VO OV RESP	RW	NVM	Output over-voltage response. 00b: Ignore. Continue operating without interruption. 10b: Shutdown . Shutdown and retry according to VO OV RETRY Other: Invalid/Unsupported
5:3	VO OV RETRY	R	NVM	0d: Do not attempt to restart (latch off). 7d: After shutting down, wait 1 HICCUP period, and attempt to restart indefinitely, until commanded OFF, or a successful startup occurs.

Attempts to write (41h) VOUT_OV_FAULT_RESPONSE to any value outside those specified as valid, will be considered invalid/unsupported data and cause TPS536xx to respond by flagging the appropriate status bits, and notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

1.2.39 (42h) VOUT_OV_WARN_LIMIT

CMD Address	42h
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	ULINEAR16 Absolute
Paged:	Yes
Phased:	No
NVM Back-up:	EEPROM
Updates:	On-the-fly. Command may be NACK but still updated on the valid channel, if PAGE = FFh and data received is valid for only one channel.

The VOUT_OV_WARN_LIMIT command sets the value of the output voltage at the sense or output pins that causes an output voltage high warning. This value must be less than the output overvoltage threshold. The VOUT_OV_WARN_LIMIT sets an over-voltage threshold relative to the current VOUT_COMMAND. Updates to VOUT_COMMAND cause the hex value of VOUT_OV_WARN_LIMIT to be re-calculated, but do not change the actual offset threshold selected.

For example, if VOUT_COMMAND = 1.0 V, write VOUT_OV_WARN_LIMIT = 1.064 V to select the +64 mV tracking over-voltage warning threshold. If the VOUT_COMMAND is changed to 1.1 V, the +64 mV threshold selection is not changed, but TPS536xx reports the VOUT_OV_WARN_LIMIT as 1.1+64mV = 1.164 V.

Note: All calculations assume zero load-line and zero VOUT_TRIM . Updates to VOUT_DROOP or READ_IOUT or VOUT_TRIM do not affect this command. However, this fault detection occurs in the analog domain, and does in fact include all offsets and droop compensation. All calculations assume VOUT_SCALE_LOOP = 1.0. For example, selecting the +64 mV threshold with VOUT_SCALE_LOOP = 0.5 results in an actual threshold of +128 mV (+64 mV as measured at the TPS536xx VSP pins).

When the sensed output voltage exceeds the VOUT_OV_WARN_LIMIT threshold, the following actions are taken:

- Set the VOUT bit in the STATUS_WORD ,
- Set the VOUT_OVW bit in the STATUS_VOUT register
- Notify the host per PMBus 1.3.1 Part II specification, section 10.2.

(42h) VOUT_OV_WARN_LIMIT Register Map

15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
VOUT OVW (High Byte)							
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VOUT OVW (Low Byte)							

LEGEND: R/W = Read/Write; R = Read only

Table 1-47. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:0	VOUT OVW	RW	NVM	Sets the overvoltage warning limit. Format is ULINEAR16. When VBOOT = 0V, the device automatically selects the widest threshold (+448 mV) regardless if the value stored in NVM.

Hardware Support and Value Mapping

The Hardware for VOUT_OV_WARN_LIMIT is implemented as a fixed offset relative to the current output voltage target. TPS536xx calculates the threshold to select based on the VOUT_OV_WARN_LIMIT value it receives, when this command is updated.

Table 1-48. Supported Value Mapping (Absolute format)

VOUT_OV_WARN_LIMIT value programmed	Tracking OV warn threshold (mV)
VOUT_COMMAND + (less than 8 mV)	Invalid/Unsupported
VOUT_COMMAND + 8 mV	8
VOUT_COMMAND + 16 mV	16
VOUT_COMMAND + 24 mV	24
VOUT_COMMAND + 32 mV	32
VOUT_COMMAND + 40 mV	40
VOUT_COMMAND + 48 mV	48
VOUT_COMMAND + 56 mV	56
VOUT_COMMAND + 64 mV	64
VOUT_COMMAND + 72 mV	72
VOUT_COMMAND + 80 mV	80
VOUT_COMMAND + 88 mV	88
VOUT_COMMAND + 96 mV	96
VOUT_COMMAND + 104 mV	104
VOUT_COMMAND + 112 mV	112
VOUT_COMMAND + 120 mV	120
VOUT_COMMAND + 128 mV	128
VOUT_COMMAND + 136 mV	136
VOUT_COMMAND + 144 mV	144
VOUT_COMMAND + 152 mV	152
VOUT_COMMAND + 160 mV	160
VOUT_COMMAND + 168 mV	168
VOUT_COMMAND + 176 mV	176
VOUT_COMMAND + 184 mV	184
VOUT_COMMAND + 192 mV	192
VOUT_COMMAND + 200 mV	200
VOUT_COMMAND + 208 mV	208
VOUT_COMMAND + 216 mV	216
VOUT_COMMAND + 224 mV	224
VOUT_COMMAND + 232 mV	232
VOUT_COMMAND + 240 mV	240
VOUT_COMMAND + 248 mV	248
VOUT_COMMAND + 256 mV	256
VOUT_COMMAND + 264 mV	264
VOUT_COMMAND + 272 mV	272
VOUT_COMMAND + 280 mV	280
VOUT_COMMAND + 288 mV	288
VOUT_COMMAND + 296 mV	296
VOUT_COMMAND + 304 mV	304
VOUT_COMMAND + 312 mV	312
VOUT_COMMAND + 320 mV	320
VOUT_COMMAND + 328 mV	328

Table 1-48. Supported Value Mapping (Absolute format) (continued)

VOUT_OV_WARN_LIMIT value programmed	Tracking OV warn threshold (mV)
VOUT_COMMAND + 336 mV	336
VOUT_COMMAND + 344 mV	344
VOUT_COMMAND + 352 mV	352
VOUT_COMMAND + 360 mV	360
VOUT_COMMAND + 368 mV	368
VOUT_COMMAND + 376 mV	376
VOUT_COMMAND + 384 mV	384
VOUT_COMMAND + 392 mV	392
VOUT_COMMAND + 400 mV	400
VOUT_COMMAND + 408 mV	408
VOUT_COMMAND + 416 mV	416
VOUT_COMMAND + 424 mV	424
VOUT_COMMAND + 432 mV	432
VOUT_COMMAND + 440 mV	440
VOUT_COMMAND + 448 mV	448
VOUT_COMMAND + (greater than 448 mV)	Invalid/Unsupported

Attempts to write (42h) VOUT_OV_WARN_LIMIT to any value outside those specified as valid, will be considered invalid/unsupported data and cause TPS536xx to respond by flagging the appropriate status bits, and notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

1.2.40 (43h) VOUT_UV_WARN_LIMIT

CMD Address	43h
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	ULINEAR16 Absolute
Paged:	Yes
Phased:	No
NVM Back-up:	EEPROM
Updates:	On-the-fly. Command may be NACK but still updated on the valid channel, if PAGE = FFh and data received is valid for only one channel.

The VOUT_UV_WARN_LIMIT command sets the value of the output voltage at the sense or output pins that causes an output voltage low warning. The VOUT_UV_WARN_LIMIT sets an under-voltage threshold relative to the current VOUT_COMMAND. Updates to VOUT_COMMAND cause the hex value of VOUT_UV_WARN_LIMIT to be re-calculated, but do not change the actual offset threshold selected.

For example, if VOUT_COMMAND = 1.0 V, write VOUT_UV_WARN_LIMIT = 0.936 V to select the -64 mV tracking under-voltage warning threshold. If the VOUT_COMMAND is changed to 1.1 V, the -64 mV threshold selection is not changed, but TPS536xx reports the VOUT_UV_WARN_LIMIT as 1.1-64mV = 1.036 V.

Note: All calculations assume zero load-line and zero VOUT_TRIM. Updates to VOUT_DROOP or READ_IOUT or VOUT_TRIM do not affect this command. However, this fault detection occurs in the analog domain, and does in fact include all offsets and droop compensation. All calculations assume VOUT_SCALE_LOOP = 1.0. For example, selecting the -64 mV threshold with VOUT_SCALE_LOOP = 0.5 results in an actual threshold of -128 mV (-64 mV as measured at the TPS536xx VSP pin).

When the sensed output voltage exceeds the VOUT_UV_WARN_LIMIT threshold, the following actions are taken:

- Set the VOUT bit in the STATUS_WORD ,
- Set the VOUT_UVW bit in the STATUS_VOUT register
- Notify the host per PMBus 1.3.1 Part II specification, section 10.2.

(43h) VOUT_UV_WARN_LIMIT Register Map

15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
VOUT UVW (High Byte)							
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VOUT UVW (Low Byte)							

LEGEND: R/W = Read/Write; R = Read only

Table 1-49. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:0	VOUT UVW	RW	NVM	Sets the undervoltage warning limit. Format is ULINEAR16. When VBOOT = 0V, the device automatically selects the widest threshold (-448 mV) regardless of the value stored in NVM.

Hardware Mapping and Supported Values

The Hardware for VOUT_UV_WARN_LIMIT is implemented as a fixed offset relative to the current output voltage target. TPS536xx calculates the threshold to select based on the VOUT_OV_WARN_LIMIT value it receives, when this command is updated.

Table 1-50. Supported Value Mapping (Absolute format)

VOUT_UV_WARN_LIMIT value programmed	Tracking UV warn threshold (mV)
VOUT_COMMAND − (less than 8 mV)	Invalid/Unsupported
VOUT_COMMAND − 8 mV	8
VOUT_COMMAND − 16 mV	16
VOUT_COMMAND − 24 mV	24
VOUT_COMMAND − 32 mV	32
VOUT_COMMAND − 40 mV	40
VOUT_COMMAND − 48 mV	48
VOUT_COMMAND − 56 mV	56
VOUT_COMMAND − 64 mV	64
VOUT_COMMAND − 72 mV	72
VOUT_COMMAND − 80 mV	80
VOUT_COMMAND − 88 mV	88
VOUT_COMMAND − 96 mV	96
VOUT_COMMAND − 104 mV	104
VOUT_COMMAND − 112 mV	112
VOUT_COMMAND − 120 mV	120
VOUT_COMMAND − 128 mV	128
VOUT_COMMAND − 136 mV	136
VOUT_COMMAND − 144 mV	144
VOUT_COMMAND − 152 mV	152
VOUT_COMMAND − 160 mV	160
VOUT_COMMAND − 168 mV	168
VOUT_COMMAND − 176 mV	176
VOUT_COMMAND − 184 mV	184
VOUT_COMMAND − 192 mV	192
VOUT_COMMAND − 200 mV	200
VOUT_COMMAND − 208 mV	208
VOUT_COMMAND − 216 mV	216
VOUT_COMMAND − 224 mV	224
VOUT_COMMAND − 232 mV	232
VOUT_COMMAND − 240 mV	240
VOUT_COMMAND − 248 mV	248
VOUT_COMMAND − 256 mV	256
VOUT_COMMAND − 264 mV	264
VOUT_COMMAND − 272 mV	272
VOUT_COMMAND − 280 mV	280
VOUT_COMMAND − 288 mV	288
VOUT_COMMAND − 296 mV	296
VOUT_COMMAND − 304 mV	304
VOUT_COMMAND − 312 mV	312
VOUT_COMMAND − 320 mV	320
VOUT_COMMAND − 328 mV	328
VOUT_COMMAND − 336 mV	336
VOUT_COMMAND − 344 mV	344
VOUT_COMMAND − 352 mV	352

Table 1-50. Supported Value Mapping (Absolute format) (continued)

VOUT_UV_WARN_LIMIT value programmed	Tracking UV warn threshold (mV)
VOUT_COMMAND − 360 mV	360
VOUT_COMMAND − 368 mV	368
VOUT_COMMAND − 376 mV	376
VOUT_COMMAND − 384 mV	384
VOUT_COMMAND − 392 mV	392
VOUT_COMMAND − 400 mV	400
VOUT_COMMAND − 408 mV	408
VOUT_COMMAND − 416 mV	416
VOUT_COMMAND − 424 mV	424
VOUT_COMMAND − 432 mV	432
VOUT_COMMAND − 440 mV	440
VOUT_COMMAND − 448 mV	448
VOUT_COMMAND − (greater than 448 mV)	Invalid/Unsupported

Attempts to write (43h) VOUT_UV_WARN_LIMIT to any value outside those specified as valid, will be considered invalid/unsupported data and cause TPS536xx to respond by flagging the appropriate status bits, and notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

1.2.41 (44h) VOUT_UV_FAULT_LIMIT

CMD Address	44h
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	ULINEAR16 Absolute
Paged:	Yes
Phased:	No
NVM Back-up:	EEPROM
Updates:	On-the-fly. Command may be NACK but still updated on the valid channel, if PAGE = FFh and data received is valid for only one channel.

The VOUT_UV_FAULT_LIMIT command sets the value of the output voltage at the sense or output pins that causes an output voltage fault. The VOUT_UV_FAULT_LIMIT sets an under-voltage threshold relative to the current VOUT_COMMAND. Updates to VOUT_COMMAND cause the hex value of VOUT_UV_WARN_LIMIT to be re-calculated, but do not change the actual offset threshold selected.

For example, if VOUT_COMMAND = 1.0 V, write VOUT_UV_FAULT_LIMIT = 0.872 V to select the -128 mV tracking under-voltage warning threshold. If the VOUT_COMMAND is changed to 1.1 V, the -128 mV threshold selection is not changed, but TPS536xx reports the VOUT_UV_FAULT_LIMIT as 1.1-128mV = 0.972 V.

Note: All calculations assume zero load-line and zero VOUT_TRIM. Updates to VOUT_DROOP or READ_IOUT or VOUT_TRIM do not affect this command. However, this fault detection occurs in the analog domain, and does in fact include all offsets and droop compensation. All calculations assume VOUT_SCALE_LOOP = 1.0. For example, selecting the -128 mV threshold with VOUT_SCALE_LOOP = 0.5 results in an actual threshold of -256 mV (-128 mV as measured by the TPS536xx VSP pins).

When the undervoltage fault condition is triggered, the TPS536xx responds according to VOUT_UV_FAULT_RESPONSE .

(44h) VOUT_UV_FAULT_LIMIT Register Map

15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
VOUT UVF (High Byte)							
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VOUT UVF (Low Byte)							

LEGEND: R/W = Read/Write; R = Read only

Table 1-51. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:0	VOUT UVF	RW	NVM	Sets the undervoltage fault limit. Format is ULINEAR16. When VBOOT = 0V, the device automatically selects the widest threshold (-448 mV) regardless if the value stored in NVM.

Hardware Mapping and Supported Values

The Hardware for VOUT_UV_FAULT_LIMIT is implemented as a fixed offset relative to the current output voltage target. TPS536xx calculates the threshold to select based on the VOUT_OV_WARN_LIMIT value it receives, when this command is updated.

Table 1-52. Supported Value Mapping

VOUT_UV_FAULT_LIMIT value programmed	Tracking UV fault limit selected (mV)
VOUT_COMMAND − (less than 32 mV)	Invalid/Unsupported

Table 1-52. Supported Value Mapping (continued)

VOUT_UV_FAULT_LIMIT value programmed	Tracking UV fault limit selected (mV)
VOUT_COMMAND − 32 mV	32
VOUT_COMMAND − 64 mV	64
VOUT_COMMAND − 96 mV	96
VOUT_COMMAND − 128 mV	128
VOUT_COMMAND − 160 mV	160
VOUT_COMMAND − 192 mV	192
VOUT_COMMAND − 224 mV	224
VOUT_COMMAND − 256 mV	256
VOUT_COMMAND − 288 mV	288
VOUT_COMMAND − 320 mV	320
VOUT_COMMAND − 352 mV	352
VOUT_COMMAND − 384 mV	384
VOUT_COMMAND − 416 mV	416
VOUT_COMMAND − 448 mV	448
VOUT_COMMAND − (greater than 448 mV)	Invalid

Attempts to write (44h) VOUT_UV_FAULT_LIMIT to any value outside those specified as valid, will be considered invalid/unsupported data and cause TPS536xx to respond by flagging the appropriate status bits, and notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

1.2.42 (45h) VOUT_UV_FAULT_RESPONSE

CMD Address	45h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
Paged:	Yes
Phased:	No
NVM Back-up:	EEPROM
Updates:	On-the-fly. Do not change during a fault shutdown event.

The VOUT_UV_FAULT_RESPONSE instructs the device on what action to take in response to an output undervoltage fault. Upon triggering the over-voltage fault, the controller TPS536xx responds according to the data byte below, and the following actions are taken:

- Set the NONE OF THE ABOVE bit in the STATUS_BYTE ,
- Set the VOUT bit in the STATUS_WORD ,
- Set the VOUT UVF bit in the STATUS_VOUT register
- Notify the host per PMBus 1.3.1 Part II specification, section 10.2.

(45h) VOUT_UV_FAULT_RESPONSE Register Map

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VO UV RESP		VO UV HICCUP			VO UV DLY		

LEGEND: R/W = Read/Write; R = Read only

Table 1-53. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:6	VO UV RESP	RW	NVM	Output over-voltage response. 00b: Ignore. Continue operating without interruption. 01b: Shutdown after Delay. Continue 10b: Shutdown Immediately. Shutdown and do not restart. Restart/clearing behavior is specified in the PMBus Specification v1.3, part II, section 10.7. Other: Invalid/Unsupported
5:3	VO UV HICCUP	RW	NVM	000b: Latch-off. 111b: Hiccup, retry indefinitely. Others: invalid/unsupported
2:0	VO UV DELY	RW	NVM	UV delay time (for respond after delay). Delay will be ignored for when VO UV RESP bits instruct the device to shutdown immediately. 000b: 4 µs 001b: 8 µs 010b: 12 µs 011b: 16 µs Others: Invalid/unsupported

Attempts to write (45h) VOUT_UV_FAULT_RESPONSE to any value outside those specified as valid, will be considered invalid/unsupported data and cause TPS536xx to respond by flagging the appropriate status bits, and notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

1.2.43 (46h) IOUT_OC_FAULT_LIMIT

CMD Address	46h
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	SLINEAR11
Paged:	Yes
Phased:	Set PHASE = FFh to update **per-page OCP** Set PHASE = 00h to update **per-phase cycle-by-cycle OCL**
NVM Back-up:	EEPROM
Updates:	On-the-fly

The IOUT_OC_FAULT_LIMIT command sets the value of the output current that causes the over-current detector to indicate an over-current fault condition. Note that the per-phase current limit for individual phases is independent from the total overcurrent threshold for the PAGE . Set the per-phase overcurrent limit by writing to IOUT_OC_FAULT_LIMIT with the PHASE set to 00h. Any PHASE setting other than FFh is accepted to update the per-phase OCL limit, 00h is suggested in this document because it will be accepted regardless of the phase settings. Set the per-page overcurrent protection threshold by writing to IOUT_OC_FAULT_LIMIT with the PHASE set to FFh.

When the per-page overcurrent protection is triggered, the TPS536xx responds according to IOUT_OC_FAULT_RESPONSE. Per-phase current limit being triggered does not cause any interruption to power conversion, or set any status bits or alerts.

(46h) IOUT_OC_FAULT_LIMIT Register Map

15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
IOOCF EXP					IOOCF MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
IOOCF MAN							

LEGEND: R/W = Read/Write; R = Read only

Table 1-54. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:11	IOOCF EXP	RW	00000b	Linear format two's complement exponent.
10:0	IOOCF MAN	RW	NVM	Linear format two's complement mantissa. Refer to the table below. **Total channal OCP:** 0 A to 1023 A (PHASE = FFh). LSB = 1 A, no table is given below. **Per Phase OCL:** 17 A to 130 A (PHASE other than FF). Limited selections available, refer to the table below.

Attempts to write (46h) IOUT_OC_FAULT_LIMIT to any value outside those specified as valid, will be considered invalid/unsupported data and cause TPS536xx to respond by flagging the appropriate status bits, and notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

Command Resolution and NVM Store/Restore Behavior

The Per-PAGE (PHASE=FFh) IOUT_OC_FAULT_LIMIT is implemented using the TPS536xx internal telemetry system. As a result the value of this command may be programmed with very high resolution using the linear format. However, the TPS536xx provides only limited NVM-backed options for this command. Following a power-cycle or NVM Store/Restore operation, the value will be to the nearest reset LSB (1 A/LSB for this command), according to the value present during the last NVM store operation. During operation, updates to this

command with higher resolution this will be supported, and accepted as long as they fall between the minimum and maximum supported values given.

The Per-PHASE (PHASE != FFh) IOUT_OC_FAULT_LIMIT is implemented in analog hardware. The support values are given in the table below. Writes to this command of values between those supported values will be accepted and cast to the nearest supported value.

Phased Command Behavior

PHASE = 00h to (highest order phase assigned to the current page): Writes to (46h) IOUT_OC_FAULT_LIMIT modify the per-phase OCL threshold. Note this threshold is shared between all phases assigned to a channel. Reads to (46h) IOUT_OC_FAULT_LIMIT return the configured per-phase OCL for individual phases.

PHASE = 80h: Writes to (46h) IOUT_OC_FAULT_LIMIT modify the per-phase OCL for all individual phases. Reads to (46h) IOUT_OC_FAULT_LIMIT return the configured OCL threshold for the entire PAGE

PHASE = FFh: Writes to (46h) IOUT_OC_FAULT_LIMIT modify the total OCL for the entire PAGE . Reads to (46h) IOUT_OC_FAULT_LIMIT return the configured OCL of the entire PAGE .

Table 1-55. Supported Value Mapping

IOUT_OC_FAULT_LIMIT[PHASE=00h] (decoded)	Per-Phase OCL (A)	Nominal SLINEAR11 (hex)
IOUT_OC[PHASE=00h] < 17 A	Invalid/Unsupported	Invalid/Unsupported
17 A ≤ IOUT_OC[PHASE=00h] < 18.5 A	17	0011h
18.5 A ≤ IOUT_OC[PHASE=00h] < 21.5 A	20	0014h
21.5 A ≤ IOUT_OC[PHASE=00h] < 24.5 A	23	0017h
24.5 A ≤ IOUT_OC[PHASE=00h] < 27.5 A	26	001Ah
27.5 A ≤ IOUT_OC[PHASE=00h] < 30.5 A	29	001Dh
30.5 A ≤ IOUT_OC[PHASE=00h] < 33.5 A	32	0020h
33.5 A ≤ IOUT_OC[PHASE=00h] < 36.5 A	35	0023h
36.5 A ≤ IOUT_OC[PHASE=00h] < 39.5 A	38	0026h
39.5 A ≤ IOUT_OC[PHASE=00h] < 42.5 A	41	0029h
42.5 A ≤ IOUT_OC[PHASE=00h] < 45.5 A	44	002Ch
45.5 A ≤ IOUT_OC[PHASE=00h] < 48.5 A	47	002Fh
48.5 A ≤ IOUT_OC[PHASE=00h] < 51.5 A	50	0032h
51.5 A ≤ IOUT_OC[PHASE=00h] < 54.5 A	53	0035h
54.5 A ≤ IOUT_OC[PHASE=00h] < 57.5 A	56	0038h
57.5 A ≤ IOUT_OC[PHASE=00h] < 60.5 A	59	003Bh
60.5 A ≤ IOUT_OC[PHASE=00h] < 63.5 A	62	003Eh
63.5 A ≤ IOUT_OC[PHASE=00h] < 66.5 A	65	0041h
66.5 A ≤ IOUT_OC[PHASE=00h] < 69.5 A	68	0044h
69.5 A ≤ IOUT_OC[PHASE=00h] < 72.5 A	71	0047h
72.5 A ≤ IOUT_OC[PHASE=00h] < 75.5 A	74	004Ah
75.5 A ≤ IOUT_OC[PHASE=00h] < 78.5 A	77	004Dh
78.5 A ≤ IOUT_OC[PHASE=00h] < 82.5 A	80	0050h
82.5 A ≤ IOUT_OC[PHASE=00h] < 87.5 A	85	0055h
87.5 A ≤ IOUT_OC[PHASE=00h] < 92.5 A	90	005Ah
92.5 A ≤ IOUT_OC[PHASE=00h] < 97.5 A	95	005Fh
97.5 A ≤ IOUT_OC[PHASE=00h] < 102.5 A	100	0064h
102.5 A ≤ IOUT_OC[PHASE=00h] < 107.5 A	105	0069h
107.5 A ≤ IOUT_OC[PHASE=00h] < 112.5 A	110	006Eh
112.5 A ≤ IOUT_OC[PHASE=00h] < 117.5 A	115	0073h
117.5 A ≤ IOUT_OC[PHASE=00h] < 122.5 A	120	0078h

Table 1-55. Supported Value Mapping (continued)

IOUT_OC_FAULT_LIMIT[PHASE=00h] (decoded)	Per-Phase OCL (A)	Nominal SLINEAR11 (hex)
122.5 A ≤ IOUT_OC[PHASE=00h] < 127.5 A	125	007Dh
127.5 A ≤ IOUT_OC[PHASE=00h] ≤ 130 A	130	0082h
IOUT_OC[PHASE=00h] > 130 A	Invalid/Unsupported	Invalid/Unsupported

1.2.44 (47h) IOUT_OC_FAULT_RESPONSE

CMD Address	47h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
Paged:	Yes
Phased:	No
NVM Back-up:	EEPROM
Updates:	On-the-fly. Do not change during a fault shutdown event.

The IOUT_OC_FAULT_RESPONSE instructs the device on what action to take in response to a total-PAGE overcurrent fault. Upon triggering the per-page overcurrent fault, the TPS536xx responds according to the data byte below, and the following actions are taken:

- Set the IOUT_OC bit in the STATUS_BYTE ,
- Set the IOUT bit in the STATUS_WORD ,
- Set the IOUT_OCF bit in the STATUS_IOUT register
- Notify the host per PMBus 1.3.1 Part II specification, section 10.2.

(47h) IOUT_OC_FAULT_RESPONSE Register Map

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	R	R	R
IO OC RESP					0	0	0

LEGEND: R/W = Read/Write; R = Read only

Table 1-56. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:3	IO OC RESP	RW	NVM	Output over-current response. 00000b: Ignore. Continue operating without interruption. 11000b: Latch-off immediately. Shutdown and do not restart. Restart/clearing behavior is specified in the PMBus Specification v1.3, part II, section 10.7. 11111b: Hiccup immediately. shutdown and attempt to restart after 1 HICCUP time and repeat, until either the unit is commanded OFF, or a successful start-up retrial. Other: Invalid/Unsupported

Attempts to write (47h) IOUT_OC_FAULT_RESPONSE to any value outside those specified as valid, will be considered invalid/unsupported data and cause TPS536xx to respond by flagging the appropriate status bits, and notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

1.2.45 (4Ah) IOUT_OC_WARN_LIMIT

CMD Address	4Ah
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	SLINEAR11
Paged:	Yes
Phased:	No
NVM Back-up:	EEPROM
Updates:	On-the-fly

The IOUT_OC_WARN_LIMIT command sets the value of the output current, in amperes, that causes the over-current detector to indicate an over-current warning condition. The units are amperes. IOUT_OC_WARN_LIMIT is not a phased command. There is no per-phase overcurrent warning.

In response to an overcurrent warning condition, the TPS536xx takes the following action:

- Set the NONE OF THE ABOVE bit in the STATUS_BYTE ,
- Set the IOUT bit in the STATUS_WORD ,
- Set the IOUT_OCW bit in the STATUS_IOUT register
- Notify the host per PMBus 1.3.1 Part II specification, section 10.2.

(4Ah) IOUT_OC_WARN_LIMIT Register Map

15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
IOOCW EXP					IOOCW MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
IOOCW MAN							

LEGEND: R/W = Read/Write; R = Read only

Table 1-57. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:11	IOOCW EXP	RW	00000b	Linear format two's complement exponent.
10:0	IOOCW MAN	RW	NVM	Linear format two's complement mantissa. Refer to the table below. Supported values: 0 to 1023 A.

Attempts to write (4Ah) IOUT_OC_WARN_LIMIT to any value outside those specified as valid, will be considered invalid/unsupported data and cause TPS536xx to respond by flagging the appropriate status bits, and notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

Command Resolution and NVM Store/Restore Behavior

The Per-PAGE (PHASE=FFh) IOUT_OC_WARN_LIMIT is implemented using the TPS536xx internal telemetry system. As a result the value of this command may be programmed with very high resolution using the linear format. However, the TPS536xx provides only limited NVM-backed options for this command. Following a power-cycle or NVM Store/Restore operation, the value will be to the nearest reset LSB (1 A/LSB for this command), according to the value present during the last NVM store operation. During operation, updates to this command with higher resolution this will be supported, and accepted as long as they fall between the minimum and maximum supported values given.

1.2.46 (4Fh) OT_FAULT_LIMIT

CMD Address	4Fh
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	SLINEAR11
Paged:	Yes
Phased:	No
NVM Back-up:	EEPROM
Updates:	On-the-fly

The OT_FAULT_LIMIT command sets the value of the temperature limit, in degrees Celsius, that causes an over-temperature fault condition. This temperature limit is referenced to READ_TEMPERATURE_1 (Power Stage Temperature), which is telemetry data returned to the controller by the ATSEN/BTSEN pins of the power stage. There is no built-in hysteresis to this value. TI recommends to use either the latch-off or hiccup response setting rather than hysteretic response.

The converter response to an overtemperature event is described in OT_FAULT_RESPONSE .

(4Fh) OT_FAULT_LIMIT Register Map

15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
OTF EXP					OTF MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
OTF MAN							

LEGEND: R/W = Read/Write; R = Read only

Table 1-58. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:11	OTF EXP	RW	00000b	Linear format two's complement exponent.
10:0	OTF MAN	RW	NVM	Linear format two's complement mantissa. Refer to the text below.

Attempts to write (4Fh) OT_FAULT_LIMIT to any value outside those specified as valid, will be considered invalid/unsupported data and cause TPS536xx to respond by flagging the appropriate status bits, and notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

Command Resolution and NVM Store/Restore Behavior

The (4Fh) OT_FAULT_LIMIT command is implemented using the TPS536xx internal telemetry system. As a result the value of this command may be programmed with very high resolution using the linear format. However, the TPS536xx provides only limited NVM-backed options for this command. Following a power-cycle or NVM Store/Restore operation, the value will be restored to one of the values in the table below, according to the value present during the last NVM store operation. Refer to the table below. During operation, updates to this command with higher resolution than the options in the NVM supported table, will be supported, and accepted as long as they fall between the minimum and maximum supported values given.

Table 1-59. NVM Supported Values

OT_FAULT_LIMIT (decoded) during last NVM Store	Reset Value (decoded) OT Fault Limit (degC)	Nominal SLINEAR11 (hex)
OTF < 90 C	Invalid/Unsupported	Invalid/Unsupported
90 C ≤ OTF < 95 C	90	005Ah
95 C ≤ OTF < 105 C	100	0064h

Table 1-59. NVM Supported Values (continued)

OT_FAULT_LIMIT (decoded) during last NVM Store	Reset Value (decoded) OT Fault Limit (degC)	Nominal SLINEAR11 (hex)
105 C ≤ OTF < 115 C	110	006Eh
115 C ≤ OTF < 125 C	120	0078h
125 C ≤ OTF < 135 C	130	0082h
135 C ≤ OTF < 145 C	140	008Ch
145 C ≤ OTF < 155 C	150	0096h
155 C ≤ OTF < 160 C	160	00A0h
OTF > 160 C	Invalid/Unsupported	Invalid/Unsupported

1.2.47 (50h) OT_FAULT_RESPONSE

CMD Address	50h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
Paged:	Yes
Phased:	No
NVM Back-up:	EEPROM
Updates:	On-the-fly. Do not change during a fault shutdown event.

The OT_FAULT_RESPONSE command instructs the device on what action to take in response to an over temperature fault. Upon triggering the over-temperature fault, the converter responds per the data byte below, and the following actions are taken:

- Set the TEMP bit in the STATUS_BYTE ,
- Set the OTF bit in the STATUS_TEMPERATURE register
- Notify the host per PMBus 1.3.1 Part II specification, section 10.2

(50h) OT_FAULT_RESPONSE Register Map

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	R	R	R
OTF RESP					0	0	0

LEGEND: R/W = Read/Write; R = Read only

Table 1-60. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:3	OTF RESP	RW	NVM	Over-temperature fault response. 00000b: Ignore. Continue operating without interruption. 10000b: Latch-off immediately. Shutdown and do not restart. Restart/clearing behavior is specified in the PMBus Specification v1.3, part II, section 10.7. 10111b: Hiccup immediately. Shutdown, wait 1 HICCUP period and attempt to restart and repeat, until either the unit is commanded OFF, or a successful retrial. The HICCUP period is selected in MFR_PROTECTION_CONFIG. 11111b: Hysteresis only. Power conversion is disabled when the sensed temperature exceeds the overtemperature fault limit. The unit attempts to restart power conversion once the sensed temperature falls below the overtemperature fault limit. Other: Invalid/Unsupported

Attempts to write (50h) OT_FAULT_RESPONSE to any value outside those specified as valid, will be considered invalid/unsupported data and cause TPS536xx to respond by flagging the appropriate status bits, and notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

1.2.48 (51h) OT_WARN_LIMIT

CMD Address	51h
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	SLINEAR11
Paged:	Yes
Phased:	No
NVM Back-up:	EEPROM
Updates:	On-the-fly

The OT_WARN_LIMIT command sets the temperature of the unit at which level indicates an over-temperature warning alarm. The units are degrees C.

Upon triggering the over-temperature fault, the converter responds per the data byte below, and the following actions are taken:

- Set the TEMP bit in the STATUS_BYTE ,
- Set the OTF bit in the STATUS_TEMPERATURE register
- Notify the host per PMBus 1.3.1 Part II specification, section 10.2

(51h) OT_WARN_LIMIT Register Map

15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
OTW EXP					OTW MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
OTW MAN							

LEGEND: R/W = Read/Write; R = Read only

Table 1-61. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:11	OTW EXP	R	00000b	Linear format two's complement exponent. Exponent = 0, LSB = 1 °C
10:0	OTW MAN	RW	NVM	Linear format two's complement mantissa. Refer to the text below.

Attempts to write (51h) OT_WARN_LIMIT to any value outside those specified as valid, will be considered invalid/unsupported data and cause TPS536xx to respond by flagging the appropriate status bits, and notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

Command Resolution and NVM Store/Restore Behavior

The (51h) OT_WARN_LIMIT command is implemented using the TPS536xx internal telemetry system. As a result the value of this command may be programmed with very high resolution using the linear format. However, the TPS536xx provides only limited NVM-backed options for this command. Following a power-cycle or NVM Store/Restore operation, the value is restored to one of the values in the table below, according to the value present during the last NVM store operation. Refer to the table below. During operation, updates to this command with higher resolution than the options in the NVM supported table, are supported, and accepted as long as they fall between the minimum and maximum supported values given.

Table 1-62. NVM Supported Values

OT_WARN_LIMIT (decoded) during last NVM Store	Reset value (decoded) OT Warn Limit (degC)	Nominal SLINEAR11 (hex)
OTW < 90 C	Invalid/unsupported	Invalid/unsupported

Table 1-62. NVM Supported Values (continued)

OT_WARN_LIMIT (decoded) during last NVM Store	Reset value (decoded) OT Warn Limit (degC)	Nominal SLINEAR11 (hex)
90 C ≤ OTW < 95 C	90	005Ah
95 C ≤ OTW < 105 C	100	0064h
105 C ≤ OTW < 115 C	110	006Eh
115 C ≤ OTW < 125 C	120	0078h
125 C ≤ OTW < 135 C	130	0082h
135 C ≤ OTW < 145 C	140	008Ch
145 C ≤ OTW < 155 C	150	0096h
155 C ≤ OTW ≤ 160 C	160	00A0h
OTW > 160 C	Invalid	Invalid/unsupported

1.2.49 (55h) VIN_OV_FAULT_LIMIT

CMD Address	55h
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	SLINEAR11
Paged:	No
Phased:	No
NVM Back-up:	EEPROM
Updates:	On-the-fly

The VIN_OV_FAULT_LIMIT command sets the value, in Volts, of the input voltage that causes an input overvoltage fault.

The converter response to the VIN_OV_FAULT event is described in VIN_OV_FAULT_RESPONSE .

(55h) VIN_OV_FAULT_LIMIT Register Map

15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
VIN OVF EXP					VIN OVF MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VIN OVF MAN							

LEGEND: R/W = Read/Write; R = Read only

Table 1-63. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:11	VI OVF EXP	RW	00000b	Linear format two's complement exponent.
10:0	VI OVF MAN	RW	NVM	Linear format two's complement mantissa. Refer to the table below.

Attempts to write (55h) VIN_OV_FAULT_LIMIT to any value outside those specified as valid, will be considered invalid/unsupported data and cause TPS536xx to respond by flagging the appropriate status bits, and notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

Command Resolution and NVM Store/Restore Behavior

The (55h) VIN_OV_FAULT_LIMIT command is implemented using the TPS536xx internal telemetry system. As a result the value of this command may be programmed with very high resolution using the linear format. However, the TPS536xx provides only limited NVM-backed options for this command. Following a power-cycle or NVM Store/Restore operation, the value will be restored to one of the values in the table below, according to the value present during the last NVM store operation. Refer to the table below. During operation, updates to this command with higher resolution than the options in the NVM supported table, will be supported, and accepted as long as they fall between the minimum and maximum supported values given.

Table 1-64. NVM-Supported Value Mapping

VIN_OV_FAULT_LIMIT (decoded) during last NVM Store	Reset value (decoded) VIN Over-Voltage Threshold (V)	Nominal SLINEAR11 (hex)
0 V ≤ VIN OVF < 0.5 V	0	0000h
0.5 V ≤ VIN OVF < 1.5 V	1	0001h
1.5 V ≤ VIN OVF < 2.5 V	2	0002h
2.5 V ≤ VIN OVF < 3.5 V	3	0003h
3.5 V ≤ VIN OVF < 4.5 V	4	0004h

Table 1-64. NVM-Supported Value Mapping (continued)

VIN_OV_FAULT_LIMIT (decoded) during last NVM Store	Reset value (decoded) VIN Over-Voltage Threshold (V)	Nominal SLINEAR11 (hex)
4.5 V ≤ VIN OVF < 5.5 V	5	0005h
5.5 V ≤ VIN OVF < 6.5 V	6	0006h
6.5 V ≤ VIN OVF < 7.5 V	7	0007h
7.5 V ≤ VIN OVF < 8.5 V	8	0008h
8.5 V ≤ VIN OVF < 9.5 V	9	0009h
9.5 V ≤ VIN OVF < 10.5 V	10	000Ah
10.5 V ≤ VIN OVF < 11.5 V	11	000Bh
11.5 V ≤ VIN OVF < 12.5 V	12	000Ch
12.5 V ≤ VIN OVF < 13.5 V	13	000Dh
13.5 V ≤ VIN OVF < 14.5 V	14	000Eh
14.5 V ≤ VIN OVF < 15.5 V	15	000Fh
15.5 V ≤ VIN OVF < 16.5 V	16	0010h
16.5 V ≤ VIN OVF < 17.5 V	17	0011h
17.5 V ≤ VIN OVF < 18.5 V	18	0012h
18.5 V ≤ VIN OVF ≤ 19.0 V	19	0013h
VIN OVF > 19.0 V	Invalid/Unsupported	Invalid/Unsupported

1.2.50 (56h) VIN_OV_FAULT_RESPONSE

CMD Address	56h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
Paged:	No
Phased:	No
NVM Back-up:	EEPROM
Updates:	On-the-fly. Do not change during a fault shutdown event.

The VIN_OV_FAULT_RESPONSE instructs the device on what action to take in response to an input over-voltage fault. Upon triggering the over-voltage fault, the converter responds per the byte below and the following actions are taken:

- Set the NONE OF THE ABOVE bit in the STATUS_BYTE
- Set the INPUT bit in the STATUS_WORD
- Set the VIN OVF bit in STATUS_INPUT
- Notify the host per PMBus 1.3.1 Part II specification, section 10.2

(56h) VIN_OV_FAULT_RESPONSE Register Map

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	R	R	R
VIOV RESP					0	0	0

LEGEND: R/W = Read/Write; R = Read only

Table 1-65. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:3	VIOV RESP	RW	NVM	Input over-voltage response. 00000b: Ignore. Continue operating without interruption. 10000b: Latch-off immediately. Shutdown and do not restart. Restart/clearing behavior is specified in the PMBus Specification v1.3, part II, section 10.7. 10111b: Hiccup immediately. Shutdown, wait 1 HICCUP period and attempt to restart and repeat, until either the unit is commanded OFF, or a successful retrial. The HICCUP time is selected in MFR_PROTECTION_CONFIG. Other: Invalid/Unsupported

Attempts to write (56h) VIN_OV_FAULT_RESPONSE to any value outside those specified as valid, will be considered invalid/unsupported data and cause TPS536xx to respond by flagging the appropriate status bits, and notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

1.2.51 (57h) VIN_OV_WARN_LIMIT

CMD Address	57h
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	SLINEAR11
Paged:	No
Phased:	No
NVM Back-up:	EEPROM
Updates:	On-the-fly

The VIN_OV_WARN_LIMIT command sets the value, in Volts, of the input voltage that causes an input overvoltage warning. When the sensed input voltage exceeds the VIN_OV_WARN_LIMIT , the converter responds as follows:

- Set the NONE OF THE ABOVE bit in the STATUS_BYTE
- Set the INPUT bit in the STATUS_WORD
- Set the VIN OVW bit in STATUS_INPUT
- Notify the host per PMBus 1.3.1 Part II specification, section 10.2

(57h) VIN_OV_WARN_LIMIT Register Map

15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
VIN OVW EXP					VIN OVW MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VIN OVW MAN							

LEGEND: R/W = Read/Write; R = Read only

Table 1-66. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:11	VIN OVW EXP	RW	00000b	Linear format two's complement exponent.
10:0	VIN OVW MAN	RW	NVM	Linear format two's complement mantissa.

Attempts to write (57h) VIN_OV_WARN_LIMIT to any value outside those specified as valid, will be considered invalid/unsupported data and cause TPS536xx to respond by flagging the appropriate status bits, and notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

Command Resolution and NVM Store/Restore Behavior

The (57h) VIN_OV_WARN_LIMIT command is implemented using the TPS536xx internal telemetry system. As a result the value of this command may be programmed with very high resolution using the linear format. However, the TPS536xx provides only limited NVM-backed options for this command. Following a power-cycle or NVM Store/Restore operation, the value will be restored to one of the values in the table below, according to the value present during the last NVM store operation. Refer to the table below. During operation, updates to this command with higher resolution than the options in the NVM supported table, will be supported, and accepted as long as they fall between the minimum and maximum supported values given.

Table 1-67. NVM Supported Values

VIN_OV_WARN_LIMIT (decoded) during last NVM Store	Reset Value (decoded) VIN Over-Voltage Warning Threshold (V)	Nominal SLINEAR11 (hex)
0 V ≤ VIN OVW < 0.5 V	0	0000h
0.5 V ≤ VIN OVW < 1.5 V	1	0001h
1.5 V ≤ VIN OVW < 2.5 V	2	0002h
2.5 V ≤ VIN OVW < 3.5 V	3	0003h
3.5 V ≤ VIN OVW < 4.5 V	4	0004h
4.5 V ≤ VIN OVW < 5.5 V	5	0005h
5.5 V ≤ VIN OVW < 6.5 V	6	0006h
6.5 V ≤ VIN OVW < 7.5 V	7	0007h
7.5 V ≤ VIN OVW < 8.5 V	8	0008h
8.5 V ≤ VIN OVW < 9.5 V	9	0009h
9.5 V ≤ VIN OVW < 10.5 V	10	000Ah
10.5 V ≤ VIN OVW < 11.5 V	11	000Bh
11.5 V ≤ VIN OVW < 12.5 V	12	000Ch
12.5 V ≤ VIN OVW < 13.5 V	13	000Dh
13.5 V ≤ VIN OVW < 14.5 V	14	000Eh
14.5 V ≤ VIN OVW < 15.5 V	15	000Fh
15.5 V ≤ VIN OVW < 16.5 V	16	0010h
16.5 V ≤ VIN OVW < 17.5 V	17	0011h
17.5 V ≤ VIN OVW < 18.5 V	18	0012h
18.5 V ≤ VIN OVW ≤ 19.0 V	19	0013h
VIN OVW > 19.0 V	Invalid/Unsupported	Invalid/Unsupported

1.2.52 (58h) VIN_UV_WARN_LIMIT

CMD Address	58h
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	SLINEAR11
Paged:	No
Phased:	No
NVM Back-up:	EEPROM
Updates:	On-the-fly

The VIN_UV_WARN_LIMIT command sets the value, in Volts, of the input voltage that causes an input undervoltage warning. When the sensed input voltage falls below the VIN_UV_WARN_LIMIT , the converter responds as follows:

- Set the NONE OF THE ABOVE bit in the STATUS_BYTE
- Set the INPUT bit in the STATUS_WORD
- Set the VIN_UVW bit in STATUS_INPUT
- Notify the host per PMBus 1.3.1 Part II specification, section 10.2

The VIN_UVW warning condition is masked until the sensed input voltage exceeds the VIN_ON value and the VIN_UV_WARN_LIMIT for the first time.

(58h) VIN_UV_WARN_LIMIT Register Map

15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
VIN UVW EXP					VIN UVW MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VIN UVW MAN							

LEGEND: R/W = Read/Write; R = Read only

Table 1-68. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:11	VIN UVW EXP	RW	11110b	Linear format two's complement exponent.
10:0	VIN UVW MAN	RW	NVM	Linear format two's complement mantissa. Refer to the table below.

Attempts to write (58h) VIN_UV_WARN_LIMIT to any value outside those specified as valid, will be considered invalid/unsupported data and cause TPS536xx to respond by flagging the appropriate status bits, and notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

Command Resolution and NVM Store/Restore Behavior

The (58h) VIN_UV_WARN_LIMIT command is implemented using the TPS536xx internal telemetry system. As a result the value of this command may be programmed with very high resolution using the linear format. However, the TPS536xx provides only limited NVM-backed options for this command. Following a power-cycle or NVM Store/Restore operation, the value will be restored to one of the values in the table below, according to the value present during the last NVM store operation. Refer to the table below. During operation, updates to this command with higher resolution than the options in the NVM supported table, will be supported, and accepted as long as they fall between the minimum and maximum supported values given.

Table 1-69. NVM Supported Value Mapping

VIN_OV_WARN_LIMIT (decoded) during last NVM Store	Reset value (decoded) VIN Over-Voltage Warning Threshold (V)	Nominal SLINEAR11 (hex)
VIN UVW < 4 V	Invalid/Unsupported	Invalid/Unsupported
4 V ≤ VIN UVW < 4.125 V	4.00	F010h
4.125 V ≤ VIN UVW < 4.375 V	4.25	F011h
4.375 V ≤ VIN UVW < 4.625 V	4.50	F012h
4.625 V ≤ VIN UVW < 4.875 V	4.75	F013h
4.875 V ≤ VIN UVW < 5.125 V	5.00	F014h
5.125 V ≤ VIN UVW < 5.375 V	5.25	F015h
5.375 V ≤ VIN UVW < 5.625 V	5.50	F016h
5.625 V ≤ VIN UVW < 5.875 V	5.75	F017h
5.875 V ≤ VIN UVW < 6.125 V	6.00	F018h
6.125 V ≤ VIN UVW < 6.375 V	6.25	F019h
6.375 V ≤ VIN UVW < 6.625 V	6.50	F01Ah
6.625 V ≤ VIN UVW < 6.875 V	6.75	F01Bh
6.875 V ≤ VIN UVW < 7.125 V	7.00	F01Ch
7.125 V ≤ VIN UVW < 7.375 V	7.25	F01Dh
7.375 V ≤ VIN UVW < 7.625 V	7.50	F01Eh
7.625 V ≤ VIN UVW < 7.875 V	7.75	F01Fh
7.875 V ≤ VIN UVW < 8.125 V	8.00	F020h
8.125 V ≤ VIN UVW < 8.375 V	8.25	F021h
8.375 V ≤ VIN UVW < 8.625 V	8.50	F022h
8.625 V ≤ VIN UVW < 8.875 V	8.75	F023h
8.875 V ≤ VIN UVW < 9.125 V	9.00	F024h
9.125 V ≤ VIN UVW < 9.375 V	9.25	F025h
9.375 V ≤ VIN UVW < 9.625 V	9.50	F026h
9.625 V ≤ VIN UVW < 9.875 V	9.75	F027h
9.875 V ≤ VIN UVW < 10.125 V	10.00	F028h
10.125 V ≤ VIN UVW < 10.375 V	10.25	F029h
10.375 V ≤ VIN UVW < 10.625 V	10.50	F02Ah
10.625 V ≤ VIN UVW < 10.875 V	10.75	F02Bh
10.875 V ≤ VIN UVW < 11.125 V	11.00	F02Ch
11.125 V ≤ VIN UVW ≤ 11.25 V	11.25	F02Dh
VIN UVW > 11.25 V	Invalid/Unsupported	Invalid/Unsupported

1.2.53 (59h) VIN_UV_FAULT_LIMIT

CMD Address	59h
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	SLINEAR11
Paged:	No
Phased:	No
NVM Back-up:	EEPROM
Updates:	On-the-fly

The VIN_UV_FAULT_LIMIT command sets the value, in Volts, of the input voltage that causes an input undervoltage warning. This command is a shadow register for VIN_OFF . Updates to VIN_UV_FAULT_LIMIT also update VIN_OFF . Likewise, updates to VIN_OFF also update VIN_UV_FAULT_LIMIT .

The VIN_UV_FAULT condition is masked until the first time the sensed input voltage exceeds the VIN_ON and VIN_UV_FAULT_LIMIT thresholds.

(59h) VIN_UV_FAULT_LIMIT Register Map

15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
VIN UVF EXP					VIN UVF MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VIN UVF MAN							

LEGEND: R/W = Read/Write; R = Read only

Table 1-70. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:11	VIN UVF EXP	RW	11110b	Linear format two's complement exponent.
10:0	VIN UVF MAN	RW	NVM	Linear format two's complement mantissa.

Attempts to write (59h) VIN_UV_FAULT_LIMIT will be considered invalid/unsupported command and cause TPS536xx to respond by flagging the appropriate status bits, and notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

Table 1-71. NVM-Supported Values

VIN_OFF (decoded) during last NVM Store	VIN_OFF Reset value (decoded) following Reset/Restore (V)	Nominal SLINEAR11 (hex)
Less than 4 V	Invalid/Unsupported	Invalid/Unsupported
4 ≤ VIN UVF < 4.125 V	4.00	F010h
4.125 ≤ VIN UVF < 4.375 V	4.25	F011h
4.375 ≤ VIN UVF < 4.625 V	4.50	F012h
4.625 ≤ VIN UVF < 4.875 V	4.75	F013h
4.875 ≤ VIN UVF < 5.125 V	5.00	F014h
5.125 ≤ VIN UVF < 5.375 V	5.25	F015h
5.375 ≤ VIN UVF < 5.625 V	5.50	F016h
5.625 ≤ VIN UVF < 5.875 V	5.75	F017h
5.875 ≤ VIN UVF < 6.125 V	6.00	F018h

Table 1-71. NVM-Supported Values (continued)

VIN_OFF (decoded) during last NVM Store	VIN_OFF Reset value (decoded) following Reset/Restore (V)	Nominal SLINEAR11 (hex)
6.125 ≤ VIN UVF < 6.375 V	6.25	F019h
6.375 ≤ VIN UVF < 6.625 V	6.50	F01Ah
6.625 ≤ VIN UVF < 6.875 V	6.75	F01Bh
6.875 ≤ VIN UVF < 7.125 V	7.00	F01Ch
7.125 ≤ VIN UVF < 7.375 V	7.25	F01Dh
7.375 ≤ VIN UVF < 7.625 V	7.50	F01Eh
7.625 ≤ VIN UVF < 7.875 V	7.75	F01Fh
7.875 ≤ VIN UVF < 8.125 V	8.00	F020h
8.125 ≤ VIN UVF < 8.375 V	8.25	F021h
8.375 ≤ VIN UVF < 8.625 V	8.50	F022h
8.625 ≤ VIN UVF < 8.875 V	8.75	F023h
8.875 ≤ VIN UVF < 9.125 V	9.00	F024h
9.125 ≤ VIN UVF < 9.375 V	9.25	F025h
9.375 ≤ VIN UVF < 9.625 V	9.50	F026h
9.625 ≤ VIN UVF < 9.875 V	9.75	F027h
9.875 ≤ VIN UVF < 10.125 V	10.00	F028h
10.125 ≤ VIN UVF < 10.375 V	10.25	F029h
10.375 ≤ VIN UVF < 10.625 V	10.50	F02Ah
10.625 ≤ VIN UVF < 10.875 V	10.75	F02Bh
10.875 ≤ VIN UVF < 11.125 V	11.00	F02Ch
11.125 ≤ VIN UVF ≤ 11.25 V	11.25	F02Dh
Greater than 11.25 V	Invalid/unsupported	Invalid/Unsupported

Command Resolution and NVM Store/Restore Behavior

The (59h) VIN_UV_FAULT_LIMIT command is implemented using the TPS536xx internal telemetry system. As a result the value of this command may be programmed with very high resolution using the linear format. However, the TPS536xx provides only limited NVM-backed options for this command. Following a power-cycle or NVM Store/Restore operation, the value will be restored to one of the values in the table below, according to the value present during the last NVM store operation. Refer to the table below. During operation, updates to this command with higher resolution than the options in the NVM supported table, will be supported, and accepted as long as they fall between the minimum and maximum supported values given.

1.2.54 (5Ah) VIN_UV_FAULT_RESPONSE

CMD Address	5Ah
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
Paged:	No
Phased:	No
NVM Back-up:	EEPROM
Updates:	On-the-fly. Do not change during a fault shutdown event.

The VIN_UV_FAULT_RESPONSE instructs the device on what action to take in response to an input under-voltage fault. Upon triggering the input under-voltage fault, the converter responds per the byte below and the following actions are taken:

- Set the VIN_UVF bit in the STATUS_BYTE
- Set the INPUT bit in the STATUS_WORD
- Set the VIN_UVF bit in STATUS_INPUT
- Notify the host per PMBus 1.3.1 Part II specification, section 10.2

The VIN_UV_FAULT_LIMIT fault is masked until the first time the sensed input voltage exceeds the VIN_ON and VIN_UV_FAULT_LIMIT thresholds. Note that regardless of the VIN_UV_FAULT_RESPONSE and VIN_UV_FAULT_LIMIT setting, when the sensed input voltage falls below the minimum VIN_OFF setting of 4.0 V, the TPS536xx stops power conversion.

(5Ah) VIN_UV_FAULT_RESPONSE Register Map

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	R	R	R
VIN UV RESP					0	0	0

LEGEND: R/W = Read/Write; R = Read only

Table 1-72. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:3	VIN UV RESP	RW	NVM	Input under-voltage response. 00000b: Ignore. Continue operating without interruption. 10000b: Latch-off immediately. Shutdown and do not restart. Restart/clearing behavior is specified in the PMBus Specification v1.3, part II, section 10.7. 10111b: Hiccup immediately. Shutdown, wait 1 HICCUP period and attempt to restart and repeat, until either the unit is commanded OFF, or a successful retrial. The HICCUP time is selected in MFR_PROTECTION_CONFIG. Other: Invalid/Unsupported

Attempts to write (5Ah) VIN_UV_FAULT_RESPONSE to any value outside those specified as valid, will be considered invalid/unsupported data and cause TPS536xx to respond by flagging the appropriate status bits, and notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

1.2.55 (5Bh) IIN_OC_FAULT_LIMIT

CMD Address	5Bh
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	SLINEAR11
Paged:	No
Phased:	No
NVM Back-up:	EEPROM
Updates:	On-the-fly

The IIN_OC_FAULT_LIMIT command sets the value of the input current, in Amperes, that causes an Input overcurrent fault. When the IIN_OC_FAULT condition is triggered the TPS536xx responds according to IIN_OC_FAULT_RESPONSE .

(5Bh) IIN_OC_FAULT_LIMIT Register Map

15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
IIOCF EXP					IIOCF MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
IIOCF MAN							

LEGEND: R/W = Read/Write; R = Read only

Table 1-73. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:11	IIOCF EXP	RW	00000b	Linear two's complement exponent.
10:0	IIOCF MAN	RW	NVM	Linear format two's complement mantissa.

Attempts to write (5Bh) IIN_OC_FAULT_LIMIT to any value other than those specified as valid will be considered invalid/unsupported command and cause TPS536xx to respond by flagging the appropriate status bits, and notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3

Command Resolution and NVM Store/Restore Behavior

The (5Bh) IIN_OC_FAULT_LIMIT command is implemented using the TPS536xx internal telemetry system. As a result the value of this command may be programmed with very high resolution using the linear format. However, the TPS536xx provides only limited NVM-backed options for this command. Following a power-cycle or NVM Store/Restore operation, the value will be restored to one of the values in the table below, according to the value present during the last NVM store operation. Refer to the table below. During operation, updates to this command with higher resolution than the options in the NVM supported table, will be supported, and accepted as long as they fall between the minimum and maximum supported values given.

Table 1-74. NVM Supported Values

IIN_OC_FAULT_LIMIT (decoded) during last NVM Store	Reset value (decoded) Input OC Fault Threshold (A)	Nominal SLINEAR11 (hex)
IIN OCF < 4A	Invalid/Unsupported	Invalid/Unsupported
4 A ≤ IIN OCF < 6 A	4	0004h
6 A ≤ IIN OCF < 10 A	8	0008h
10 A ≤ IIN OCF < 14 A	12	000Ch
14 A ≤ IIN OCF < 18 A	16	0010h
18 A ≤ IIN OCF < 22 A	20	0014h

Table 1-74. NVM Supported Values (continued)

IIN_OC_FAULT_LIMIT (decoded) during last NVM Store	Reset value (decoded) Input OC Fault Threshold (A)	Nominal SLINEAR11 (hex)
22 A ≤ IIN OCF < 26 A	24	0018h
26 A ≤ IIN OCF < 30 A	28	001Ch
30 A ≤ IIN OCF < 34 A	32	0020h
34 A ≤ IIN OCF < 38 A	36	0024h
38 A ≤ IIN OCF < 42 A	40	0028h
42 A ≤ IIN OCF < 46 A	44	002Ch
46 A ≤ IIN OCF < 50 A	48	0030h
50 A ≤ IIN OCF < 54 A	52	0034h
54 A ≤ IIN OCF < 58 A	56	0038h
58 A ≤ IIN OCF < 62 A	60	003Ch
62 A ≤ IIN OCF < 66 A	64	0040h
66 A ≤ IIN OCF < 70 A	68	0044h
70 A ≤ IIN OCF < 74 A	72	0048h
74 A ≤ IIN OCF < 78 A	76	004Ch
78 A ≤ IIN OCF < 82 A	80	0050h
82 A ≤ IIN OCF < 86 A	84	0054h
86 A ≤ IIN OCF < 90 A	88	0058h
90 A ≤ IIN OCF < 94 A	92	005Ch
94 A ≤ IIN OCF < 98 A	96	0060h
98 A ≤ IIN OCF < 102 A	100	0064h
102 A ≤ IIN OCF < 106 A	104	0068h
106 A ≤ IIN OCF < 110 A	108	006Ch
110 A ≤ IIN OCF < 114 A	112	0070h
114 A ≤ IIN OCF < 118 A	116	0074h
118 A ≤ IIN OCF < 122 A	120	0078h
122 A ≤ IIN OCF < 126 A	124	007Ch
126 A ≤ IIN OCF ≤ 128 A	128	0080h
IIN OCF > 128 A	Invalid/Unsupported	Invalid/Unsupported

1.2.56 (5Ch) IIN_OC_FAULT_RESPONSE

CMD Address	5Ch
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	Unsigned Binary (1 byte)
Paged:	No
Phased:	No
NVM Back-up:	EEPROM
Updates:	On-the-fly. Do not change during a fault shutdown response.

The IIN_OC_FAULT_RESPONSE instructs the device on what action to take in response to an input overcurrent fault. Upon triggering the input overcurrent fault, the converter responds per the byte below and the following actions are taken:

- Set the NONE OF THE ABOVE bit in the STATUS_BYTE
- Set the INPUT bit in the STATUS_WORD
- Set the IIN_OCF bit in STATUS_INPUT
- Notify the host per PMBus 1.3.1 Part II specification, section 10.2

(5Ch) IIN_OC_FAULT_RESPONSE Register Map

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	R	R	R
IIOC RESP					0	0	0

LEGEND: R/W = Read/Write; R = Read only

Table 1-75. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:3	IIOC RESP	RW	NVM	Input under-voltage response. 00000b: Ignore. Continue operating without interruption. 11000b: Latch-off immediately. Shutdown and do not restart. Restart/clearing behavior is specified in the PMBus Specification v1.3, part II, section 10.7. 11111b: Hiccup immediately. Shutdown, wait 1 HICCUP period and attempt to restart and repeat, until either the unit is commanded OFF, or a successful retrial. The HICCUP time is selected in MFR_PROTECTION_CONFIG. Other: Invalid/Unsupported

Attempts to write (5Ch) IIN_OC_FAULT_RESPONSE to any value outside those specified as valid, will be considered invalid/unsupported data and cause TPS536xx to respond by flagging the appropriate status bits, and notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

1.2.57 (5Dh) IIN_OC_WARN_LIMIT

CMD Address	5Dh
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	SLINEAR11
Paged:	No.
Phased:	No
NVM Back-up:	EEPROM
Updates:	On-the-fly

The IIN_OC_WARN_LIMIT command sets the value of the input current, in Amperes, that causes an Input Overcurrent warning. When the IIN_OC_WARN condition is triggered the TPS536xx responds as follows:

- Set the NONE OF THE ABOVE bit in the STATUS_BYTE
- Set the INPUT bit in the STATUS_WORD
- Set the IIN OCW bit in STATUS_INPUT
- Notify the host per PMBus 1.3.1 Part II specification, section 10.2

(5Dh) IIN_OC_WARN_LIMIT Register Map

15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
IIOCW EXP					IIOCW MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
IIOCW MAN							

LEGEND: R/W = Read/Write; R = Read only

Table 1-76. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:11	IIOCW EXP	RW	00000b	Linear two's complement exponent.
10:0	IIOCW MAN	RW	NVM	Linear format two's complement mantissa.

Attempts to write (5Dh) IIN_OC_WARN_LIMIT to any value other than those specified as valid will be considered invalid/unsupported command and cause TPS536xx to respond by flagging the appropriate status bits, and notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

Command Resolution and NVM Store/Restore Behavior

The (5Dh) IIN_OC_WARN_LIMIT command is implemented using the TPS536xx internal telemetry system. As a result the value of this command may be programmed with very high resolution using the linear format. However, the TPS536xx provides only limited NVM-backed options for this command. Following a power-cycle or NVM Store/Restore operation, the value will be restored to one of the values in the table below, according to the value present during the last NVM store operation. Refer to the table below. During operation, updates to this command with higher resolution than the options in the NVM supported table, will be supported, and accepted as long as they fall between the minimum and maximum supported values given.

Table 1-77. NVM Supported Values

IIN_OC_WARN_LIMIT (decoded) during last NVM Store	Reset value (decoded) Input OC Warn Threshold (A)	Nominal SLINEAR11 (hex)
IIN OCW < 4A	Invalid/Unsupported	Invalid/Unsupported
4 A ≤ IIN OCW < 6 A	4	0004h
6 A ≤ IIN OCW < 10 A	8	0008h

Table 1-77. NVM Supported Values (continued)

IIN_OC_WARN_LIMIT (decoded) during last NVM Store	Reset value (decoded) Input OC Warn Threshold (A)	Nominal SLINEAR11 (hex)
10 A ≤ IIN OCW < 14 A	12	000Ch
14 A ≤ IIN OCW < 18 A	16	0010h
18 A ≤ IIN OCW < 22 A	20	0014h
22 A ≤ IIN OCW < 26 A	24	0018h
26 A ≤ IIN OCW < 30 A	28	001Ch
30 A ≤ IIN OCW < 34 A	32	0020h
34 A ≤ IIN OCW < 38 A	36	0024h
38 A ≤ IIN OCW < 42 A	40	0028h
42 A ≤ IIN OCW < 46 A	44	002Ch
46 A ≤ IIN OCW < 50 A	48	0030h
50 A ≤ IIN OCW < 54 A	52	0034h
54 A ≤ IIN OCW < 58 A	56	0038h
58 A ≤ IIN OCW < 62 A	60	003Ch
62 A ≤ IIN OCW < 66 A	64	0040h
66 A ≤ IIN OCW < 70 A	68	0044h
70 A ≤ IIN OCW < 74 A	72	0048h
74 A ≤ IIN OCW < 78 A	76	004Ch
78 A ≤ IIN OCW < 82 A	80	0050h
82 A ≤ IIN OCW < 86 A	84	0054h
86 A ≤ IIN OCW < 90 A	88	0058h
90 A ≤ IIN OCW < 94 A	92	005Ch
94 A ≤ IIN OCW < 98 A	96	0060h
98 A ≤ IIN OCW < 102 A	100	0064h
102 A ≤ IIN OCW < 106 A	104	0068h
106 A ≤ IIN OCW < 110 A	108	006Ch
110 A ≤ IIN OCW < 114 A	112	0070h
114 A ≤ IIN OCW < 118 A	116	0074h
118 A ≤ IIN OCW < 122 A	120	0078h
122 A ≤ IIN OCW < 126 A	124	007Ch
126 A ≤ IIN OCW ≤ 128 A	128	0080h
IIN OCW > 128 A	Invalid/Unsupported	Invalid/Unsupported

1.2.58 (60h) TON_DELAY

CMD Address	60h
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	SLINEAR11
Paged:	Yes
Phased:	No
NVM Back-up:	EEPROM
Updates:	On-the-fly

The TON_DELAY command sets the time, in milliseconds, from when a start condition is received (as programmed by the ON_OFF_CONFIG command) until the output voltage starts to rise. Note that TPS536xx requires approximately 500 µs from the moment it is commanded to enable power conversion, to the beginning of switching activity. Delay added by TON_DELAY is in addition to this.

(60h) TON_DELAY Register Map

15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
TONDLY EXP					TONDLY MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
TONDLY MAN							

LEGEND: R/W = Read/Write; R = Read only

Table 1-78. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:11	TONDLY EXP	RW	11111b	Linear format two's complement exponent.
10:0	TONDLY MAN	RW	NVM	Linear format two's complement mantissa.

Attempts to write (60h) TON_DELAY will be considered invalid/unsupported command and cause TPS536xx to respond by flagging the appropriate status bits, and notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

Table 1-79. Supported Value Mapping

TON_DELAY (decoded)	Turn-on Delay (ms)	Nominal SLINEAR11 (hex)
TON_DELAY = 0 ms	As fast as possible(< 0.1 ms)	F800h
0 ms < TONDLY < 0.75 ms	0.50	F801h
0.75 ms ≤ TONDLY < 1.25 ms	1.00	F802h
1.25 ms ≤ TONDLY < 1.75 ms	1.50	F803h
1.75 ms ≤ TONDLY < 2.25 ms	2.00	F804h
2.25 ms ≤ TONDLY < 2.75 ms	2.50	F805h
2.75 ms ≤ TONDLY < 3.25 ms	3.00	F806h
3.25 ms ≤ TONDLY < 3.75 ms	3.50	F807h
3.75 ms ≤ TONDLY < 4.25 ms	4.00	F808h
4.25 ms ≤ TONDLY < 4.75 ms	4.50	F809h
4.75 ms ≤ TONDLY < 5.25 ms	5.00	F80Ah
5.25 ms ≤ TONDLY < 5.75 ms	5.50	F80Bh

Table 1-79. Supported Value Mapping (continued)

TON_DELAY (decoded)	Turn-on Delay (ms)	Nominal SLINEAR11 (hex)
5.75 ms ≤ TONDLY < 6.25 ms	6.00	F80Ch
6.25 ms ≤ TONDLY < 6.75 ms	6.50	F80Dh
6.75 ms ≤ TONDLY < 7.25 ms	7.00	F80Eh
7.25 ms ≤ TONDLY < 7.75 ms	7.50	F80Fh
7.75 ms ≤ TONDLY < 8.25 ms	8.00	F810h
8.25 ms ≤ TONDLY < 8.75 ms	8.50	F811h
8.75 ms ≤ TONDLY < 9.25 ms	9.00	F812h
9.25 ms ≤ TONDLY < 9.75 ms	9.50	F813h
9.75 ms ≤ TONDLY < 10.25 ms	10.00	F814h
10.25 ms ≤ TONDLY < 10.75 ms	10.50	F815h
10.75 ms ≤ TONDLY < 11.25 ms	11.00	F816h
11.25 ms ≤ TONDLY < 11.75 ms	11.50	F817h
11.75 ms ≤ TONDLY < 12.25 ms	12.00	F818h
12.25 ms ≤ TONDLY < 12.75 ms	12.50	F819h
12.75 ms ≤ TONDLY < 13.25 ms	13.00	F81Ah
13.25 ms ≤ TONDLY < 13.75 ms	13.50	F81Bh
13.75 ms ≤ TONDLY < 14.25 ms	14.00	F81Ch
14.25 ms ≤ TONDLY < 14.75 ms	14.50	F81Dh
14.75 ms ≤ TONDLY < 15.25 ms	15.00	F81Eh
15.25 ms ≤ TONDLY < 15.75 ms	15.50	F81Fh
15.75 ms ≤ TONDLY < 16.25 ms	16.00	F820h
16.25 ms ≤ TONDLY < 16.75 ms	16.50	F821h
16.75 ms ≤ TONDLY < 17.25 ms	17.00	F822h
17.25 ms ≤ TONDLY < 17.75 ms	17.50	F823h
17.75 ms ≤ TONDLY < 18.25 ms	18.00	F824h
18.25 ms ≤ TONDLY < 18.75 ms	18.50	F825h
18.75 ms ≤ TONDLY < 19.25 ms	19.00	F826h
19.25 ms ≤ TONDLY < 19.75 ms	19.50	F827h
19.75 ms ≤ TONDLY < 20.25 ms	20.00	F828h
20.25 ms ≤ TONDLY < 20.75 ms	20.50	F829h
20.75 ms ≤ TONDLY < 21.25 ms	21.00	F82Ah
21.25 ms ≤ TONDLY < 21.75 ms	21.50	F82Bh
21.75 ms ≤ TONDLY < 22.25 ms	22.00	F82Ch
22.25 ms ≤ TONDLY < 22.75 ms	22.50	F82Dh
22.75 ms ≤ TONDLY < 23.25 ms	23.00	F82Eh
23.25 ms ≤ TONDLY < 23.75 ms	23.50	F82Fh
23.75 ms ≤ TONDLY < 24.25 ms	24.00	F830h
24.25 ms ≤ TONDLY < 24.75 ms	24.50	F831h
24.75 ms ≤ TONDLY < 25.25 ms	25.00	F832h
25.25 ms ≤ TONDLY < 25.75 ms	25.50	F833h
25.75 ms ≤ TONDLY < 26.25 ms	26.00	F834h
26.25 ms ≤ TONDLY < 26.75 ms	26.50	F835h
26.75 ms ≤ TONDLY < 27.25 ms	27.00	F836h
27.25 ms ≤ TONDLY < 27.75 ms	27.50	F837h
27.75 ms ≤ TONDLY < 28.25 ms	28.00	F838h

Table 1-79. Supported Value Mapping (continued)

TON_DELAY (decoded)	Turn-on Delay (ms)	Nominal SLINEAR11 (hex)
28.25 ms ≤ TONDLY < 28.75 ms	28.50	F839h
28.75 ms ≤ TONDLY < 29.25 ms	29.00	F83Ah
29.25 ms ≤ TONDLY < 29.75 ms	29.50	F83Bh
29.75 ms ≤ TONDLY < 30.25 ms	30.00	F83Ch
30.25 ms ≤ TONDLY < 30.75 ms	30.50	F83Dh
30.75 ms ≤ TONDLY < 31.25 ms	31.00	F83Eh
31.25 ms ≤ TONDLY < 31.75 ms	31.50	F83Fh
31.75 ms ≤ TONDLY < 32.25 ms	32.00	F840h
32.25 ms ≤ TONDLY < 32.75 ms	32.50	F841h
32.75 ms ≤ TONDLY < 33.25 ms	33.00	F842h
33.25 ms ≤ TONDLY < 33.75 ms	33.50	F843h
33.75 ms ≤ TONDLY < 34.25 ms	34.00	F844h
34.25 ms ≤ TONDLY < 34.75 ms	34.50	F845h
34.75 ms ≤ TONDLY < 35.25 ms	35.00	F846h
35.25 ms ≤ TONDLY < 35.75 ms	35.50	F847h
35.75 ms ≤ TONDLY < 36.25 ms	36.00	F848h
36.25 ms ≤ TONDLY < 36.75 ms	36.50	F849h
36.75 ms ≤ TONDLY < 37.25 ms	37.00	F84Ah
37.25 ms ≤ TONDLY < 37.75 ms	37.50	F84Bh
37.75 ms ≤ TONDLY < 38.25 ms	38.00	F84Ch
38.25 ms ≤ TONDLY < 38.75 ms	38.50	F84Dh
38.75 ms ≤ TONDLY < 39.25 ms	39.00	F84Eh
39.25 ms ≤ TONDLY < 39.75 ms	39.50	F84Fh
39.75 ms ≤ TONDLY < 40.25 ms	40.00	F850h
40.25 ms ≤ TONDLY < 40.75 ms	40.50	F851h
40.75 ms ≤ TONDLY < 41.25 ms	41.00	F852h
41.25 ms ≤ TONDLY < 41.75 ms	41.50	F853h
41.75 ms ≤ TONDLY < 42.25 ms	42.00	F854h
42.25 ms ≤ TONDLY < 42.75 ms	42.50	F855h
42.75 ms ≤ TONDLY < 43.25 ms	43.00	F856h
43.25 ms ≤ TONDLY < 43.75 ms	43.50	F857h
43.75 ms ≤ TONDLY < 44.25 ms	44.00	F858h
44.25 ms ≤ TONDLY < 44.75 ms	44.50	F859h
44.75 ms ≤ TONDLY < 45.25 ms	45.00	F85Ah
45.25 ms ≤ TONDLY < 45.75 ms	45.50	F85Bh
45.75 ms ≤ TONDLY < 46.25 ms	46.00	F85Ch
46.25 ms ≤ TONDLY < 46.75 ms	46.50	F85Dh
46.75 ms ≤ TONDLY < 47.25 ms	47.00	F85Eh
47.25 ms ≤ TONDLY < 47.75 ms	47.50	F85Fh
47.75 ms ≤ TONDLY < 48.25 ms	48.00	F860h
48.25 ms ≤ TONDLY < 48.75 ms	48.50	F861h
48.75 ms ≤ TONDLY < 49.25 ms	49.00	F862h
49.25 ms ≤ TONDLY < 49.75 ms	49.50	F863h
49.75 ms ≤ TONDLY < 50.25 ms	50.00	F864h
50.25 ms ≤ TONDLY < 50.75 ms	50.50	F865h

Table 1-79. Supported Value Mapping (continued)

TON_DELAY (decoded)	Turn-on Delay (ms)	Nominal SLINEAR11 (hex)
50.75 ms ≤ TONDLY < 51.25 ms	51.00	F866h
51.25 ms ≤ TONDLY < 51.75 ms	51.50	F867h
51.75 ms ≤ TONDLY < 52.25 ms	52.00	F868h
52.25 ms ≤ TONDLY < 52.75 ms	52.50	F869h
52.75 ms ≤ TONDLY < 53.25 ms	53.00	F86Ah
53.25 ms ≤ TONDLY < 53.75 ms	53.50	F86Bh
53.75 ms ≤ TONDLY < 54.25 ms	54.00	F86Ch
54.25 ms ≤ TONDLY < 54.75 ms	54.50	F86Dh
54.75 ms ≤ TONDLY < 55.25 ms	55.00	F86Eh
55.25 ms ≤ TONDLY < 55.75 ms	55.50	F86Fh
55.75 ms ≤ TONDLY < 56.25 ms	56.00	F870h
56.25 ms ≤ TONDLY < 56.75 ms	56.50	F871h
56.75 ms ≤ TONDLY < 57.25 ms	57.00	F872h
57.25 ms ≤ TONDLY < 57.75 ms	57.50	F873h
57.75 ms ≤ TONDLY < 58.25 ms	58.00	F874h
58.25 ms ≤ TONDLY < 58.75 ms	58.50	F875h
58.75 ms ≤ TONDLY < 59.25 ms	59.00	F876h
59.25 ms ≤ TONDLY < 59.75 ms	59.50	F877h
59.75 ms ≤ TONDLY < 60.25 ms	60.00	F878h
60.25 ms ≤ TONDLY < 60.75 ms	60.50	F879h
60.75 ms ≤ TONDLY < 61.25 ms	61.00	F87Ah
61.25 ms ≤ TONDLY < 61.75 ms	61.50	F87Bh
61.75 ms ≤ TONDLY < 62.25 ms	62.00	F87Ch
62.25 ms ≤ TONDLY < 62.75 ms	62.50	F87Dh
62.75 ms ≤ TONDLY < 63.25 ms	63.00	F87Eh
63.25 ms ≤ TONDLY < 63.75 ms	63.50	F87Fh
63.75 ms ≤ TONDLY < 64.25 ms	64.00	F880h
64.25 ms ≤ TONDLY < 64.75 ms	64.50	F881h
64.75 ms ≤ TONDLY < 65.25 ms	65.00	F882h
65.25 ms ≤ TONDLY < 65.75 ms	65.50	F883h
65.75 ms ≤ TONDLY < 66.25 ms	66.00	F884h
66.25 ms ≤ TONDLY < 66.75 ms	66.50	F885h
66.75 ms ≤ TONDLY < 67.25 ms	67.00	F886h
67.25 ms ≤ TONDLY < 67.75 ms	67.50	F887h
67.75 ms ≤ TONDLY < 68.25 ms	68.00	F888h
68.25 ms ≤ TONDLY < 68.75 ms	68.50	F889h
68.75 ms ≤ TONDLY < 69.25 ms	69.00	F88Ah
69.25 ms ≤ TONDLY < 69.75 ms	69.50	F88Bh
69.75 ms ≤ TONDLY < 70.25 ms	70.00	F88Ch
70.25 ms ≤ TONDLY < 70.75 ms	70.50	F88Dh
70.75 ms ≤ TONDLY < 71.25 ms	71.00	F88Eh
71.25 ms ≤ TONDLY < 71.75 ms	71.50	F88Fh
71.75 ms ≤ TONDLY < 72.25 ms	72.00	F890h
72.25 ms ≤ TONDLY < 72.75 ms	72.50	F891h
72.75 ms ≤ TONDLY < 73.25 ms	73.00	F892h

Table 1-79. Supported Value Mapping (continued)

TON_DELAY (decoded)	Turn-on Delay (ms)	Nominal SLINEAR11 (hex)
73.25 ms ≤ TONDLY < 73.75 ms	73.50	F893h
73.75 ms ≤ TONDLY < 74.25 ms	74.00	F894h
74.25 ms ≤ TONDLY < 74.75 ms	74.50	F895h
74.75 ms ≤ TONDLY < 75.25 ms	75.00	F896h
75.25 ms ≤ TONDLY < 75.75 ms	75.50	F897h
75.75 ms ≤ TONDLY < 76.25 ms	76.00	F898h
76.25 ms ≤ TONDLY < 76.75 ms	76.50	F899h
76.75 ms ≤ TONDLY < 77.25 ms	77.00	F89Ah
77.25 ms ≤ TONDLY < 77.75 ms	77.50	F89Bh
77.75 ms ≤ TONDLY < 78.25 ms	78.00	F89Ch
78.25 ms ≤ TONDLY < 78.75 ms	78.50	F89Dh
78.75 ms ≤ TONDLY < 79.25 ms	79.00	F89Eh
79.25 ms ≤ TONDLY < 79.75 ms	79.50	F89Fh
79.75 ms ≤ TONDLY < 80.25 ms	80.00	F8A0h
80.25 ms ≤ TONDLY < 80.75 ms	80.50	F8A1h
80.75 ms ≤ TONDLY < 81.25 ms	81.00	F8A2h
81.25 ms ≤ TONDLY < 81.75 ms	81.50	F8A3h
81.75 ms ≤ TONDLY < 82.25 ms	82.00	F8A4h
82.25 ms ≤ TONDLY < 82.75 ms	82.50	F8A5h
82.75 ms ≤ TONDLY < 83.25 ms	83.00	F8A6h
83.25 ms ≤ TONDLY < 83.75 ms	83.50	F8A7h
83.75 ms ≤ TONDLY < 84.25 ms	84.00	F8A8h
84.25 ms ≤ TONDLY < 84.75 ms	84.50	F8A9h
84.75 ms ≤ TONDLY < 85.25 ms	85.00	F8AAh
85.25 ms ≤ TONDLY < 85.75 ms	85.50	F8ABh
85.75 ms ≤ TONDLY < 86.25 ms	86.00	F8ACh
86.25 ms ≤ TONDLY < 86.75 ms	86.50	F8ADh
86.75 ms ≤ TONDLY < 87.25 ms	87.00	F8AEh
87.25 ms ≤ TONDLY < 87.75 ms	87.50	F8AFh
87.75 ms ≤ TONDLY < 88.25 ms	88.00	F8B0h
88.25 ms ≤ TONDLY < 88.75 ms	88.50	F8B1h
88.75 ms ≤ TONDLY < 89.25 ms	89.00	F8B2h
89.25 ms ≤ TONDLY < 89.75 ms	89.50	F8B3h
89.75 ms ≤ TONDLY < 90.25 ms	90.00	F8B4h
90.25 ms ≤ TONDLY < 90.75 ms	90.50	F8B5h
90.75 ms ≤ TONDLY < 91.25 ms	91.00	F8B6h
91.25 ms ≤ TONDLY < 91.75 ms	91.50	F8B7h
91.75 ms ≤ TONDLY < 92.25 ms	92.00	F8B8h
92.25 ms ≤ TONDLY < 92.75 ms	92.50	F8B9h
92.75 ms ≤ TONDLY < 93.25 ms	93.00	F8BAh
93.25 ms ≤ TONDLY < 93.75 ms	93.50	F8BBh
93.75 ms ≤ TONDLY < 94.25 ms	94.00	F8BCh
94.25 ms ≤ TONDLY < 94.75 ms	94.50	F8BDh
94.75 ms ≤ TONDLY < 95.25 ms	95.00	F8BEh
95.25 ms ≤ TONDLY < 95.75 ms	95.50	F8BFh

Table 1-79. Supported Value Mapping (continued)

TON_DELAY (decoded)	Turn-on Delay (ms)	Nominal SLINEAR11 (hex)
95.75 ms ≤ TONDLY < 96.25 ms	96.00	F8C0h
96.25 ms ≤ TONDLY < 96.75 ms	96.50	F8C1h
96.75 ms ≤ TONDLY < 97.25 ms	97.00	F8C2h
97.25 ms ≤ TONDLY < 97.75 ms	97.50	F8C3h
97.75 ms ≤ TONDLY < 98.25 ms	98.00	F8C4h
98.25 ms ≤ TONDLY < 98.75 ms	98.50	F8C5h
98.75 ms ≤ TONDLY < 99.25 ms	99.00	F8C6h
99.25 ms ≤ TONDLY < 99.75 ms	99.50	F8C7h
99.75 ms ≤ TONDLY < 100.25 ms	100.00	F8C8h
100.25 ms ≤ TONDLY < 100.75 ms	100.50	F8C9h
100.75 ms ≤ TONDLY < 101.25 ms	101.00	F8CAh
101.25 ms ≤ TONDLY < 101.75 ms	101.50	F8CBh
101.75 ms ≤ TONDLY < 102.25 ms	102.00	F8CCh
102.25 ms ≤ TONDLY < 102.75 ms	102.50	F8CDh
102.75 ms ≤ TONDLY < 103.25 ms	103.00	F8CEh
103.25 ms ≤ TONDLY < 103.75 ms	103.50	F8CFh
103.75 ms ≤ TONDLY < 104.25 ms	104.00	F8D0h
104.25 ms ≤ TONDLY < 104.75 ms	104.50	F8D1h
104.75 ms ≤ TONDLY < 105.25 ms	105.00	F8D2h
105.25 ms ≤ TONDLY < 105.75 ms	105.50	F8D3h
105.75 ms ≤ TONDLY < 106.25 ms	106.00	F8D4h
106.25 ms ≤ TONDLY < 106.75 ms	106.50	F8D5h
106.75 ms ≤ TONDLY < 107.25 ms	107.00	F8D6h
107.25 ms ≤ TONDLY < 107.75 ms	107.50	F8D7h
107.75 ms ≤ TONDLY < 108.25 ms	108.00	F8D8h
108.25 ms ≤ TONDLY < 108.75 ms	108.50	F8D9h
108.75 ms ≤ TONDLY < 109.25 ms	109.00	F8DAh
109.25 ms ≤ TONDLY < 109.75 ms	109.50	F8DBh
109.75 ms ≤ TONDLY < 110.25 ms	110.00	F8DCh
110.25 ms ≤ TONDLY < 110.75 ms	110.50	F8DDh
110.75 ms ≤ TONDLY < 111.25 ms	111.00	F8DEh
111.25 ms ≤ TONDLY < 111.75 ms	111.50	F8DFh
111.75 ms ≤ TONDLY < 112.25 ms	112.00	F8E0h
112.25 ms ≤ TONDLY < 112.75 ms	112.50	F8E1h
112.75 ms ≤ TONDLY < 113.25 ms	113.00	F8E2h
113.25 ms ≤ TONDLY < 113.75 ms	113.50	F8E3h
113.75 ms ≤ TONDLY < 114.25 ms	114.00	F8E4h
114.25 ms ≤ TONDLY < 114.75 ms	114.50	F8E5h
114.75 ms ≤ TONDLY < 115.25 ms	115.00	F8E6h
115.25 ms ≤ TONDLY < 115.75 ms	115.50	F8E7h
115.75 ms ≤ TONDLY < 116.25 ms	116.00	F8E8h
116.25 ms ≤ TONDLY < 116.75 ms	116.50	F8E9h
116.75 ms ≤ TONDLY < 117.25 ms	117.00	F8EAh
117.25 ms ≤ TONDLY < 117.75 ms	117.50	F8EBh
117.75 ms ≤ TONDLY < 118.25 ms	118.00	F8ECh

Table 1-79. Supported Value Mapping (continued)

TON_DELAY (decoded)	Turn-on Delay (ms)	Nominal SLINEAR11 (hex)
118.25 ms ≤ TONDLY < 118.75 ms	118.50	F8EDh
118.75 ms ≤ TONDLY < 119.25 ms	119.00	F8EEh
119.25 ms ≤ TONDLY < 119.75 ms	119.50	F8EFh
119.75 ms ≤ TONDLY < 120.25 ms	120.00	F8F0h
120.25 ms ≤ TONDLY < 120.75 ms	120.50	F8F1h
120.75 ms ≤ TONDLY < 121.25 ms	121.00	F8F2h
121.25 ms ≤ TONDLY < 121.75 ms	121.50	F8F3h
121.75 ms ≤ TONDLY < 122.25 ms	122.00	F8F4h
122.25 ms ≤ TONDLY < 122.75 ms	122.50	F8F5h
122.75 ms ≤ TONDLY < 123.25 ms	123.00	F8F6h
123.25 ms ≤ TONDLY < 123.75 ms	123.50	F8F7h
123.75 ms ≤ TONDLY < 124.25 ms	124.00	F8F8h
124.25 ms ≤ TONDLY < 124.75 ms	124.50	F8F9h
124.75 ms ≤ TONDLY < 125.25 ms	125.00	F8FAh
125.25 ms ≤ TONDLY < 125.75 ms	125.50	F8FBh
125.75 ms ≤ TONDLY < 126.25 ms	126.00	F8FCh
126.25 ms ≤ TONDLY < 126.75 ms	126.50	F8FDh
126.75 ms ≤ TONDLY < 127.25 ms	127.00	F8FEh
127.25 ms ≤ TONDLY ≤ 127.5 ms	127.50	F8FFh
TON_DELAY > 127.5 ms	Invalid/Unsupported	Invalid/Unsupported

1.2.59 (61h) TON_RISE

CMD Address	61h
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	SLINEAR11
Paged:	Yes
Phased:	No
NVM Back-up:	EEPROM
Updates:	On-the-fly

The TON_RISE command sets the time, in milliseconds, from when the output starts to rise until the voltage has entered the regulation band. This effectively sets the slew rate of the reference DAC during the soft-start period. Note that the rise time is equal to TON_RISE regardless of the value of the target output voltage or VOUT_SCALE_LOOP . For the purposes of slew rate selection based on the target output voltage, the TPS536xx assumes a zero-loadline configuration.

Note

NOTE: The rise time during power-up will not match the value programmed into TON_RISE . Instead, the TPS536xx will calculate the desired slew rate as SR_{BOOT} = VBOOT/TON_RISE, and select the nearest supported transition rate, as described in the product datasheet.

(61h) TON_RISE Register Map

15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
TONR EXP					TONR MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
TONR MAN							

LEGEND: R/W = Read/Write; R = Read only

Table 1-80. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:11	TONR EXP	RW	11110b	Linear format two's complement exponent.
10:0	TONR MAN	RW	NVM	Linear format two's complement mantissa.

Attempts to write (61h) TON_RISE will be considered invalid/unsupported command and cause TPS536xx to respond by flagging the appropriate status bits, and notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

Table 1-81. Supported Value Mapping

TON_RISE (decoded)	Turn-on Rise Time (ms)	Nominal SLINEAR11 (hex)
TON_RISE = 0 ms	0.25	F000h
0 ms < TON_RISE < 0.375 ms	0.25	F001h
0.375 ms ≤ TON_RISE < 0.625 ms	0.50	F002h
0.625 ms ≤ TON_RISE < 0.875 ms	0.75	F003h
0.875 ms ≤ TON_RISE < 1.125 ms	1.00	F004h
1.125 ms ≤ TON_RISE < 1.375 ms	1.25	F005h
1.375 ms ≤ TON_RISE < 1.625 ms	1.50	F006h
1.625 ms ≤ TON_RISE < 1.875 ms	1.75	F007h
1.875 ms ≤ TON_RISE < 2.125 ms	2.00	F008h

Table 1-81. Supported Value Mapping (continued)

TON_RISE (decoded)	Turn-on Rise Time (ms)	Nominal SLINEAR11 (hex)
2.125 ms ≤ TON_RISE < 2.375 ms	2.25	F009h
2.375 ms ≤ TON_RISE < 2.625 ms	2.50	F00Ah
2.625 ms ≤ TON_RISE < 2.875 ms	2.75	F00Bh
2.875 ms ≤ TON_RISE < 3.125 ms	3.00	F00Ch
3.125 ms ≤ TON_RISE < 3.375 ms	3.25	F00Dh
3.375 ms ≤ TON_RISE < 3.625 ms	3.50	F00Eh
3.625 ms ≤ TON_RISE < 3.875 ms	3.75	F00Fh
3.875 ms ≤ TON_RISE < 4.125 ms	4.00	F010h
4.125 ms ≤ TON_RISE < 4.375 ms	4.25	F011h
4.375 ms ≤ TON_RISE < 4.625 ms	4.50	F012h
4.625 ms ≤ TON_RISE < 4.875 ms	4.75	F013h
4.875 ms ≤ TON_RISE < 5.125 ms	5.00	F014h
5.125 ms ≤ TON_RISE < 5.375 ms	5.25	F015h
5.375 ms ≤ TON_RISE < 5.625 ms	5.50	F016h
5.625 ms ≤ TON_RISE < 5.875 ms	5.75	F017h
5.875 ms ≤ TON_RISE < 6.125 ms	6.00	F018h
6.125 ms ≤ TON_RISE < 6.375 ms	6.25	F019h
6.375 ms ≤ TON_RISE < 6.625 ms	6.50	F01Ah
6.625 ms ≤ TON_RISE < 6.875 ms	6.75	F01Bh
6.875 ms ≤ TON_RISE < 7.125 ms	7.00	F01Ch
7.125 ms ≤ TON_RISE < 7.375 ms	7.25	F01Dh
7.375 ms ≤ TON_RISE < 7.625 ms	7.50	F01Eh
7.625 ms ≤ TON_RISE < 7.875 ms	7.75	F01Fh
7.875 ms ≤ TON_RISE < 8.125 ms	8.00	F020h
8.125 ms ≤ TON_RISE < 8.375 ms	8.25	F021h
8.375 ms ≤ TON_RISE < 8.625 ms	8.50	F022h
8.625 ms ≤ TON_RISE < 8.875 ms	8.75	F023h
8.875 ms ≤ TON_RISE < 9.125 ms	9.00	F024h
9.125 ms ≤ TON_RISE < 9.375 ms	9.25	F025h
9.375 ms ≤ TON_RISE < 9.625 ms	9.50	F026h
9.625 ms ≤ TON_RISE < 9.875 ms	9.75	F027h
9.875 ms ≤ TON_RISE < 10.125 ms	10.00	F028h
10.125 ms ≤ TON_RISE < 10.375 ms	10.25	F029h
10.375 ms ≤ TON_RISE < 10.625 ms	10.50	F02Ah
10.625 ms ≤ TON_RISE < 10.875 ms	10.75	F02Bh
10.875 ms ≤ TON_RISE < 11.125 ms	11.00	F02Ch
11.125 ms ≤ TON_RISE < 11.375 ms	11.25	F02Dh
11.375 ms ≤ TON_RISE < 11.625 ms	11.50	F02Eh
11.625 ms ≤ TON_RISE < 11.875 ms	11.75	F02Fh
11.875 ms ≤ TON_RISE < 12.125 ms	12.00	F030h
12.125 ms ≤ TON_RISE < 12.375 ms	12.25	F031h
12.375 ms ≤ TON_RISE < 12.625 ms	12.50	F032h
12.625 ms ≤ TON_RISE < 12.875 ms	12.75	F033h
12.875 ms ≤ TON_RISE < 13.125 ms	13.00	F034h
13.125 ms ≤ TON_RISE < 13.375 ms	13.25	F035h

Table 1-81. Supported Value Mapping (continued)

TON_RISE (decoded)	Turn-on Rise Time (ms)	Nominal SLINEAR11 (hex)
13.375 ms ≤ TON_RISE < 13.625 ms	13.50	F036h
13.625 ms ≤ TON_RISE < 13.875 ms	13.75	F037h
13.875 ms ≤ TON_RISE < 14.125 ms	14.00	F038h
14.125 ms ≤ TON_RISE < 14.375 ms	14.25	F039h
14.375 ms ≤ TON_RISE < 14.625 ms	14.50	F03Ah
14.625 ms ≤ TON_RISE < 14.875 ms	14.75	F03Bh
14.875 ms ≤ TON_RISE < 15.125 ms	15.00	F03Ch
15.125 ms ≤ TON_RISE < 15.375 ms	15.25	F03Dh
15.375 ms ≤ TON_RISE < 15.625 ms	15.50	F03Eh
15.625 ms ≤ TON_RISE < 15.875 ms	15.75	F03Fh
15.875 ms ≤ TON_RISE < 16.125 ms	16.00	F040h
16.125 ms ≤ TON_RISE < 16.375 ms	16.25	F041h
16.375 ms ≤ TON_RISE < 16.625 ms	16.50	F042h
16.625 ms ≤ TON_RISE < 16.875 ms	16.75	F043h
16.875 ms ≤ TON_RISE < 17.125 ms	17.00	F044h
17.125 ms ≤ TON_RISE < 17.375 ms	17.25	F045h
17.375 ms ≤ TON_RISE < 17.625 ms	17.50	F046h
17.625 ms ≤ TON_RISE < 17.875 ms	17.75	F047h
17.875 ms ≤ TON_RISE < 18.125 ms	18.00	F048h
18.125 ms ≤ TON_RISE < 18.375 ms	18.25	F049h
18.375 ms ≤ TON_RISE < 18.625 ms	18.50	F04Ah
18.625 ms ≤ TON_RISE < 18.875 ms	18.75	F04Bh
18.875 ms ≤ TON_RISE < 19.125 ms	19.00	F04Ch
19.125 ms ≤ TON_RISE < 19.375 ms	19.25	F04Dh
19.375 ms ≤ TON_RISE < 19.625 ms	19.50	F04Eh
19.625 ms ≤ TON_RISE < 19.875 ms	19.75	F04Fh
19.875 ms ≤ TON_RISE < 20.125 ms	20.00	F050h
20.125 ms ≤ TON_RISE < 20.375 ms	20.25	F051h
20.375 ms ≤ TON_RISE < 20.625 ms	20.50	F052h
20.625 ms ≤ TON_RISE < 20.875 ms	20.75	F053h
20.875 ms ≤ TON_RISE < 21.125 ms	21.00	F054h
21.125 ms ≤ TON_RISE < 21.375 ms	21.25	F055h
21.375 ms ≤ TON_RISE < 21.625 ms	21.50	F056h
21.625 ms ≤ TON_RISE < 21.875 ms	21.75	F057h
21.875 ms ≤ TON_RISE < 22.125 ms	22.00	F058h
22.125 ms ≤ TON_RISE < 22.375 ms	22.25	F059h
22.375 ms ≤ TON_RISE < 22.625 ms	22.50	F05Ah
22.625 ms ≤ TON_RISE < 22.875 ms	22.75	F05Bh
22.875 ms ≤ TON_RISE < 23.125 ms	23.00	F05Ch
23.125 ms ≤ TON_RISE < 23.375 ms	23.25	F05Dh
23.375 ms ≤ TON_RISE < 23.625 ms	23.50	F05Eh
23.625 ms ≤ TON_RISE < 23.875 ms	23.75	F05Fh
23.875 ms ≤ TON_RISE < 24.125 ms	24.00	F060h
24.125 ms ≤ TON_RISE < 24.375 ms	24.25	F061h
24.375 ms ≤ TON_RISE < 24.625 ms	24.50	F062h

Table 1-81. Supported Value Mapping (continued)

TON_RISE (decoded)	Turn-on Rise Time (ms)	Nominal SLINEAR11 (hex)
24.625 ms ≤ TON_RISE < 24.875 ms	24.75	F063h
24.875 ms ≤ TON_RISE < 25.125 ms	25.00	F064h
25.125 ms ≤ TON_RISE < 25.375 ms	25.25	F065h
25.375 ms ≤ TON_RISE < 25.625 ms	25.50	F066h
25.625 ms ≤ TON_RISE < 25.875 ms	25.75	F067h
25.875 ms ≤ TON_RISE < 26.125 ms	26.00	F068h
26.125 ms ≤ TON_RISE < 26.375 ms	26.25	F069h
26.375 ms ≤ TON_RISE < 26.625 ms	26.50	F06Ah
26.625 ms ≤ TON_RISE < 26.875 ms	26.75	F06Bh
26.875 ms ≤ TON_RISE < 27.125 ms	27.00	F06Ch
27.125 ms ≤ TON_RISE < 27.375 ms	27.25	F06Dh
27.375 ms ≤ TON_RISE < 27.625 ms	27.50	F06Eh
27.625 ms ≤ TON_RISE < 27.875 ms	27.75	F06Fh
27.875 ms ≤ TON_RISE < 28.125 ms	28.00	F070h
28.125 ms ≤ TON_RISE < 28.375 ms	28.25	F071h
28.375 ms ≤ TON_RISE < 28.625 ms	28.50	F072h
28.625 ms ≤ TON_RISE < 28.875 ms	28.75	F073h
28.875 ms ≤ TON_RISE < 29.125 ms	29.00	F074h
29.125 ms ≤ TON_RISE < 29.375 ms	29.25	F075h
29.375 ms ≤ TON_RISE < 29.625 ms	29.50	F076h
29.625 ms ≤ TON_RISE < 29.875 ms	29.75	F077h
29.875 ms ≤ TON_RISE < 30.125 ms	30.00	F078h
30.125 ms ≤ TON_RISE < 30.375 ms	30.25	F079h
30.375 ms ≤ TON_RISE < 30.625 ms	30.50	F07Ah
30.625 ms ≤ TON_RISE < 30.875 ms	30.75	F07Bh
30.875 ms ≤ TON_RISE < 31.125 ms	31.00	F07Ch
31.125 ms ≤ TON_RISE < 31.375 ms	31.25	F07Dh
31.375 ms ≤ TON_RISE < 31.625 ms	31.50	F07Eh
31.625 ms ≤ TON_RISE ≤ 31.75 ms	31.75	F07Fh
TON_RISE > 31.75 ms	Invalid/Unsupported	Invalid/Unsupported

1.2.60 (62h) TON_MAX_FAULT_LIMIT

CMD Address	62h
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	SLINEAR11
Paged:	Yes
Phased:	No
NVM Back-up:	EEPROM
Updates:	On-the-fly

The TON_MAX_FAULT_LIMIT command sets an upper limit, in milliseconds, on how long the unit can attempt to power up the output without reaching the target voltage.

The TON_MAX time is defined as the maximum allowable amount of time from the end of TON_DELAY , until the output voltage reaches the V_{TONMAX} threshold, as calculated below:

V_{TONMAX} = VOUT_UV_FAULT_LIMIT – (IOUT_OC_FAULT_LIMIT × VOUT_DROOP)

That is, if the sensed output voltage is not greater than the tracking VOUT_UV_FAULT_LIMIT based on the the DAC setting, by the time the TON_MAX time has expired, the TON_MAX fault is declared.

Note that for TPS536xx, the undervoltage fault limit is enabled at the beginning of switching (tracking the current output target minius offset). As a consequence, unless VOUT_UV_FAULT_RESPONSE is set to ignore, in the case of a “real” TON_MAX fault (e.g. output voltage did not rise quickly enough), UV faults / associated response will always precede TON_MAX.

The converter response to a TON_MAX fault event is described in TON_MAX_FAULT_RESPONSE .

(62h) TON_MAX_FAULT_LIMIT Register Map

15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
TONMAXF EXP					TONMAXF MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
TONMAXF MAN							

LEGEND: R/W = Read/Write; R = Read only

Table 1-82. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:11	TONMAXF EXP	RW	11110b	Linear format two’s complement exponent.
10:0	TONMAXF MAN	RW	NVM	Linear format two’s complement mantissa.

Attempts to write (62h) TON_MAX_FAULT_LIMIT will be considered invalid/unsupported command and cause TPS536xx to respond by flagging the appropriate status bits, and notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

Table 1-83. Supported Value Mapping

TON_MAX_FAULT_LIMIT (decoded)	TON_MAX Limit (ms)	Nominal SLINEAR11 (hex)
TONMAXF = 0 ms	TON_MAX Disabled	F000h
TONMAXF < TON_RISE	TON_MAX Disabled*	Invalid/Unsupported
0 ms < TON_MAX < 0.375 ms	0.25	F001h

Table 1-83. Supported Value Mapping (continued)

TON_MAX_FAULT_LIMIT (decoded)	TON_MAX Limit (ms)	Nominal SLINEAR11 (hex)
0.375 ms ≤ TONMAXF < 0.625 ms	0.50	F002h
0.625 ms ≤ TONMAXF < 0.875 ms	0.75	F003h
0.875 ms ≤ TONMAXF < 1.125 ms	1.00	F004h
1.125 ms ≤ TONMAXF < 1.375 ms	1.25	F005h
1.375 ms ≤ TONMAXF < 1.625 ms	1.50	F006h
1.625 ms ≤ TONMAXF < 1.875 ms	1.75	F007h
1.875 ms ≤ TONMAXF < 2.125 ms	2.00	F008h
2.125 ms ≤ TONMAXF < 2.375 ms	2.25	F009h
2.375 ms ≤ TONMAXF < 2.625 ms	2.50	F00Ah
2.625 ms ≤ TONMAXF < 2.875 ms	2.75	F00Bh
2.875 ms ≤ TONMAXF < 3.125 ms	3.00	F00Ch
3.125 ms ≤ TONMAXF < 3.375 ms	3.25	F00Dh
3.375 ms ≤ TONMAXF < 3.625 ms	3.50	F00Eh
3.625 ms ≤ TONMAXF < 3.875 ms	3.75	F00Fh
3.875 ms ≤ TONMAXF < 4.125 ms	4.00	F010h
4.125 ms ≤ TONMAXF < 4.375 ms	4.25	F011h
4.375 ms ≤ TONMAXF < 4.625 ms	4.50	F012h
4.625 ms ≤ TONMAXF < 4.875 ms	4.75	F013h
4.875 ms ≤ TONMAXF < 5.125 ms	5.00	F014h
5.125 ms ≤ TONMAXF < 5.375 ms	5.25	F015h
5.375 ms ≤ TONMAXF < 5.625 ms	5.50	F016h
5.625 ms ≤ TONMAXF < 5.875 ms	5.75	F017h
5.875 ms ≤ TONMAXF < 6.125 ms	6.00	F018h
6.125 ms ≤ TONMAXF < 6.375 ms	6.25	F019h
6.375 ms ≤ TONMAXF < 6.625 ms	6.50	F01Ah
6.625 ms ≤ TONMAXF < 6.875 ms	6.75	F01Bh
6.875 ms ≤ TONMAXF < 7.125 ms	7.00	F01Ch
7.125 ms ≤ TONMAXF < 7.375 ms	7.25	F01Dh
7.375 ms ≤ TONMAXF < 7.625 ms	7.50	F01Eh
7.625 ms ≤ TONMAXF < 7.875 ms	7.75	F01Fh
7.875 ms ≤ TONMAXF < 8.125 ms	8.00	F020h
8.125 ms ≤ TONMAXF < 8.375 ms	8.25	F021h
8.375 ms ≤ TONMAXF < 8.625 ms	8.50	F022h
8.625 ms ≤ TONMAXF < 8.875 ms	8.75	F023h
8.875 ms ≤ TONMAXF < 9.125 ms	9.00	F024h
9.125 ms ≤ TONMAXF < 9.375 ms	9.25	F025h
9.375 ms ≤ TONMAXF < 9.625 ms	9.50	F026h
9.625 ms ≤ TONMAXF < 9.875 ms	9.75	F027h
9.875 ms ≤ TONMAXF < 10.125 ms	10.00	F028h
10.125 ms ≤ TONMAXF < 10.375 ms	10.25	F029h
10.375 ms ≤ TONMAXF < 10.625 ms	10.50	F02Ah
10.625 ms ≤ TONMAXF < 10.875 ms	10.75	F02Bh
10.875 ms ≤ TONMAXF < 11.125 ms	11.00	F02Ch
11.125 ms ≤ TONMAXF < 11.375 ms	11.25	F02Dh
11.375 ms ≤ TONMAXF < 11.625 ms	11.50	F02Eh

Table 1-83. Supported Value Mapping (continued)

TON_MAX_FAULT_LIMIT (decoded)	TON_MAX Limit (ms)	Nominal SLINEAR11 (hex)
11.625 ms ≤ TONMAXF < 11.875 ms	11.75	F02Fh
11.875 ms ≤ TONMAXF < 12.125 ms	12.00	F030h
12.125 ms ≤ TONMAXF < 12.375 ms	12.25	F031h
12.375 ms ≤ TONMAXF < 12.625 ms	12.50	F032h
12.625 ms ≤ TONMAXF < 12.875 ms	12.75	F033h
12.875 ms ≤ TONMAXF < 13.125 ms	13.00	F034h
13.125 ms ≤ TONMAXF < 13.375 ms	13.25	F035h
13.375 ms ≤ TONMAXF < 13.625 ms	13.50	F036h
13.625 ms ≤ TONMAXF < 13.875 ms	13.75	F037h
13.875 ms ≤ TONMAXF < 14.125 ms	14.00	F038h
14.125 ms ≤ TONMAXF < 14.375 ms	14.25	F039h
14.375 ms ≤ TONMAXF < 14.625 ms	14.50	F03Ah
14.625 ms ≤ TONMAXF < 14.875 ms	14.75	F03Bh
14.875 ms ≤ TONMAXF < 15.125 ms	15.00	F03Ch
15.125 ms ≤ TONMAXF < 15.375 ms	15.25	F03Dh
15.375 ms ≤ TONMAXF < 15.625 ms	15.50	F03Eh
15.625 ms ≤ TONMAXF < 15.875 ms	15.75	F03Fh
15.875 ms ≤ TONMAXF < 16.125 ms	16.00	F040h
16.125 ms ≤ TONMAXF < 16.375 ms	16.25	F041h
16.375 ms ≤ TONMAXF < 16.625 ms	16.50	F042h
16.625 ms ≤ TONMAXF < 16.875 ms	16.75	F043h
16.875 ms ≤ TONMAXF < 17.125 ms	17.00	F044h
17.125 ms ≤ TONMAXF < 17.375 ms	17.25	F045h
17.375 ms ≤ TONMAXF < 17.625 ms	17.50	F046h
17.625 ms ≤ TONMAXF < 17.875 ms	17.75	F047h
17.875 ms ≤ TONMAXF < 18.125 ms	18.00	F048h
18.125 ms ≤ TONMAXF < 18.375 ms	18.25	F049h
18.375 ms ≤ TONMAXF < 18.625 ms	18.50	F04Ah
18.625 ms ≤ TONMAXF < 18.875 ms	18.75	F04Bh
18.875 ms ≤ TONMAXF < 19.125 ms	19.00	F04Ch
19.125 ms ≤ TONMAXF < 19.375 ms	19.25	F04Dh
19.375 ms ≤ TONMAXF < 19.625 ms	19.50	F04Eh
19.625 ms ≤ TONMAXF < 19.875 ms	19.75	F04Fh
19.875 ms ≤ TONMAXF < 20.125 ms	20.00	F050h
20.125 ms ≤ TONMAXF < 20.375 ms	20.25	F051h
20.375 ms ≤ TONMAXF < 20.625 ms	20.50	F052h
20.625 ms ≤ TONMAXF < 20.875 ms	20.75	F053h
20.875 ms ≤ TONMAXF < 21.125 ms	21.00	F054h
21.125 ms ≤ TONMAXF < 21.375 ms	21.25	F055h
21.375 ms ≤ TONMAXF < 21.625 ms	21.50	F056h
21.625 ms ≤ TONMAXF < 21.875 ms	21.75	F057h
21.875 ms ≤ TONMAXF < 22.125 ms	22.00	F058h
22.125 ms ≤ TONMAXF < 22.375 ms	22.25	F059h
22.375 ms ≤ TONMAXF < 22.625 ms	22.50	F05Ah
22.625 ms ≤ TONMAXF < 22.875 ms	22.75	F05Bh

Table 1-83. Supported Value Mapping (continued)

TON_MAX_FAULT_LIMIT (decoded)	TON_MAX Limit (ms)	Nominal SLINEAR11 (hex)
22.875 ms ≤ TONMAXF < 23.125 ms	23.00	F05Ch
23.125 ms ≤ TONMAXF < 23.375 ms	23.25	F05Dh
23.375 ms ≤ TONMAXF < 23.625 ms	23.50	F05Eh
23.625 ms ≤ TONMAXF < 23.875 ms	23.75	F05Fh
23.875 ms ≤ TONMAXF < 24.125 ms	24.00	F060h
24.125 ms ≤ TONMAXF < 24.375 ms	24.25	F061h
24.375 ms ≤ TONMAXF < 24.625 ms	24.50	F062h
24.625 ms ≤ TONMAXF < 24.875 ms	24.75	F063h
24.875 ms ≤ TONMAXF < 25.125 ms	25.00	F064h
25.125 ms ≤ TONMAXF < 25.375 ms	25.25	F065h
25.375 ms ≤ TONMAXF < 25.625 ms	25.50	F066h
25.625 ms ≤ TONMAXF < 25.875 ms	25.75	F067h
25.875 ms ≤ TONMAXF < 26.125 ms	26.00	F068h
26.125 ms ≤ TONMAXF < 26.375 ms	26.25	F069h
26.375 ms ≤ TONMAXF < 26.625 ms	26.50	F06Ah
26.625 ms ≤ TONMAXF < 26.875 ms	26.75	F06Bh
26.875 ms ≤ TONMAXF < 27.125 ms	27.00	F06Ch
27.125 ms ≤ TONMAXF < 27.375 ms	27.25	F06Dh
27.375 ms ≤ TONMAXF < 27.625 ms	27.50	F06Eh
27.625 ms ≤ TONMAXF < 27.875 ms	27.75	F06Fh
27.875 ms ≤ TONMAXF < 28.125 ms	28.00	F070h
28.125 ms ≤ TONMAXF < 28.375 ms	28.25	F071h
28.375 ms ≤ TONMAXF < 28.625 ms	28.50	F072h
28.625 ms ≤ TONMAXF < 28.875 ms	28.75	F073h
28.875 ms ≤ TONMAXF < 29.125 ms	29.00	F074h
29.125 ms ≤ TONMAXF < 29.375 ms	29.25	F075h
29.375 ms ≤ TONMAXF < 29.625 ms	29.50	F076h
29.625 ms ≤ TONMAXF < 29.875 ms	29.75	F077h
29.875 ms ≤ TONMAXF < 30.125 ms	30.00	F078h
30.125 ms ≤ TONMAXF < 30.375 ms	30.25	F079h
30.375 ms ≤ TONMAXF < 30.625 ms	30.50	F07Ah
30.625 ms ≤ TONMAXF < 30.875 ms	30.75	F07Bh
30.875 ms ≤ TONMAXF < 31.125 ms	31.00	F07Ch
31.125 ms ≤ TONMAXF < 31.375 ms	31.25	F07Dh
31.375 ms ≤ TONMAXF < 31.625 ms	31.50	F07Eh
31.625 ms ≤ TONMAXF ≤ 31.75 ms	31.75	F07Fh
TONMAXF > 31.75 ms	Invalid/Unsupported	Invalid/Unsupported

*Note: programming TON_MAX_FAULT less than TON_RISE disables the TON_MAX functionality. Programming TON_RISE less than the current TON_MAX re-enables this functionality.

1.2.61 (63h) TON_MAX_FAULT_RESPONSE

CMD Address	63h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
Paged:	Yes
Phased:	No
NVM Back-up:	EEPROM
Updates:	On-the-fly. Do not change during a fault shutdown event.

The TON_MAX_FAULT_RESPONSE instructs the device on what action to take in response to TON_MAX fault. Upon triggering the input TON MAX fault, the converter responds per the byte below and the following actions are taken:

- Set the NONE OF THE ABOVE bit in the STATUS_BYTE
- Set the VOUT bit in the STATUS_WORD
- Set the TON_MAX bit in STATUS_VOUT
- Notify the host per PMBus 1.3.1 Part II specification, section 10.2

(63h) TON_MAX_FAULT_RESPONSE Register Map

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	R	R	R
TONMAX RESP					0	0	0

LEGEND: R/W = Read/Write; R = Read only

Table 1-84. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:3	TONMAX RESP	RW	NVM	TON MAX Fault Response. 00000b: Ignore. Continue operating without interruption. 10000b: Latch-off immediately. Shutdown and do not restart. Restart/clearing behavior is specified in the PMBus Specification v1.3, part II, section 10.7. 10111b: Hiccup immediately. Shutdown, wait 1 HICCUP period and attempt to restart and repeat, until either the unit is commanded OFF, or a successful retrial. Other: Invalid/Unsupported

Attempts to write (63h) TON_MAX_FAULT_RESPONSE to any value outside those specified as valid, will be considered invalid/unsupported data and cause TPS536xx to respond by flagging the appropriate status bits, and notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

1.2.62 (64h) TOFF_DELAY

CMD Address	64h
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	SLINEAR11
Paged:	Yes
Phased:	No
NVM Back-up:	EEPROM
Updates:	On-the-fly

The TOFF_DELAY command sets the time, in milliseconds, from when a stop condition is received (as programmed by the ON_OFF_CONFIG command) until the unit stops transferring energy to the output.

(64h) TOFF_DELAY Register Map

15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
TOFF DLY EXP					TOFF DLY MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
TOFF DLY MAN							

LEGEND: R/W = Read/Write; R = Read only

Table 1-85. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:11	TOFF DLY EXP	RW	11111b	Linear format two's complement exponent.
10:0	TOFF DLY MAN	RW	NVM	Linear format two's complement mantissa.

Attempts to write (64h) TOFF_DELAY will be considered invalid/unsupported command and cause TPS536xx to respond by flagging the appropriate status bits, and notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

Table 1-86. Supported Value Mapping

TOFF_DELAY (decoded)	Turn-off Delay (ms)	Nominal SLINEAR11 (hex)
TOFF_DELAY = 0 ms	As quickly as possible (< 0.1 ms)	F800h
0 ms < TOFF_DELAY < 0.75 ms	0.50	F801h
0.75 ms ≤ TOFF_DELAY < 1.25 ms	1.00	F802h
1.25 ms ≤ TOFF_DELAY < 1.75 ms	1.50	F803h
1.75 ms ≤ TOFF_DELAY < 2.25 ms	2.00	F804h
2.25 ms ≤ TOFF_DELAY < 2.75 ms	2.50	F805h
2.75 ms ≤ TOFF_DELAY < 3.25 ms	3.00	F806h
3.25 ms ≤ TOFF_DELAY < 3.75 ms	3.50	F807h
3.75 ms ≤ TOFF_DELAY < 4.25 ms	4.00	F808h
4.25 ms ≤ TOFF_DELAY < 4.75 ms	4.50	F809h
4.75 ms ≤ TOFF_DELAY < 5.25 ms	5.00	F80Ah
5.25 ms ≤ TOFF_DELAY < 5.75 ms	5.50	F80Bh
5.75 ms ≤ TOFF_DELAY < 6.25 ms	6.00	F80Ch
6.25 ms ≤ TOFF_DELAY < 6.75 ms	6.50	F80Dh

Table 1-86. Supported Value Mapping (continued)

TOFF_DELAY (decoded)	Turn-off Delay (ms)	Nominal SLINEAR11 (hex)
6.75 ms ≤ TOFF_DELAY < 7.25 ms	7.00	F80Eh
7.25 ms ≤ TOFF_DELAY < 7.75 ms	7.50	F80Fh
7.75 ms ≤ TOFF_DELAY < 8.25 ms	8.00	F810h
8.25 ms ≤ TOFF_DELAY < 8.75 ms	8.50	F811h
8.75 ms ≤ TOFF_DELAY < 9.25 ms	9.00	F812h
9.25 ms ≤ TOFF_DELAY < 9.75 ms	9.50	F813h
9.75 ms ≤ TOFF_DELAY < 10.25 ms	10.00	F814h
10.25 ms ≤ TOFF_DELAY < 10.75 ms	10.50	F815h
10.75 ms ≤ TOFF_DELAY < 11.25 ms	11.00	F816h
11.25 ms ≤ TOFF_DELAY < 11.75 ms	11.50	F817h
11.75 ms ≤ TOFF_DELAY < 12.25 ms	12.00	F818h
12.25 ms ≤ TOFF_DELAY < 12.75 ms	12.50	F819h
12.75 ms ≤ TOFF_DELAY < 13.25 ms	13.00	F81Ah
13.25 ms ≤ TOFF_DELAY < 13.75 ms	13.50	F81Bh
13.75 ms ≤ TOFF_DELAY < 14.25 ms	14.00	F81Ch
14.25 ms ≤ TOFF_DELAY < 14.75 ms	14.50	F81Dh
14.75 ms ≤ TOFF_DELAY < 15.25 ms	15.00	F81Eh
15.25 ms ≤ TOFF_DELAY < 15.75 ms	15.50	F81Fh
15.75 ms ≤ TOFF_DELAY < 16.25 ms	16.00	F820h
16.25 ms ≤ TOFF_DELAY < 16.75 ms	16.50	F821h
16.75 ms ≤ TOFF_DELAY < 17.25 ms	17.00	F822h
17.25 ms ≤ TOFF_DELAY < 17.75 ms	17.50	F823h
17.75 ms ≤ TOFF_DELAY < 18.25 ms	18.00	F824h
18.25 ms ≤ TOFF_DELAY < 18.75 ms	18.50	F825h
18.75 ms ≤ TOFF_DELAY < 19.25 ms	19.00	F826h
19.25 ms ≤ TOFF_DELAY < 19.75 ms	19.50	F827h
19.75 ms ≤ TOFF_DELAY < 20.25 ms	20.00	F828h
20.25 ms ≤ TOFF_DELAY < 20.75 ms	20.50	F829h
20.75 ms ≤ TOFF_DELAY < 21.25 ms	21.00	F82Ah
21.25 ms ≤ TOFF_DELAY < 21.75 ms	21.50	F82Bh
21.75 ms ≤ TOFF_DELAY < 22.25 ms	22.00	F82Ch
22.25 ms ≤ TOFF_DELAY < 22.75 ms	22.50	F82Dh
22.75 ms ≤ TOFF_DELAY < 23.25 ms	23.00	F82Eh
23.25 ms ≤ TOFF_DELAY < 23.75 ms	23.50	F82Fh
23.75 ms ≤ TOFF_DELAY < 24.25 ms	24.00	F830h
24.25 ms ≤ TOFF_DELAY < 24.75 ms	24.50	F831h
24.75 ms ≤ TOFF_DELAY < 25.25 ms	25.00	F832h
25.25 ms ≤ TOFF_DELAY < 25.75 ms	25.50	F833h
25.75 ms ≤ TOFF_DELAY < 26.25 ms	26.00	F834h
26.25 ms ≤ TOFF_DELAY < 26.75 ms	26.50	F835h
26.75 ms ≤ TOFF_DELAY < 27.25 ms	27.00	F836h
27.25 ms ≤ TOFF_DELAY < 27.75 ms	27.50	F837h
27.75 ms ≤ TOFF_DELAY < 28.25 ms	28.00	F838h
28.25 ms ≤ TOFF_DELAY < 28.75 ms	28.50	F839h
28.75 ms ≤ TOFF_DELAY < 29.25 ms	29.00	F83Ah

Table 1-86. Supported Value Mapping (continued)

TOFF_DELAY (decoded)	Turn-off Delay (ms)	Nominal SLINEAR11 (hex)
29.25 ms ≤ TOFF_DELAY < 29.75 ms	29.50	F83Bh
29.75 ms ≤ TOFF_DELAY < 30.25 ms	30.00	F83Ch
30.25 ms ≤ TOFF_DELAY < 30.75 ms	30.50	F83Dh
30.75 ms ≤ TOFF_DELAY < 31.25 ms	31.00	F83Eh
31.25 ms ≤ TOFF_DELAY < 31.75 ms	31.50	F83Fh
31.75 ms ≤ TOFF_DELAY < 32.25 ms	32.00	F840h
32.25 ms ≤ TOFF_DELAY < 32.75 ms	32.50	F841h
32.75 ms ≤ TOFF_DELAY < 33.25 ms	33.00	F842h
33.25 ms ≤ TOFF_DELAY < 33.75 ms	33.50	F843h
33.75 ms ≤ TOFF_DELAY < 34.25 ms	34.00	F844h
34.25 ms ≤ TOFF_DELAY < 34.75 ms	34.50	F845h
34.75 ms ≤ TOFF_DELAY < 35.25 ms	35.00	F846h
35.25 ms ≤ TOFF_DELAY < 35.75 ms	35.50	F847h
35.75 ms ≤ TOFF_DELAY < 36.25 ms	36.00	F848h
36.25 ms ≤ TOFF_DELAY < 36.75 ms	36.50	F849h
36.75 ms ≤ TOFF_DELAY < 37.25 ms	37.00	F84Ah
37.25 ms ≤ TOFF_DELAY < 37.75 ms	37.50	F84Bh
37.75 ms ≤ TOFF_DELAY < 38.25 ms	38.00	F84Ch
38.25 ms ≤ TOFF_DELAY < 38.75 ms	38.50	F84Dh
38.75 ms ≤ TOFF_DELAY < 39.25 ms	39.00	F84Eh
39.25 ms ≤ TOFF_DELAY < 39.75 ms	39.50	F84Fh
39.75 ms ≤ TOFF_DELAY < 40.25 ms	40.00	F850h
40.25 ms ≤ TOFF_DELAY < 40.75 ms	40.50	F851h
40.75 ms ≤ TOFF_DELAY < 41.25 ms	41.00	F852h
41.25 ms ≤ TOFF_DELAY < 41.75 ms	41.50	F853h
41.75 ms ≤ TOFF_DELAY < 42.25 ms	42.00	F854h
42.25 ms ≤ TOFF_DELAY < 42.75 ms	42.50	F855h
42.75 ms ≤ TOFF_DELAY < 43.25 ms	43.00	F856h
43.25 ms ≤ TOFF_DELAY < 43.75 ms	43.50	F857h
43.75 ms ≤ TOFF_DELAY < 44.25 ms	44.00	F858h
44.25 ms ≤ TOFF_DELAY < 44.75 ms	44.50	F859h
44.75 ms ≤ TOFF_DELAY < 45.25 ms	45.00	F85Ah
45.25 ms ≤ TOFF_DELAY < 45.75 ms	45.50	F85Bh
45.75 ms ≤ TOFF_DELAY < 46.25 ms	46.00	F85Ch
46.25 ms ≤ TOFF_DELAY < 46.75 ms	46.50	F85Dh
46.75 ms ≤ TOFF_DELAY < 47.25 ms	47.00	F85Eh
47.25 ms ≤ TOFF_DELAY < 47.75 ms	47.50	F85Fh
47.75 ms ≤ TOFF_DELAY < 48.25 ms	48.00	F860h
48.25 ms ≤ TOFF_DELAY < 48.75 ms	48.50	F861h
48.75 ms ≤ TOFF_DELAY < 49.25 ms	49.00	F862h
49.25 ms ≤ TOFF_DELAY < 49.75 ms	49.50	F863h
49.75 ms ≤ TOFF_DELAY < 50.25 ms	50.00	F864h
50.25 ms ≤ TOFF_DELAY < 50.75 ms	50.50	F865h
50.75 ms ≤ TOFF_DELAY < 51.25 ms	51.00	F866h
51.25 ms ≤ TOFF_DELAY < 51.75 ms	51.50	F867h

Table 1-86. Supported Value Mapping (continued)

TOFF_DELAY (decoded)	Turn-off Delay (ms)	Nominal SLINEAR11 (hex)
51.75 ms ≤ TOFF_DELAY < 52.25 ms	52.00	F868h
52.25 ms ≤ TOFF_DELAY < 52.75 ms	52.50	F869h
52.75 ms ≤ TOFF_DELAY < 53.25 ms	53.00	F86Ah
53.25 ms ≤ TOFF_DELAY < 53.75 ms	53.50	F86Bh
53.75 ms ≤ TOFF_DELAY < 54.25 ms	54.00	F86Ch
54.25 ms ≤ TOFF_DELAY < 54.75 ms	54.50	F86Dh
54.75 ms ≤ TOFF_DELAY < 55.25 ms	55.00	F86Eh
55.25 ms ≤ TOFF_DELAY < 55.75 ms	55.50	F86Fh
55.75 ms ≤ TOFF_DELAY < 56.25 ms	56.00	F870h
56.25 ms ≤ TOFF_DELAY < 56.75 ms	56.50	F871h
56.75 ms ≤ TOFF_DELAY < 57.25 ms	57.00	F872h
57.25 ms ≤ TOFF_DELAY < 57.75 ms	57.50	F873h
57.75 ms ≤ TOFF_DELAY < 58.25 ms	58.00	F874h
58.25 ms ≤ TOFF_DELAY < 58.75 ms	58.50	F875h
58.75 ms ≤ TOFF_DELAY < 59.25 ms	59.00	F876h
59.25 ms ≤ TOFF_DELAY < 59.75 ms	59.50	F877h
59.75 ms ≤ TOFF_DELAY < 60.25 ms	60.00	F878h
60.25 ms ≤ TOFF_DELAY < 60.75 ms	60.50	F879h
60.75 ms ≤ TOFF_DELAY < 61.25 ms	61.00	F87Ah
61.25 ms ≤ TOFF_DELAY < 61.75 ms	61.50	F87Bh
61.75 ms ≤ TOFF_DELAY < 62.25 ms	62.00	F87Ch
62.25 ms ≤ TOFF_DELAY < 62.75 ms	62.50	F87Dh
62.75 ms ≤ TOFF_DELAY < 63.25 ms	63.00	F87Eh
63.25 ms ≤ TOFF_DELAY < 63.75 ms	63.50	F87Fh
63.75 ms ≤ TOFF_DELAY < 64.25 ms	64.00	F880h
64.25 ms ≤ TOFF_DELAY < 64.75 ms	64.50	F881h
64.75 ms ≤ TOFF_DELAY < 65.25 ms	65.00	F882h
65.25 ms ≤ TOFF_DELAY < 65.75 ms	65.50	F883h
65.75 ms ≤ TOFF_DELAY < 66.25 ms	66.00	F884h
66.25 ms ≤ TOFF_DELAY < 66.75 ms	66.50	F885h
66.75 ms ≤ TOFF_DELAY < 67.25 ms	67.00	F886h
67.25 ms ≤ TOFF_DELAY < 67.75 ms	67.50	F887h
67.75 ms ≤ TOFF_DELAY < 68.25 ms	68.00	F888h
68.25 ms ≤ TOFF_DELAY < 68.75 ms	68.50	F889h
68.75 ms ≤ TOFF_DELAY < 69.25 ms	69.00	F88Ah
69.25 ms ≤ TOFF_DELAY < 69.75 ms	69.50	F88Bh
69.75 ms ≤ TOFF_DELAY < 70.25 ms	70.00	F88Ch
70.25 ms ≤ TOFF_DELAY < 70.75 ms	70.50	F88Dh
70.75 ms ≤ TOFF_DELAY < 71.25 ms	71.00	F88Eh
71.25 ms ≤ TOFF_DELAY < 71.75 ms	71.50	F88Fh
71.75 ms ≤ TOFF_DELAY < 72.25 ms	72.00	F890h
72.25 ms ≤ TOFF_DELAY < 72.75 ms	72.50	F891h
72.75 ms ≤ TOFF_DELAY < 73.25 ms	73.00	F892h
73.25 ms ≤ TOFF_DELAY < 73.75 ms	73.50	F893h
73.75 ms ≤ TOFF_DELAY < 74.25 ms	74.00	F894h

Table 1-86. Supported Value Mapping (continued)

TOFF_DELAY (decoded)	Turn-off Delay (ms)	Nominal SLINEAR11 (hex)
74.25 ms ≤ TOFF_DELAY < 74.75 ms	74.50	F895h
74.75 ms ≤ TOFF_DELAY < 75.25 ms	75.00	F896h
75.25 ms ≤ TOFF_DELAY < 75.75 ms	75.50	F897h
75.75 ms ≤ TOFF_DELAY < 76.25 ms	76.00	F898h
76.25 ms ≤ TOFF_DELAY < 76.75 ms	76.50	F899h
76.75 ms ≤ TOFF_DELAY < 77.25 ms	77.00	F89Ah
77.25 ms ≤ TOFF_DELAY < 77.75 ms	77.50	F89Bh
77.75 ms ≤ TOFF_DELAY < 78.25 ms	78.00	F89Ch
78.25 ms ≤ TOFF_DELAY < 78.75 ms	78.50	F89Dh
78.75 ms ≤ TOFF_DELAY < 79.25 ms	79.00	F89Eh
79.25 ms ≤ TOFF_DELAY < 79.75 ms	79.50	F89Fh
79.75 ms ≤ TOFF_DELAY < 80.25 ms	80.00	F8A0h
80.25 ms ≤ TOFF_DELAY < 80.75 ms	80.50	F8A1h
80.75 ms ≤ TOFF_DELAY < 81.25 ms	81.00	F8A2h
81.25 ms ≤ TOFF_DELAY < 81.75 ms	81.50	F8A3h
81.75 ms ≤ TOFF_DELAY < 82.25 ms	82.00	F8A4h
82.25 ms ≤ TOFF_DELAY < 82.75 ms	82.50	F8A5h
82.75 ms ≤ TOFF_DELAY < 83.25 ms	83.00	F8A6h
83.25 ms ≤ TOFF_DELAY < 83.75 ms	83.50	F8A7h
83.75 ms ≤ TOFF_DELAY < 84.25 ms	84.00	F8A8h
84.25 ms ≤ TOFF_DELAY < 84.75 ms	84.50	F8A9h
84.75 ms ≤ TOFF_DELAY < 85.25 ms	85.00	F8AAh
85.25 ms ≤ TOFF_DELAY < 85.75 ms	85.50	F8ABh
85.75 ms ≤ TOFF_DELAY < 86.25 ms	86.00	F8ACh
86.25 ms ≤ TOFF_DELAY < 86.75 ms	86.50	F8ADh
86.75 ms ≤ TOFF_DELAY < 87.25 ms	87.00	F8AEh
87.25 ms ≤ TOFF_DELAY < 87.75 ms	87.50	F8AFh
87.75 ms ≤ TOFF_DELAY < 88.25 ms	88.00	F8B0h
88.25 ms ≤ TOFF_DELAY < 88.75 ms	88.50	F8B1h
88.75 ms ≤ TOFF_DELAY < 89.25 ms	89.00	F8B2h
89.25 ms ≤ TOFF_DELAY < 89.75 ms	89.50	F8B3h
89.75 ms ≤ TOFF_DELAY < 90.25 ms	90.00	F8B4h
90.25 ms ≤ TOFF_DELAY < 90.75 ms	90.50	F8B5h
90.75 ms ≤ TOFF_DELAY < 91.25 ms	91.00	F8B6h
91.25 ms ≤ TOFF_DELAY < 91.75 ms	91.50	F8B7h
91.75 ms ≤ TOFF_DELAY < 92.25 ms	92.00	F8B8h
92.25 ms ≤ TOFF_DELAY < 92.75 ms	92.50	F8B9h
92.75 ms ≤ TOFF_DELAY < 93.25 ms	93.00	F8BAh
93.25 ms ≤ TOFF_DELAY < 93.75 ms	93.50	F8BBh
93.75 ms ≤ TOFF_DELAY < 94.25 ms	94.00	F8BCh
94.25 ms ≤ TOFF_DELAY < 94.75 ms	94.50	F8BDh
94.75 ms ≤ TOFF_DELAY < 95.25 ms	95.00	F8BEh
95.25 ms ≤ TOFF_DELAY < 95.75 ms	95.50	F8BFh
95.75 ms ≤ TOFF_DELAY < 96.25 ms	96.00	F8C0h
96.25 ms ≤ TOFF_DELAY < 96.75 ms	96.50	F8C1h

Table 1-86. Supported Value Mapping (continued)

TOFF_DELAY (decoded)	Turn-off Delay (ms)	Nominal SLINEAR11 (hex)
96.75 ms ≤ TOFF_DELAY < 97.25 ms	97.00	F8C2h
97.25 ms ≤ TOFF_DELAY < 97.75 ms	97.50	F8C3h
97.75 ms ≤ TOFF_DELAY < 98.25 ms	98.00	F8C4h
98.25 ms ≤ TOFF_DELAY < 98.75 ms	98.50	F8C5h
98.75 ms ≤ TOFF_DELAY < 99.25 ms	99.00	F8C6h
99.25 ms ≤ TOFF_DELAY < 99.75 ms	99.50	F8C7h
99.75 ms ≤ TOFF_DELAY < 100.25 ms	100.00	F8C8h
100.25 ms ≤ TOFF_DELAY < 100.75 ms	100.50	F8C9h
100.75 ms ≤ TOFF_DELAY < 101.25 ms	101.00	F8CAh
101.25 ms ≤ TOFF_DELAY < 101.75 ms	101.50	F8CBh
101.75 ms ≤ TOFF_DELAY < 102.25 ms	102.00	F8CCh
102.25 ms ≤ TOFF_DELAY < 102.75 ms	102.50	F8CDh
102.75 ms ≤ TOFF_DELAY < 103.25 ms	103.00	F8CEh
103.25 ms ≤ TOFF_DELAY < 103.75 ms	103.50	F8CFh
103.75 ms ≤ TOFF_DELAY < 104.25 ms	104.00	F8D0h
104.25 ms ≤ TOFF_DELAY < 104.75 ms	104.50	F8D1h
104.75 ms ≤ TOFF_DELAY < 105.25 ms	105.00	F8D2h
105.25 ms ≤ TOFF_DELAY < 105.75 ms	105.50	F8D3h
105.75 ms ≤ TOFF_DELAY < 106.25 ms	106.00	F8D4h
106.25 ms ≤ TOFF_DELAY < 106.75 ms	106.50	F8D5h
106.75 ms ≤ TOFF_DELAY < 107.25 ms	107.00	F8D6h
107.25 ms ≤ TOFF_DELAY < 107.75 ms	107.50	F8D7h
107.75 ms ≤ TOFF_DELAY < 108.25 ms	108.00	F8D8h
108.25 ms ≤ TOFF_DELAY < 108.75 ms	108.50	F8D9h
108.75 ms ≤ TOFF_DELAY < 109.25 ms	109.00	F8DAh
109.25 ms ≤ TOFF_DELAY < 109.75 ms	109.50	F8DBh
109.75 ms ≤ TOFF_DELAY < 110.25 ms	110.00	F8DCh
110.25 ms ≤ TOFF_DELAY < 110.75 ms	110.50	F8DDh
110.75 ms ≤ TOFF_DELAY < 111.25 ms	111.00	F8DEh
111.25 ms ≤ TOFF_DELAY < 111.75 ms	111.50	F8DFh
111.75 ms ≤ TOFF_DELAY < 112.25 ms	112.00	F8E0h
112.25 ms ≤ TOFF_DELAY < 112.75 ms	112.50	F8E1h
112.75 ms ≤ TOFF_DELAY < 113.25 ms	113.00	F8E2h
113.25 ms ≤ TOFF_DELAY < 113.75 ms	113.50	F8E3h
113.75 ms ≤ TOFF_DELAY < 114.25 ms	114.00	F8E4h
114.25 ms ≤ TOFF_DELAY < 114.75 ms	114.50	F8E5h
114.75 ms ≤ TOFF_DELAY < 115.25 ms	115.00	F8E6h
115.25 ms ≤ TOFF_DELAY < 115.75 ms	115.50	F8E7h
115.75 ms ≤ TOFF_DELAY < 116.25 ms	116.00	F8E8h
116.25 ms ≤ TOFF_DELAY < 116.75 ms	116.50	F8E9h
116.75 ms ≤ TOFF_DELAY < 117.25 ms	117.00	F8EAh
117.25 ms ≤ TOFF_DELAY < 117.75 ms	117.50	F8EBh
117.75 ms ≤ TOFF_DELAY < 118.25 ms	118.00	F8ECh
118.25 ms ≤ TOFF_DELAY < 118.75 ms	118.50	F8EDh
118.75 ms ≤ TOFF_DELAY < 119.25 ms	119.00	F8EEh

Table 1-86. Supported Value Mapping (continued)

TOFF_DELAY (decoded)	Turn-off Delay (ms)	Nominal SLINEAR11 (hex)
119.25 ms ≤ TOFF_DELAY < 119.75 ms	119.50	F8EFh
119.75 ms ≤ TOFF_DELAY < 120.25 ms	120.00	F8F0h
120.25 ms ≤ TOFF_DELAY < 120.75 ms	120.50	F8F1h
120.75 ms ≤ TOFF_DELAY < 121.25 ms	121.00	F8F2h
121.25 ms ≤ TOFF_DELAY < 121.75 ms	121.50	F8F3h
121.75 ms ≤ TOFF_DELAY < 122.25 ms	122.00	F8F4h
122.25 ms ≤ TOFF_DELAY < 122.75 ms	122.50	F8F5h
122.75 ms ≤ TOFF_DELAY < 123.25 ms	123.00	F8F6h
123.25 ms ≤ TOFF_DELAY < 123.75 ms	123.50	F8F7h
123.75 ms ≤ TOFF_DELAY < 124.25 ms	124.00	F8F8h
124.25 ms ≤ TOFF_DELAY < 124.75 ms	124.50	F8F9h
124.75 ms ≤ TOFF_DELAY < 125.25 ms	125.00	F8FAh
125.25 ms ≤ TOFF_DELAY < 125.75 ms	125.50	F8FBh
125.75 ms ≤ TOFF_DELAY < 126.25 ms	126.00	F8FCh
126.25 ms ≤ TOFF_DELAY < 126.75 ms	126.50	F8FDh
126.75 ms ≤ TOFF_DELAY < 127.25 ms	127.00	F8FEh
127.25 ms ≤ TOFF_DELAY ≤ 127.5 ms	127.50	F8FFh
TOFF_DELAY > 127.5 ms	Invalid/Unsupported	Invalid/Unsupported

1.2.63 (65h) TOFF_FALL

CMD Address	65h
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	SLINEAR11
Paged:	Yes
Phased:	No
NVM Back-up:	EEPROM
Updates:	On-the-fly

The TOFF_FALL command sets the time, in milliseconds, from the end of the turn-off delay time until the voltage is commanded to zero. Note that this command can only be used with a device whose output can sink enough current to cause the output voltage to decrease at a controlled rate. This effectively sets the slew rate of the reference DAC during the soft-off period. Note that the fall time is equal to TOFF_FALL regardless of the value of the target output voltage or VOUT_SCALE_LOOP . For the purposes of slew rate selection based on the target output voltage, the TPS536xx assumes a zero-loadline configuration.

Note: The fall time during power-down will not match the value programmed into TOFF_FALL . Instead, the TPS536xx will calculate the desired slew rate as SR_{OFF} = VBOOT / TOFF_FALL, and select the nearest supported transition rate, as described in the product datasheet.

(65h) TOFF_FALL Register Map

15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
TOFFF_EXP					TOFFF_MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
TOFFF_MAN							

LEGEND: R/W = Read/Write; R = Read only

Table 1-87. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:11	TOFFF_EXP	RW	11110b	Linear format two's complement exponent. Exponent = -2, LSB = 0.25 ms
10:0	TOFFF_MAN	RW	NVM	Linear format two's complement mantissa.

Attempts to write (65h) TOFF_FALL will be considered invalid/unsupported command and cause TPS536xx to respond by flagging the appropriate status bits, and notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

Table 1-88. Supported Value Mapping

TOFF_FALL (decoded)	Turn-off Time (ms)	Nominal SLINEAR11 (hex)
TOFF_FALL = 0 ms	0.25 ms	F000h
0 ms < TOFF_FALL < 0.375 ms	0.25	F001h
0.375 ms ≤ TOFF_FALL < 0.625 ms	0.50	F002h
0.625 ms ≤ TOFF_FALL < 0.875 ms	0.75	F003h
0.875 ms ≤ TOFF_FALL < 1.125 ms	1.00	F004h
1.125 ms ≤ TOFF_FALL < 1.375 ms	1.25	F005h
1.375 ms ≤ TOFF_FALL < 1.625 ms	1.50	F006h

Table 1-88. Supported Value Mapping (continued)

TOFF_FALL (decoded)	Turn-off Time (ms)	Nominal SLINEAR11 (hex)
1.625 ms ≤ TOFF_FALL < 1.875 ms	1.75	F007h
1.875 ms ≤ TOFF_FALL < 2.125 ms	2.00	F008h
2.125 ms ≤ TOFF_FALL < 2.375 ms	2.25	F009h
2.375 ms ≤ TOFF_FALL < 2.625 ms	2.50	F00Ah
2.625 ms ≤ TOFF_FALL < 2.875 ms	2.75	F00Bh
2.875 ms ≤ TOFF_FALL < 3.125 ms	3.00	F00Ch
3.125 ms ≤ TOFF_FALL < 3.375 ms	3.25	F00Dh
3.375 ms ≤ TOFF_FALL < 3.625 ms	3.50	F00Eh
3.625 ms ≤ TOFF_FALL < 3.875 ms	3.75	F00Fh
3.875 ms ≤ TOFF_FALL < 4.125 ms	4.00	F010h
4.125 ms ≤ TOFF_FALL < 4.375 ms	4.25	F011h
4.375 ms ≤ TOFF_FALL < 4.625 ms	4.50	F012h
4.625 ms ≤ TOFF_FALL < 4.875 ms	4.75	F013h
4.875 ms ≤ TOFF_FALL < 5.125 ms	5.00	F014h
5.125 ms ≤ TOFF_FALL < 5.375 ms	5.25	F015h
5.375 ms ≤ TOFF_FALL < 5.625 ms	5.50	F016h
5.625 ms ≤ TOFF_FALL < 5.875 ms	5.75	F017h
5.875 ms ≤ TOFF_FALL < 6.125 ms	6.00	F018h
6.125 ms ≤ TOFF_FALL < 6.375 ms	6.25	F019h
6.375 ms ≤ TOFF_FALL < 6.625 ms	6.50	F01Ah
6.625 ms ≤ TOFF_FALL < 6.875 ms	6.75	F01Bh
6.875 ms ≤ TOFF_FALL < 7.125 ms	7.00	F01Ch
7.125 ms ≤ TOFF_FALL < 7.375 ms	7.25	F01Dh
7.375 ms ≤ TOFF_FALL < 7.625 ms	7.50	F01Eh
7.625 ms ≤ TOFF_FALL < 7.875 ms	7.75	F01Fh
7.875 ms ≤ TOFF_FALL < 8.125 ms	8.00	F020h
8.125 ms ≤ TOFF_FALL < 8.375 ms	8.25	F021h
8.375 ms ≤ TOFF_FALL < 8.625 ms	8.50	F022h
8.625 ms ≤ TOFF_FALL < 8.875 ms	8.75	F023h
8.875 ms ≤ TOFF_FALL < 9.125 ms	9.00	F024h
9.125 ms ≤ TOFF_FALL < 9.375 ms	9.25	F025h
9.375 ms ≤ TOFF_FALL < 9.625 ms	9.50	F026h
9.625 ms ≤ TOFF_FALL < 9.875 ms	9.75	F027h
9.875 ms ≤ TOFF_FALL < 10.125 ms	10.00	F028h
10.125 ms ≤ TOFF_FALL < 10.375 ms	10.25	F029h
10.375 ms ≤ TOFF_FALL < 10.625 ms	10.50	F02Ah
10.625 ms ≤ TOFF_FALL < 10.875 ms	10.75	F02Bh
10.875 ms ≤ TOFF_FALL < 11.125 ms	11.00	F02Ch
11.125 ms ≤ TOFF_FALL < 11.375 ms	11.25	F02Dh
11.375 ms ≤ TOFF_FALL < 11.625 ms	11.50	F02Eh
11.625 ms ≤ TOFF_FALL < 11.875 ms	11.75	F02Fh
11.875 ms ≤ TOFF_FALL < 12.125 ms	12.00	F030h
12.125 ms ≤ TOFF_FALL < 12.375 ms	12.25	F031h
12.375 ms ≤ TOFF_FALL < 12.625 ms	12.50	F032h
12.625 ms ≤ TOFF_FALL < 12.875 ms	12.75	F033h

Table 1-88. Supported Value Mapping (continued)

TOFF_FALL (decoded)	Turn-off Time (ms)	Nominal SLINEAR11 (hex)
12.875 ms ≤ TOFF_FALL < 13.125 ms	13.00	F034h
13.125 ms ≤ TOFF_FALL < 13.375 ms	13.25	F035h
13.375 ms ≤ TOFF_FALL < 13.625 ms	13.50	F036h
13.625 ms ≤ TOFF_FALL < 13.875 ms	13.75	F037h
13.875 ms ≤ TOFF_FALL < 14.125 ms	14.00	F038h
14.125 ms ≤ TOFF_FALL < 14.375 ms	14.25	F039h
14.375 ms ≤ TOFF_FALL < 14.625 ms	14.50	F03Ah
14.625 ms ≤ TOFF_FALL < 14.875 ms	14.75	F03Bh
14.875 ms ≤ TOFF_FALL < 15.125 ms	15.00	F03Ch
15.125 ms ≤ TOFF_FALL < 15.375 ms	15.25	F03Dh
15.375 ms ≤ TOFF_FALL < 15.625 ms	15.50	F03Eh
15.625 ms ≤ TOFF_FALL < 15.875 ms	15.75	F03Fh
15.875 ms ≤ TOFF_FALL < 16.125 ms	16.00	F040h
16.125 ms ≤ TOFF_FALL < 16.375 ms	16.25	F041h
16.375 ms ≤ TOFF_FALL < 16.625 ms	16.50	F042h
16.625 ms ≤ TOFF_FALL < 16.875 ms	16.75	F043h
16.875 ms ≤ TOFF_FALL < 17.125 ms	17.00	F044h
17.125 ms ≤ TOFF_FALL < 17.375 ms	17.25	F045h
17.375 ms ≤ TOFF_FALL < 17.625 ms	17.50	F046h
17.625 ms ≤ TOFF_FALL < 17.875 ms	17.75	F047h
17.875 ms ≤ TOFF_FALL < 18.125 ms	18.00	F048h
18.125 ms ≤ TOFF_FALL < 18.375 ms	18.25	F049h
18.375 ms ≤ TOFF_FALL < 18.625 ms	18.50	F04Ah
18.625 ms ≤ TOFF_FALL < 18.875 ms	18.75	F04Bh
18.875 ms ≤ TOFF_FALL < 19.125 ms	19.00	F04Ch
19.125 ms ≤ TOFF_FALL < 19.375 ms	19.25	F04Dh
19.375 ms ≤ TOFF_FALL < 19.625 ms	19.50	F04Eh
19.625 ms ≤ TOFF_FALL < 19.875 ms	19.75	F04Fh
19.875 ms ≤ TOFF_FALL < 20.125 ms	20.00	F050h
20.125 ms ≤ TOFF_FALL < 20.375 ms	20.25	F051h
20.375 ms ≤ TOFF_FALL < 20.625 ms	20.50	F052h
20.625 ms ≤ TOFF_FALL < 20.875 ms	20.75	F053h
20.875 ms ≤ TOFF_FALL < 21.125 ms	21.00	F054h
21.125 ms ≤ TOFF_FALL < 21.375 ms	21.25	F055h
21.375 ms ≤ TOFF_FALL < 21.625 ms	21.50	F056h
21.625 ms ≤ TOFF_FALL < 21.875 ms	21.75	F057h
21.875 ms ≤ TOFF_FALL < 22.125 ms	22.00	F058h
22.125 ms ≤ TOFF_FALL < 22.375 ms	22.25	F059h
22.375 ms ≤ TOFF_FALL < 22.625 ms	22.50	F05Ah
22.625 ms ≤ TOFF_FALL < 22.875 ms	22.75	F05Bh
22.875 ms ≤ TOFF_FALL < 23.125 ms	23.00	F05Ch
23.125 ms ≤ TOFF_FALL < 23.375 ms	23.25	F05Dh
23.375 ms ≤ TOFF_FALL < 23.625 ms	23.50	F05Eh
23.625 ms ≤ TOFF_FALL < 23.875 ms	23.75	F05Fh
23.875 ms ≤ TOFF_FALL < 24.125 ms	24.00	F060h

Table 1-88. Supported Value Mapping (continued)

TOFF_FALL (decoded)	Turn-off Time (ms)	Nominal SLINEAR11 (hex)
24.125 ms ≤ TOFF_FALL < 24.375 ms	24.25	F061h
24.375 ms ≤ TOFF_FALL < 24.625 ms	24.50	F062h
24.625 ms ≤ TOFF_FALL < 24.875 ms	24.75	F063h
24.875 ms ≤ TOFF_FALL < 25.125 ms	25.00	F064h
25.125 ms ≤ TOFF_FALL < 25.375 ms	25.25	F065h
25.375 ms ≤ TOFF_FALL < 25.625 ms	25.50	F066h
25.625 ms ≤ TOFF_FALL < 25.875 ms	25.75	F067h
25.875 ms ≤ TOFF_FALL < 26.125 ms	26.00	F068h
26.125 ms ≤ TOFF_FALL < 26.375 ms	26.25	F069h
26.375 ms ≤ TOFF_FALL < 26.625 ms	26.50	F06Ah
26.625 ms ≤ TOFF_FALL < 26.875 ms	26.75	F06Bh
26.875 ms ≤ TOFF_FALL < 27.125 ms	27.00	F06Ch
27.125 ms ≤ TOFF_FALL < 27.375 ms	27.25	F06Dh
27.375 ms ≤ TOFF_FALL < 27.625 ms	27.50	F06Eh
27.625 ms ≤ TOFF_FALL < 27.875 ms	27.75	F06Fh
27.875 ms ≤ TOFF_FALL < 28.125 ms	28.00	F070h
28.125 ms ≤ TOFF_FALL < 28.375 ms	28.25	F071h
28.375 ms ≤ TOFF_FALL < 28.625 ms	28.50	F072h
28.625 ms ≤ TOFF_FALL < 28.875 ms	28.75	F073h
28.875 ms ≤ TOFF_FALL < 29.125 ms	29.00	F074h
29.125 ms ≤ TOFF_FALL < 29.375 ms	29.25	F075h
29.375 ms ≤ TOFF_FALL < 29.625 ms	29.50	F076h
29.625 ms ≤ TOFF_FALL < 29.875 ms	29.75	F077h
29.875 ms ≤ TOFF_FALL < 30.125 ms	30.00	F078h
30.125 ms ≤ TOFF_FALL < 30.375 ms	30.25	F079h
30.375 ms ≤ TOFF_FALL < 30.625 ms	30.50	F07Ah
30.625 ms ≤ TOFF_FALL < 30.875 ms	30.75	F07Bh
30.875 ms ≤ TOFF_FALL < 31.125 ms	31.00	F07Ch
31.125 ms ≤ TOFF_FALL < 31.375 ms	31.25	F07Dh
31.375 ms ≤ TOFF_FALL < 31.625 ms	31.50	F07Eh
31.625 ms ≤ TOFF_FALL ≤ 31.75 ms	31.75	F07Fh
TOFF_FALL > 31.75 ms	Invalid/Unsupported	Invalid/Unsupported

1.2.64 (6Bh) PIN_OP_WARN_LIMIT

CMD Address	6Bh
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	SLINEAR11
Paged:	No
Phased:	No
NVM Back-up:	EEPROM

The PIN_OP_WARN_LIMIT command sets the value of the input power, in watts, that causes a warning that the input power is high.

In response to the PIN_OP_WARN_LIMIT limit being exceeded, the TPS536xx responds as follows:

- Set the NONE OF THE ABOVE bit in the STATUS_BYTE
- Set the INPUT bit in the STATUS_WORD
- Set the PIN OPW bit in STATUS_INPUT
- Notify the host per PMBus 1.3.1 Part II specification, section 10.2

(6Bh) PIN_OP_WARN_LIMIT Register Map

15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
PIOPW EXP					PIOPW MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
PIOPW MAN							

LEGEND: R/W = Read/Write; R = Read only

Table 1-89. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:11	PIOPW EXP	RW	00001b	Linear format two's complement exponent.
10:0	PIOPW MAN	RW	NVM	Linear format two's complement mantissa.

Attempts to write (6Bh) PIN_OP_WARN_LIMIT will be considered invalid/unsupported command and cause TPS536xx to respond by flagging the appropriate status bits, and notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

Command Resolution and NVM Store/Restore Behavior

The (6Bh) PIN_OP_WARN_LIMIT command is implemented using the TPS536xx internal telemetry system. As a result the value of this command may be programmed with very high resolution using the linear format. However, the TPS536xx provides only limited NVM-backed options for this command. Following a power-cycle or NVM Store/Restore operation, the value will be restored to one of the values in the table below, according to the value present during the last NVM store operation. Refer to the table below. During operation, updates to this command with higher resolution than the options in the NVM supported table, will be supported, and accepted as long as they fall between the minimum and maximum supported values given.

Table 1-90. Supported Values

PIN_OP_WARN_LIMIT (decoded) during last NVM Store	Reset Value (decoded) PIN Overpower Warning (W)	Nominal SLINEAR11 (hex)
PIN OPW < 8W	Invalid/Unsupported	Invalid/Unsupported
8 W ≤ PIN OPW < 12 W	8	0804h

Table 1-90. Supported Values (continued)

PIN_OP_WARN_LIMIT (decoded) during last NVM Store	Reset Value (decoded) PIN Overpower Warning (W)	Nominal SLINEAR11 (hex)
12 W ≤ PIN OPW < 20 W	16	0808h
20 W ≤ PIN OPW < 28 W	24	080Ch
28 W ≤ PIN OPW < 36 W	32	0810h
36 W ≤ PIN OPW < 44 W	40	0814h
44 W ≤ PIN OPW < 52 W	48	0818h
52 W ≤ PIN OPW < 60 W	56	081Ch
60 W ≤ PIN OPW < 68 W	64	0820h
68 W ≤ PIN OPW < 76 W	72	0824h
76 W ≤ PIN OPW < 84 W	80	0828h
84 W ≤ PIN OPW < 92 W	88	082Ch
92 W ≤ PIN OPW < 100 W	96	0830h
100 W ≤ PIN OPW < 108 W	104	0834h
108 W ≤ PIN OPW < 116 W	112	0838h
116 W ≤ PIN OPW < 124 W	120	083Ch
124 W ≤ PIN OPW < 132 W	128	0840h
132 W ≤ PIN OPW < 140 W	136	0844h
140 W ≤ PIN OPW < 148 W	144	0848h
148 W ≤ PIN OPW < 156 W	152	084Ch
156 W ≤ PIN OPW < 164 W	160	0850h
164 W ≤ PIN OPW < 172 W	168	0854h
172 W ≤ PIN OPW < 180 W	176	0858h
180 W ≤ PIN OPW < 188 W	184	085Ch
188 W ≤ PIN OPW < 196 W	192	0860h
196 W ≤ PIN OPW < 204 W	200	0864h
204 W ≤ PIN OPW < 212 W	208	0868h
212 W ≤ PIN OPW < 220 W	216	086Ch
220 W ≤ PIN OPW < 228 W	224	0870h
228 W ≤ PIN OPW < 236 W	232	0874h
236 W ≤ PIN OPW < 244 W	240	0878h
244 W ≤ PIN OPW < 252 W	248	087Ch
252 W ≤ PIN OPW < 260 W	256	0880h
260 W ≤ PIN OPW < 268 W	264	0884h
268 W ≤ PIN OPW < 276 W	272	0888h
276 W ≤ PIN OPW < 284 W	280	088Ch
284 W ≤ PIN OPW < 292 W	288	0890h
292 W ≤ PIN OPW < 300 W	296	0894h
300 W ≤ PIN OPW < 308 W	304	0898h
308 W ≤ PIN OPW < 316 W	312	089Ch
316 W ≤ PIN OPW < 324 W	320	08A0h
324 W ≤ PIN OPW < 332 W	328	08A4h
332 W ≤ PIN OPW < 340 W	336	08A8h
340 W ≤ PIN OPW < 348 W	344	08ACh
348 W ≤ PIN OPW < 356 W	352	08B0h
356 W ≤ PIN OPW < 364 W	360	08B4h

Table 1-90. Supported Values (continued)

PIN_OP_WARN_LIMIT (decoded) during last NVM Store	Reset Value (decoded) PIN Overpower Warning (W)	Nominal SLINEAR11 (hex)
364 W ≤ PIN OPW < 372 W	368	08B8h
372 W ≤ PIN OPW < 380 W	376	08BCh
380 W ≤ PIN OPW < 388 W	384	08C0h
388 W ≤ PIN OPW < 396 W	392	08C4h
396 W ≤ PIN OPW < 404 W	400	08C8h
404 W ≤ PIN OPW < 412 W	408	08CCh
412 W ≤ PIN OPW < 420 W	416	08D0h
420 W ≤ PIN OPW < 428 W	424	08D4h
428 W ≤ PIN OPW < 436 W	432	08D8h
436 W ≤ PIN OPW < 444 W	440	08DCh
444 W ≤ PIN OPW < 452 W	448	08E0h
452 W ≤ PIN OPW < 460 W	456	08E4h
460 W ≤ PIN OPW < 468 W	464	08E8h
468 W ≤ PIN OPW < 476 W	472	08ECh
476 W ≤ PIN OPW < 484 W	480	08F0h
484 W ≤ PIN OPW < 492 W	488	08F4h
492 W ≤ PIN OPW < 500 W	496	08F8h
500 W ≤ PIN OPW < 508 W	504	08FCh
508 W ≤ PIN OPW < 520 W	512	0900h
520 W ≤ PIN OPW < 536 W	528	0908h
536 W ≤ PIN OPW < 552 W	544	0910h
552 W ≤ PIN OPW < 568 W	560	0918h
568 W ≤ PIN OPW < 584 W	576	0920h
584 W ≤ PIN OPW < 600 W	592	0928h
600 W ≤ PIN OPW < 616 W	608	0930h
616 W ≤ PIN OPW < 632 W	624	0938h
632 W ≤ PIN OPW < 648 W	640	0940h
648 W ≤ PIN OPW < 664 W	656	0948h
664 W ≤ PIN OPW < 680 W	672	0950h
680 W ≤ PIN OPW < 696 W	688	0958h
696 W ≤ PIN OPW < 712 W	704	0960h
712 W ≤ PIN OPW < 728 W	720	0968h
728 W ≤ PIN OPW < 744 W	736	0970h
744 W ≤ PIN OPW < 760 W	752	0978h
760 W ≤ PIN OPW < 776 W	768	0980h
776 W ≤ PIN OPW < 792 W	784	0988h
792 W ≤ PIN OPW < 808 W	800	0990h
808 W ≤ PIN OPW < 824 W	816	0998h
824 W ≤ PIN OPW < 840 W	832	09A0h
840 W ≤ PIN OPW < 856 W	848	09A8h
856 W ≤ PIN OPW < 872 W	864	09B0h
872 W ≤ PIN OPW < 888 W	880	09B8h
888 W ≤ PIN OPW < 904 W	896	09C0h
904 W ≤ PIN OPW < 920 W	912	09C8h

Table 1-90. Supported Values (continued)

PIN_OP_WARN_LIMIT (decoded) during last NVM Store	Reset Value (decoded) PIN Overpower Warning (W)	Nominal SLINEAR11 (hex)
920 W ≤ PIN OPW < 936 W	928	09D0h
936 W ≤ PIN OPW < 952 W	944	09D8h
952 W ≤ PIN OPW < 968 W	960	09E0h
968 W ≤ PIN OPW < 984 W	976	09E8h
984 W ≤ PIN OPW < 1000 W	992	09F0h
1000 W ≤ PIN OPW < 1016 W	1008	09F8h
1016 W ≤ PIN OPW < 1040 W	1024	0A00h
1040 W ≤ PIN OPW < 1072 W	1056	0A10h
1072 W ≤ PIN OPW < 1104 W	1088	0A20h
1104 W ≤ PIN OPW < 1136 W	1120	0A30h
1136 W ≤ PIN OPW < 1168 W	1152	0A40h
1168 W ≤ PIN OPW < 1200 W	1184	0A50h
1200 W ≤ PIN OPW < 1232 W	1216	0A60h
1232 W ≤ PIN OPW < 1264 W	1248	0A70h
1264 W ≤ PIN OPW < 1296 W	1280	0A80h
1296 W ≤ PIN OPW < 1328 W	1312	0A90h
1328 W ≤ PIN OPW < 1360 W	1344	0AA0h
1360 W ≤ PIN OPW < 1392 W	1376	0AB0h
1392 W ≤ PIN OPW < 1424 W	1408	0AC0h
1424 W ≤ PIN OPW < 1456 W	1440	0AD0h
1456 W ≤ PIN OPW < 1488 W	1472	0AE0h
1488 W ≤ PIN OPW < 1520 W	1504	0AF0h
1520 W ≤ PIN OPW < 1552 W	1536	0B00h
1552 W ≤ PIN OPW < 1584 W	1568	0B10h
1584 W ≤ PIN OPW < 1616 W	1600	0B20h
1616 W ≤ PIN OPW < 1648 W	1632	0B30h
1648 W ≤ PIN OPW < 1680 W	1664	0B40h
1680 W ≤ PIN OPW < 1712 W	1696	0B50h
1712 W ≤ PIN OPW < 1744 W	1728	0B60h
1744 W ≤ PIN OPW < 1776 W	1760	0B70h
1776 W ≤ PIN OPW < 1808 W	1792	0B80h
1808 W ≤ PIN OPW < 1840 W	1824	0B90h
1840 W ≤ PIN OPW < 1872 W	1856	0BA0h
1872 W ≤ PIN OPW < 1904 W	1888	0BB0h
1904 W ≤ PIN OPW < 1936 W	1920	0BC0h
1936 W ≤ PIN OPW < 1968 W	1952	0BD0h
1968 W ≤ PIN OPW < 2000 W	1984	0BE0h
2000 W ≤ PIN OPW < 2032 W	2016	0BF0h
PIN OPW > 2048	Invalid/Unsupported	Invalid/Unsupported

1.2.65 (78h) STATUS_BYTE

CMD Address	78h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
Paged:	Yes
Phased:	No
NVM Back-up:	No
Updates:	On-the-fly

The STATUS_BYTE command returns one byte of information with a summary of the most critical faults, such as over-voltage, over-current, over-temperature, etc. The supported STATUS_BYTE message content is described in the following table. The STATUS_BYTE is equal the low byte of STATUS_WORD . The conditions in the STATUS_BYTE are summary information only. These conditions inform the host as to which other STATUS registers to assess in the event of a fault. These bits must be set and cleared in the individual status registers. For instance, clearing VOUT_OVF in STATUS_VOUT also clears VOUT_OV in STATUS_BYTE .

(78h) STATUS_BYTE Register Map

7	6	5	4	3	2	1	0
RW	R	R	R	R	R	R	R
BUSY	OFF	VOUT OV	IOUT OC	VIN UV	TEMP	CML	NONE OF THE ABOVE

LEGEND: R/W = Read/Write; R = Read only

Table 1-91. Register Field Descriptions

Bit	Field	Access	Reset	Description
7	BUSY	RW	0b	0b: A fault was NOT declared because the device was busy and unable to respond. 1b. A fault was declared because the device was busy and unable to respond.
6	OFF	R	0b	LIVE (unlatched) status bit. 0b. The unit is enabled and converting power. 1b: The unit is NOT converting power for any reason including simply not being enabled.
5	VOUT OV	R	0b	0b: An output over-voltage fault has NOT occurred 1b: An output over-voltage fault has occurred
4	IOUT OC	R	0b	0b: An output over-current fault has NOT occurred 1b: An output over-current fault has occurred
3	VIN UV	R	0b	0b: An input under-voltage fault has NOT occurred 1b: An input under-voltage fault has occurred
2	TEMP	R	0b	0b: A temperature fault/warning has NOT occurred. 1b: A temperature fault/warning has NOT occurred, the host checks STATUS_TEMPERATURE for more information.
1	CML	R	0b	0b: A communication, memory, logic fault has NOT occurred. 1b: A communication, memory, logic fault has occurred, the host checks STATUS_CML for more information
0	NONE OF THE ABOVE	R	0b	0b: A fault other than those listed above has NOT occurred, 1b: A fault other than those listed above has occurred. The host checks the STATUS_WORD for more information.

1.2.66 (79h) STATUS_WORD

CMD Address	79h
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	Unsigned Binary (2 bytes)
Paged:	Yes
Phased:	No
NVM Back-up:	No
Updates:	On-the-fly

The STATUS_WORD command returns two bytes of information with a summary of the most critical faults, such as over-voltage, over-current, over-temperature, etc. The low byte of the STATUS_WORD is the same register as the STATUS_BYTE . The supported STATUS_WORD message content is described in the following table. The conditions in the STATUS_BYTE are summary information only.

(79h) STATUS_WORD Register Map

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
VOUT	IOUT	INPUT	MFR	PGOOD	0	OTHER	0
7	6	5	4	3	2	1	0
RW	R	R	R	R	R	R	R
STATUS BYTE							

LEGEND: R/W = Read/Write; R = Read only

Table 1-92. Register Field Descriptions

Bit	Field	Access	Reset	Description
15	VOUT	R	0b	0b: An output voltage related fault has NOT occurred. 1b: An output voltage fault has occurred. The host should check STATUS_VOUT for more information
14	IOUT	R	0b	0b: An output current related fault has NOT occurred. 1b: An output current fault has occurred. The host should check STATUS_IOUT for more information
13	INPUT	R	0b	0b: An input related fault has NOT occurred. 1b: An input fault has occurred. The host should check STATUS_INPUT for more information
12	MFR	R	0b	0b: A Manufacturer-defined fault has NOT occurred. 1b: A Manufacturer-defined fault has occurred. The host should check STATUS_MFR_SPECIFIC for more information
11	PGOOD	R	0b	LIVE (unlatched) status bit. Should follow always the value of the PGOOD/VR RDY pin is asserted. Note, this bit does not set SMBALERT# . SMBALERT_MASK for PGOOD bit is hardcoded to 1b. 0b: The output voltage is within the regulation window. PGOOD pin is de-asserted. 1b: The output voltage is NOT within the regulation window. PGOOD pin is asserted.
10	Not Supported	R	0b	Not supported and always set to 0.
9	OTHER	R	0b	0b: An OTHER fault has not occurred 1b: An OTHER fault has occurred, the host should check STATUS_OTHER for more information.
8	Not Supported	R	0b	Not supported and always set to 0.

Table 1-92. Register Field Descriptions (continued)

Bit	Field	Access	Reset	Description
7:0	STATUS BYTE	R	0	Identical to the STATUS_BYTE

All bits which may trigger SMBALERT have a corresponding bit in SMBALERT_MASK .

1.2.67 (7Ah) STATUS_VOUT

CMD Address	7Ah
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
Paged:	Yes
Phased:	No
NVM Back-up:	No
Updates:	On-the-fly

The STATUS_VOUT command returns one data byte with contents as follows. All supported bits may be cleared either by CLEAR_FAULTS , or individually by writing 1b to the (7Ah) STATUS_VOUT register in their position, per the PMBus 1.3.1 Part II specification section 10.2.4.

(7Ah) STATUS_VOUT Register Map

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	R	R
VOUT OVF	VOUT OVW	VOUT UVW	VOUT UVF	VOUT MINMAX	TON MAX	0	0

LEGEND: R/W = Read/Write; R = Read only

Table 1-93. Register Field Descriptions

Bit	Field	Access	Reset	Description
7	VOUT OVF	RW	0b	0b: Latched flag indicating VOUT OV fault has NOT occurred 1b: Latched flag indicating a VOUT OV fault has occurred Note: the mask bits for VOUT_ OVF will mask Fixed, tracking, and pre-biased OVP.
6	VOUT OVW	RW	0b	0b: Latched flag indicating VOUT OV warn has NOT occurred 1b: Latched flag indicating a VOUT OV warn has occurred Note: the mask bits for VOUT_OVF will mask Fixed, tracking, and pre-biased OVP
5	VOUT UVW	RW	0b	0b: Latched flag indicating VOUT UV warn has NOT occurred 1b: Latched flag indicating a VOUT UV warn has occurred
4	VOUT UVF	RW	0b	0b: Latched flag indicating VOUT UV fault has NOT occurred 1b: Latched flag indicating a VOUT UV fault has occurred
3	VOUT MINMAX	RW	0b	0b: Latched flag indicating a VOUT MINMAX has NOT occurred 1b: Latched flag indicating a VOUT MINMAX has occurred
2	TON MAX	RW	0b	0b: Latched flag indicating a TON MAX has NOT occurred 1b: Latched flag indicating a TON MAX has occurred
1:0	Not supported	R	0b	Not supported and always set to 0b

All bits which may trigger SMBALERT have a corresponding bit in SMBALERT_MASK.

1.2.68 (7Bh) STATUS_IOUT

CMD Address	7Bh
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
Paged:	Yes
Phased:	No
NVM Back-up:	No
Updates:	On-the-fly

The STATUS_IOUT command returns one data byte with contents as follows. All supported bits may be cleared either by CLEAR_FAULTS , or individually by writing 1b to the (7Bh) STATUS_IOUT register in their position, per the PMBus 1.3.1 Part II specification section 10.2.4.

(7Bh) STATUS_IOUT Register Map

7	6	5	4	3	2	1	0
RW	R	RW	R	RW	R	R	R
IOUT OCF	0	IOUT OCW	0	CUR SHAREF	0	0	0

LEGEND: R/W = Read/Write; R = Read only

Table 1-94. Register Field Descriptions

Bit	Field	Access	Reset	Description
7	IOUT OCF	RW	0b	0b: Latched flag indicating IOUT OC fault has NOT occurred 1b: Latched flag indicating IOUT OC fault has occurred
6	Not Supported	R	0b	Not supported and always set to 0b
5	IOUT OCW	RW	0b	0b: Latched flag indicating IOUT OC warn has NOT occurred 1b: Latched flag indicating IOUT OC warn has occurred
4	Not Supported	R	0b	Not supported and always set to 0b
3	CUR SHAREF	RW	0b	0b: Latched flag indicating current share fault has NOT occurred 1b: Latched flag indicating current share fault has occurred
2:0	Not Supported	RW	0b	Not supported and always set to 000b

All bits which may trigger SMBALERT have a corresponding bit in SMBALERT_MASK .

1.2.69 (7Ch) STATUS_INPUT

CMD Address	7Ch
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
Paged:	No.
Phased:	No
NVM Back-up:	No
Updates:	On-the-fly

The STATUS_INPUT command returns one data byte with contents as follows. All supported bits may be cleared either by CLEAR_FAULTS , or individually by writing 1b to the (7Ch) STATUS_INPUT register in their position, per the PMBus 1.3.1 Part II specification section 10.2.4.

(7Ch) STATUS_INPUT Register Map

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VIN OVF	VIN OVW	VIN UVW	VIN UVF	LOW VIN	IIN OCF	IIN OCW	PIN OPW

LEGEND: R/W = Read/Write; R = Read only

Table 1-95. Register Field Descriptions

Bit	Field	Access	Reset	Description
7	VIN OVF	RW	0b	0b: Latched flag indicating VIN OV fault has NOT occurred 1b: Latched flag indicating VIN OV fault has occurred
6	VIN OVW	RW	0b	0b: Latched flag indicating VIN OV warn has NOT occurred 1b: Latched flag indicating VIN OV warn has occurred
5	VIN UVW	RW	0b	0b: Latched flag indicating VIN UV warn has NOT occurred 1b: Latched flag indicating VIN UV warn has occurred
4	VIN UVF	RW	0b	0b: Latched flag indicating VIN UV fault has NOT occurred 1b: Latched flag indicating VIN UV fault has occurred
3	LOW VIN	RW	0b	0b: Latched flag indicating the unit was shutdown due to insufficient VIN 1b: Latched flag indicating the unit was shutdown due to insufficient VIN
2	IIN OCF	RW	0b	0b: Latched flag indicating Input OC fault has NOT occurred 1b: Latched flag indicating Input OC fault has occurred
1	IIN OCW	RW	0b	0b: Latched flag indicating Input OC warn has NOT occurred 1b: Latched flag indicating Input OC warn has occurred
0	PIN OPW	RW	0b	0b: Latched flag indicating Input OP warn has NOT occurred 1b: Latched flag indicating Input OP warn has occurred

All bits which may trigger SMBALERT have a corresponding bit in SMBALERT_MASK .

PAGE behavior

Note that (7Ch) STATUS_INPUT is a shared command, while the STATUS_BYTE is paged.

The corresponding bit STATUS_BYTE are always be an OR'ing of the supported bits in this command. When a fault condition in this command occurs, the corresponding bit in STATUS_BYTE is updated for both pages. In the same manner, if this byte is individually cleared (for example, by a write of 1 to a latched condition), it clears the corresponding bit pages STATUS_BYTE .

LOW VIN vs. VIN UVF

The LOW_VIN bit is an information only (does not assert SMBALERT) flag which indicates that the currently selected PAGE is not converting power because its input voltage is too low. LOW_VIN asserts initially at reset but does not assert SMBALERT until VIN > VIN_ON for the first time, regardless of its mask bit.

The VIN_UVF bit is a latched status bit, may assert SMBALERT if it is triggered to alert the host of an input voltage issue. VIN_UVF is masked until the first time the sensed input voltage exceeds the VIN_ON threshold for the first time.

Table 1-96. LOW_VIN vs. VIN_UVF

VIN > VIN_ON first time	VIN	VIN UVF Status bit	LOW VIN status bit
No	Less than VIN UV FAULT LIMIT and VIN ON	0	1
No	Greater than VIN UV FAULT LIMIT but less that VIN ON	0	1
Yes	Greater than VIN ON and VIN UV FAULT LIMIT	0	0
Yes	Greater than VIN UV FAULT LIMIT but less that VIN ON	0	0
Yes	Less than VIN UV FAULT LIMIT and VIN ON	1	1

1.2.70 (7Dh) STATUS_TEMPERATURE

CMD Address	7Dh
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
Paged:	Yes
Phased:	No
NVM Back-up:	No
Updates:	On-the-fly

The STATUS_TEMPERATURE command returns one data byte with contents as follows. All supported bits may be cleared either by CLEAR_FAULTS , or individually by writing 1b to the (7Dh) STATUS_TEMPERATURE register in their position, per the PMBus 1.3.1 Part II specification section 10.2.4.

(7Dh) STATUS_TEMPERATURE Register Map

7	6	5	4	3	2	1	0
RW	RW	R	R	R	R	R	R
OTF	OTW	0	0	0	0	0	0

LEGEND: R/W = Read/Write; R = Read only

Table 1-97. Register Field Descriptions

Bit	Field	Access	Reset	Description
7	OTF	RW	0b	0b: Latched flag indicating OT fault has NOT occurred 1b: Latched flag indicating OT fault has occurred
6	OTW	RW	0b	0b: Latched flag indicating OT warn has NOT occurred 1b: Latched flag indicating OT warn has occurred
5:0	Not supported	R	0d	Not supported and always set to 000000b

All bits which may trigger SMBALERT have a corresponding bit in SMBALERT_MASK .

1.2.71 (7Eh) STATUS_CML

CMD Address	7Eh
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
Paged:	No
Phased:	No
NVM Back-up:	No
Updates:	On-the-fly

The STATUS_CML command returns one data byte with contents relating to communications, logic, and memory as follows. All supported bits may be cleared either by CLEAR_FAULTS , or individually by writing 1b to the (7Eh) STATUS_CML register in their position, per the PMBus 1.3.1 Part II specification section 10.2.4.

(7Eh) STATUS_CML Register Map

7	6	5	4	3	2	1	0
RW	RW	RW	RW	R	R	RW	RW
IVC	IVD	PEC	MEM	0	0	COMM	CML_OTHER

LEGEND: R/W = Read/Write; R = Read only

Table 1-98. Register Field Descriptions

Bit	Field	Access	Reset	Description
7	IVC	RW	0b	0b: latched flag indicating invalid or unsupported command was NOT received 1b: latched flag indicating an invalid or unsupported command was received
6	IVD	RW	0b	0b: latched flag indicating invalid or unsupported data was NOT received 1b: latched flag indicating an invalid or unsupported data was received
5	PEC	RW	0b	0b: latched flag indicating NO packet error check has failed 1b: latched flag indicating a packet error check has failed
4	MEM	RW	0b	0b: latched flag indicating NO memory error was detected 1b: latched flag indicating a memory error was detected
3:2	Not supported	R	00b	Not supported and always set to 00b
1	COMM	RW	0b	0b: latched flag indicating NO communication error detected 1b: latched flag indicating communication error detected
0	CML_ OTHER	RW	0b	Other CML Fault. Note that the SMBALERT Mask bit for CML_ OTHER masks all of these sources at once. Sources include: • Attempt to write a read-only register • PMBus arbitration lost • Command aborted before finished • Master NACK block count for block command • Block command with not enough bytes • Block command with too many bytes • Master sent incorrect block size for block command • Attempt to write a write-protected command • Other errors not listed here 0b: latched flag indicating NO communication error detected 1b: latched flag indicating communication error detected

All bits which may trigger SMBALERT have a corresponding bit in SMBALERT_MASK .

PAGE behavior

Note that (7Eh) STATUS_CML is a shared command, while the STATUS_BYTE is paged.

The corresponding bit STATUS_BYTE are always be an OR'ing of the supported bits in this command. When a fault condition in this command occurs, the corresponding bit in STATUS_BYTE is updated for both pages. Likewise if this byte is individually cleared (e.g. by a write of 1 to a latched condition), it clears the corresponding bit pages STATUS_BYTE .

Status reporting for unsupported commands

Attempting to access the following commands will cause the STATUS_CML[7] bit to set: 3Ah, 3Bh, 3Ch, 3Dh, 3Eh, 3Fh, 4Dh, 4Eh, 67h, 6Ch, 6Dh, 6Eh, 6Fh, 70h, 71h, 72h, 73h, 74h, 75h, 76h, 77h, 81h, 82h, 83h, 84h, 85h, 90h, 91h, 92h, 93h, 9Ch, 9Eh, 9Fh, AFh, B0h, B6h, BCh, C0h, C1h, C2h, C3h, CAh, CBh, CCh, D9h, DEh, DFh, E1h, E2h, E6h, E7h, E8h, E9h, EAh, F4h, F9h, FFh

Attempting to access the following commands will cause the STATUS_CML[0] and STATUS_EXTENDED[41] bits to set:1Ah, 23h, 2Ah, 30h, 31h, 32h, 37h, 48h, 49h, 5Eh, 5Fh, 66h, 68h, 69h, 6Ah, 86h, 87h, 8Ah, 8Fh, 94h, 95h, A0h, A1h, A2h, A6h, A7h, A8h, A9h, AAh, ABh, ACh.

TPS536xx does allow access to several unpublished command codes which are not intended for customer use. Do not change the value of these commands unless instructed to do so by a TI representative.

1.2.72 (7Fh) STATUS_OTHER

CMD Address	7Fh
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
Paged:	No
Phased:	No
NVM Back-up:	No
Updates:	On-the-fly

The STATUS_OTHER command returns one data byte with information not specified in the other STATUS bytes.

(7Fh) STATUS_OTHER Register Map

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	RW
0	0	0	0	0	0	0	FIRS TO ALERT

LEGEND: R/W = Read/Write; R = Read only

Table 1-99. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:1	Reserved	R	0h	Reserved
0	FIRST TO ALERT	RW	0b	0b: latched flag indicating that this device was NOT the first to assert SMBALERT. This flag could indicate either that the SMBALERT signal is not asserted (or has since been cleared), or that it is asserted, but this device was not the first on the bus to assert it. 1b: latched flag indicating that this device was the first to assert SMBALERT.

PAGE behavior

Note that (7Fh) STATUS_OTHER is a shared command, while the STATUS_BYTE is paged.

The corresponding bit STATUS_BYTE are always be an OR'ing of the supported bits in this command. When a fault condition in this command occurs, the corresponding bit in STATUS_BYTE is updated for both pages. Similarly, if this byte is individually cleared (for example, by a write of 1 to a latched condition), it clears the corresponding bit pages STATUS_BYTE .

1.2.73 (80h) STATUS_MFR_SPECIFIC

CMD Address	80h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
Paged:	Yes
Phased:	No
NVM Back-up:	No
Updates:	On-the-fly

The STATUS_MFR_SPECIFIC command returns one data byte information about manufacturer-defined fault and warning conditions. All supported bits may be cleared either by CLEAR_FAULTS , or individually by writing 1b to the (80h) STATUS_MFR_SPECIFIC register in their position, per the PMBus 1.3.1 Part II specification section 10.2.4.

(80h) STATUS_MFR_SPECIFIC Register Map

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	R	R	RW
POR	MFR	VR SETTLED	PH ERR	0	0	0	PSFLT

LEGEND: R/W = Read/Write; R = Read only

Table 1-100. Register Field Descriptions

Bit	Field	Access	Reset	Description
7	POR	RW	0b	Power-on self-check failed (device will permanently latch off). 0b: Condition did NOT occur. 1b: Condition has occurred.
6	EXT	RW	0b	More information is available in the STATUS_EXTENDED block command. 0b: Condition did NOT occur. 1b: Condition has occurred.
5	VR SETTLED	RW	0b	The output voltage has settled to its new target. 0b: Condition did NOT occur. 1b: Condition has occurred.
4	PH ERR	RW	0b	More information is available in the STATUS_PHASES command. 0b: Condition did NOT occur. 1b: Condition has occurred.
3	RESET	RW	0b	A RESET# pin event has occurred. RESET# is a multi-function pin, and this bit will always be set to 0b when no RESET# pin is assigned. 0b: Condition did NOT occur. 1b: Condition has occurred.
2:0	Reserved	R	0b	Reserved.
0	PSFLT	RW	0b	0b: Power stage Fault (TAO_HIGH) has NOT occurred for the currently selected PAGE 1b: Power stage Fault (TAO_HIGH) has occurred for the currently selected PAGE

Per the PMBus Spec writing a 1 to any bit in a STATUS register shall clear that bit if it is set. All bits which may trigger SMBALERT have a corresponding bit in SMBALERT_MASK.

1.2.74 (88h) READ_VIN

CMD Address	88h
Write Transaction:	N/A
Read Transaction:	Read Word
Format:	SLINEAR11
Paged:	No
Phased:	No
NVM Back-up:	No

The READ_VIN command returns the sensed input voltage in volts.

(88h) READ_VIN Register Map

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
READ VIN EXP					READ VIN MAN		
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
READ VIN MAN							

LEGEND: R/W = Read/Write; R = Read only

Table 1-101. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:11	READ VIN EXP	RW	Current Status	Linear format two's complement exponent.
10:0	READ VIN MAN	RW	Current Status	Linear format two's complement mantissa.

Attempts to write read-only commands cause the CML OTHER fault condition, TPS536xx responds as follows:

- Set the CML bit in STATUS_BYTE
- Set the CML OTHER bit in STATUS_CML
- Notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

1.2.75 (89h) READ_IIN

CMD Address	89h
Write Transaction:	N/A
Read Transaction:	Read Word
Format:	SLINEAR11
Paged:	No
Phased:	No
NVM Back-up:	No

The READ_IIN command returns the input current in amperes.

The CALCIIN RD bit in MFR_SPECIFIC_ED (MISC_OPTIONS), allows TPS536xx to impute input current for systems which do not support shunt or DCR measurement, with a gain calibration factor in USER_DATA_13 (MFR_CALIBRATION_CONFIG) .

(89h) READ_IIN Register Map

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
READ IIN EXP					READ IIN MAN		
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
READ IIN MAN							

LEGEND: R/W = Read/Write; R = Read only

Table 1-102. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:11	READ IIN EXP	RW	Current Status	Linear format two's complement exponent.
10:0	READ IIN MAN	RW	Current Status	Linear format two's complement mantissa.

Attempts to write read-only commands cause the CML OTHER fault condition, TPS536xx responds as follows:

- Set the CML bit in STATUS_BYTE
- Set the CML OTHER bit in STATUS_CML
- Notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

1.2.76 (8Bh) READ_VOUT

CMD Address	8Bh
Write Transaction:	N/A
Read Transaction:	Read Word
Format:	ULINEAR16 Absolute
Paged:	Yes
Phased:	No
NVM Back-up:	No

The READ_VOUT command returns the actual, measured output voltage.

(8Bh) READ_VOUT Register Map

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
READ VOUT							
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
READ VOUT							

LEGEND: R/W = Read/Write; R = Read only

Table 1-103. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:0	READ VOUT	RW	Current Status	Output voltage reading, ULINEAR16 format

Attempts to write read-only commands cause the CML OTHER fault condition, TPS536xx responds as follows:

- Set the CML bit in STATUS_BYTE
- Set the CML OTHER bit in STATUS_CML
- Notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

PAGE behavior

When PAGE = 00h or FFh, READ_VOUT returns the measured output voltage of Channel A.

When PAGE = 01h, READ_VOUT returns the measured output voltage of Channel B/PAGE 1

1.2.77 (8Ch) READ_IOUT

CMD Address	8Ch
Write Transaction:	N/A
Read Transaction:	Read Word
Format:	SLINEAR11
Paged:	Yes
Phased:	Yes
NVM Back-up:	No

The READ_IOUT command returns the output current in amperes.

(8Ch) READ_IOUT Register Map

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
READ IOUT EXP					READ IOUT MAN		
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
READ IOUT MAN							

LEGEND: R/W = Read/Write; R = Read only

Table 1-104. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:11	READ IOUT EXP	RW	Current Status	Linear format two's complement exponent.
10:0	READ IOUT MAN	RW	Current Status	Linear format two's complement mantissa.

Attempts to write read-only commands cause the CML OTHER fault condition, TPS536xx responds as follows:

- Set the CML bit in STATUS_BYTE
- Set the CML OTHER bit in STATUS_CML
- Notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

PAGE and PHASE behavior

When PAGE = 00h or FFh, READ_IOUT returns current measurements related to Channel A. When PAGE = 01h, READ_IOUT returns current measurements related to Channel B.

When PHASE = FFh. READ_IOUT returns the total current for the controller at the current PAGE.

When PHASE != FFh, READ_IOUT returns the measured current of physical power stage assigned to the current PHASE by the PHASE CONFIG command. For example, if PAGE = 0, PHASE = 0, and PWM3 is assigned to PHASE 3 by PHASE_CONFIG, READ_IOUT [PAGE0][PHASE0] returns the power stage current for PWM3/CSP3.

1.2.78 (8Dh) READ_TEMPERATURE_1

CMD Address	8Dh
Write Transaction:	N/A
Read Transaction:	Read Word
Format:	SLINEAR11
Paged:	Yes
Phased:	No
NVM Back-up:	No

The READ_TEMPERATURE_1 command returns the maximum power stage temperature in degrees Celsius. READ_TEMPERATURE_1 and READ_TEMPERATURE_2 return the exact same data.

(8Eh) READ_TEMPERATURE_1 Register Map

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
READ T1 EXP					READ T1 MAN		
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
READ T1 MAN							

LEGEND: R/W = Read/Write; R = Read only

Table 1-105. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:11	READ T1 EXP	RW	Current Status	Linear format two's complement exponent. LSB = 1 degree Celsius
10:0	READ T1 MAN	RW	Current Status	Linear format two's complement mantissa.

Attempts to write read-only commands cause the CML OTHER fault condition, TPS536xx responds as follows:

- Set the CML bit in STATUS_BYTE
- Set the CML OTHER bit in STATUS_CML
- Notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

PAGE Behavior

When PAGE = 00h or FFh, READ_TEMPERATURE_1 returns the measured temperature on the ATSEN pin.
When PAGE = 01h, READ_TEMPERATURE_1 returns the measured temperature on the BTSEN pin.

1.2.79 (8Eh) READ_TEMPERATURE_2

CMD Address	8Eh
Write Transaction:	N/A
Read Transaction:	Read Word
Format:	SLINEAR11
Paged:	Yes
Phased:	No
NVM Back-up:	No

Note

READ_TEMPERATURE_2 is a shadow command for READ_TEMPERATURE_1. These commands return the same data.

The READ_TEMPERATURE_2 command returns the maximum power stage temperature in degrees Celsius.

(8Eh) READ_TEMPERATURE_2 Register Map

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
READ T2 EXP					READ T2 MAN		
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
READ T2 MAN							

LEGEND: R/W = Read/Write; R = Read only

Table 1-106. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:11	READ T2 EXP	RW	Current Status	Linear format two's complement exponent. LSB = 1 degree Celsius
10:0	READ T2 MAN	RW	Current Status	Linear format two's complement mantissa.

Attempts to write read-only commands cause the CML OTHER fault condition, TPS536xx responds as follows:

- Set the CML bit in STATUS_BYTE
- Set the CML OTHER bit in STATUS_CML
- Notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

PAGE Behavior

When PAGE = 00h or FFh, READ_TEMPERATURE_2 returns the measured temperature on the ATSEN pin.
When PAGE = 01h, READ_TEMPERATURE_2 returns the measured temperature on the BTSEN pin.

1.2.80 (96h) READ_POUT

CMD Address	96h
Write Transaction:	N/A
Read Transaction:	Read Word
Format:	SLINEAR11
Paged:	Yes
Phased:	No
NVM Back-up:	No

The READ_POUT command returns the calculated output power; the unit is watts.

(96h) READ_POUT Register Map

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
READ POUT EXP					READ POUT MAN		
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
READ POUT MAN							

LEGEND: R/W = Read/Write; R = Read only

Table 1-107. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:11	READ POUT EXP	RW	Current Status	Linear format two's complement exponent.
10:0	READ POUT MAN	RW	Current Status	Linear format two’s complement mantissa.

Attempts to write read-only commands cause the CML OTHER fault condition, TPS536xx responds as follows:

- Set the CML bit in STATUS_BYTE
- Set the CML OTHER bit in STATUS_CML
- Notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

1.2.81 (97h) READ_PIN

CMD Address	97h
Write Transaction:	N/A
Read Transaction:	Read Word
Format:	SLINEAR11
Paged:	No
Phased:	No
NVM Back-up:	No

The READ_PIN command returns the output power, in watts.

Based on the CALCIIN RD bit in MFR_SPECIFIC_ED (MISC_OPTIONS) , the calculated IIN value may also be forced to READ_IIN . When this bit is set, the READ_PIN value is calculated from calculated input current, instead of measured input current.

(97h) READ_PIN Register Map

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
READ PIN EXP					READ PIN MAN		
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
READ PIN MAN							

LEGEND: R/W = Read/Write; R = Read only

Table 1-108. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:11	READ PIN EXP	R	Current Status	Linear format two's complement exponent.
10:0	READ PIN MAN	R	Current Status	Linear format two's complement mantissa.

Attempts to write read-only commands cause the CML OTHER fault condition, TPS536xx responds as follows:

- Set the CML bit in STATUS_BYTE
- Set the CML OTHER bit in STATUS_CML
- Notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

1.2.82 (98h) PMBUS_REVISION

CMD Address	98h
Write Transaction:	N/A
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
Paged:	No
Phased:	No

The PMBUS_REVISION command reads the revision of the PMBus to which the device is compatible.

(98h) PMBUS_REVISION Register Map

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
PART I				PART II			

LEGEND: R/W = Read/Write; R = Read only

Table 1-109. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:4	PART I	R	0011b	0011b: Compatible with PMBus Rev 1.3, Part 1
3:0	PART II	R	0011b	0011b: Compatible with PMBus Rev 1.3, Part 2

Attempts to write read-only commands cause the CML_OTHER fault condition, TPS536xx responds as follows:

- Set the CML bit in STATUS_BYTE
- Set the CML_OTHER bit in STATUS_CML
- Notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

1.2.83 (99h) MFR_ID

CMD Address	99h
Write Transaction:	Write Block
Read Transaction:	Read Block
Format:	Unsigned Binary (3 bytes)
Paged:	No
Phased:	No
NVM Back-up:	EEPROM
Updates:	On-the-fly

The MFR_ID command loads the unit with text character that contains the manufacturer's ID. This is typically done once at the time of manufacture.

(99h) MFR_ID Register Map

23	22	21	20	19	18	17	16
RW	RW	RW	RW	RW	RW	RW	RW
MFR ID							
15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
MFR ID							
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
MFR ID							

LEGEND: R/W = Read/Write; R = Read only

Table 1-110. Register Field Descriptions

Bit	Field	Access	Reset	Description
23:0	MFR ID	RW	NVM	3 bytes of arbitrarily writable user-store NVM for manufactuer ID information.

1.2.84 (9Ah) MFR_MODEL

CMD Address	9Ah
Write Transaction:	Write Block
Read Transaction:	Read Block
Format:	Unsigned Binary (3 bytes)
Paged:	No
Phased:	No
NVM Back-up:	EEPROM
Updates:	On-the-fly

The MFR_MODEL command loads the unit with text character that contains the manufacturer model number. This is typically done once at the time of manufacture.

(9Ah) MFR_MODEL Register Map

23	22	21	20	19	18	17	16
RW	RW	RW	RW	RW	RW	RW	RW
MFR MODEL							
15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
MFR MODEL							
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
MFR MODEL							

LEGEND: R/W = Read/Write; R = Read only

Table 1-111. Register Field Descriptions

Bit	Field	Access	Reset	Description
23:0	MFR MODEL	RW	NVM	3 bytes of arbitrarily writable user-store NVM for manufactuer model identification.

1.2.85 (9Bh) MFR_REVISION

CMD Address	9Bh
Write Transaction:	Write Block
Read Transaction:	Read Block
Format:	Unsigned Binary (3 bytes)
Paged:	No
Phased:	No
NVM Back-up:	EEPROM
Updates:	On-the-fly

The MFR_REVISION command loads the unit with text character that contains the power supply manufacturer's revision number. This is typically done once at the time of manufacture.

(9Bh) MFR_REVISION Register Map

23	22	21	20	19	18	17	16
RW	RW	RW	RW	RW	RW	RW	RW
MFR REVISION							
15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
MFR REVISION							
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
MFR REVISION							

LEGEND: R/W = Read/Write; R = Read only

Table 1-112. Register Field Descriptions

Bit	Field	Access	Reset	Description
23:0	MFR REV	RW	NVM	3 bytes of arbitrarily writable user-store NVM for manufactuer revision information

1.2.86 (9Dh) MFR_DATE

CMD Address	9Dh
Write Transaction:	Write Block
Read Transaction:	Read Block
Format:	Unsigned Binary (3 bytes)
Paged:	No
Phased:	No
NVM Back-up:	EEPROM
Updates:	On-the-fly

The MFR_DATE command loads the unit with text character that contains the power supply manufacturing date. This is typically done once at the time of manufacture.

(9Dh) MFR_DATE Register Map

23	22	21	20	19	18	17	16
RW	RW	RW	RW	RW	RW	RW	RW
MFR DATE							
15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
MFR DATE							
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
MFR DATE							

LEGEND: R/W = Read/Write; R = Read only

Table 1-113. Register Field Descriptions

Bit	Field	Access	Reset	Description
23:0	MFR DATE	RW	NVM	3 bytes of arbitrarily writable user-store NVM for manufactuer date code information.

1.2.87 (ADh) IC_DEVICE_ID

CMD Address	ADh
Write Transaction:	N/A
Read Transaction:	Read Block
Format:	Unsigned Binary (6 bytes)
Paged:	No
Phased:	No

The IC_DEVICE_ID command is used to either set or read the type or part number of an IC embedded within a PMBus that is used for the PMBus interface.

(ADh) IC_DEVICE_ID Register Map

47	46	45	44	43	42	41	40
R	R	R	R	R	R	R	R
IC DEVICE ID							
39	38	37	36	35	34	33	32
R	R	R	R	R	R	R	R
IC DEVICE ID							
31	30	29	28	27	26	25	24
R	R	R	R	R	R	R	R
IC DEVICE ID							
23	22	21	20	19	18	17	16
R	R	R	R	R	R	R	R
IC DEVICE ID							
15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
IC DEVICE ID							
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
IC DEVICE ID							

LEGEND: R/W = Read/Write; R = Read only

Table 1-114. Register Field Descriptions

Bit	Field	Access	Reset	Description
47:0	IC DEVICE ID	RW	See description	IC_DEVICE_ID values are shown as they will appear in Fusion Digital Power Designer, LSB on the left / MSB on the right. E.g. Byte 0 = 54h, Byte 1 = 49h, etc... TPS536C7: 54 49 53 6C 70 00h TPS53676: 54 49 53 67 60 00 Note the digits 5449h are ASCII code for "TI"

Attempts to write read-only commands cause the CML_OTHER fault condition, TPS536xx responds as follows:

- Set the CML bit in STATUS_BYTE
- Set the CML_OTHER bit in STATUS_CML
- Notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3

1.2.88 (AEh) IC_DEVICE_REV

CMD Address	AEh
Write Transaction:	N/A
Read Transaction:	Read Block
Format:	Unsigned Binary (2 bytes)
Paged:	No
Phased:	No

The IC_DEVICE_REV command is used to return the revision of the IC.

(AEh) IC_DEVICE_REV Register Field Descriptions

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
IC DEVICE REV							
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
IC DEVICE REV							

LEGEND: R/W = Read/Write; R = Read only

Table 1-115. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:0	IC DEVICE REV	RW	Latest revision	TPS536xx device revision code. First device revision is 0000h.

Attempts to write read-only commands cause the CML OTHER fault condition, TPS536xx responds as follows:

- Set the CML bit in STATUS_BYTE
- Set the CML_OTHER bit in STATUS_CML

Notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3

1.2.89 (B1h) USER_DATA_01 (COMPENSATION_CONFIG)

CMD Address	B1h
Write Transaction:	Write Block
Read Transaction:	Read Block
Format:	Unsigned Binary (8 bytes)
Paged:	Yes
Phased:	No
NVM Back-up:	EEPROM
Updates:	On-the-fly

Configure the control loop compensation settings.

(B1h) USER_DATA_01 (COMPENSATION_CONFIG) Register Map

63	62	61	60	59	58	57	56
RW	RW	RW	RW	RW	RW	RW	RW
VOUT DROOP EXP					VOUT DROOP MAN		
55	54	53	52	51	50	49	48
RW	RW	RW	RW	RW	RW	RW	RW
VOUT DROOP MAN							
47	46	45	44	43	42	41	40
RW	RW	RW	RW	RW	RW	RW	RW
ACLL EXP					ACLL MAN		
39	38	37	36	35	34	33	32
RW	RW	RW	RW	RW	RW	RW	RW
ACLL MAN							
31	30	29	28	27	26	25	24
R	RW	RW	RW	RW	RW	RW	RW
0	DCM INT TC			DYN INT TC			
23	22	21	20	19	18	17	16
RW	RW	RW	RW	RW	RW	RW	R
INT TC				RAMP			0
15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
INT TC		AC GAIN		VDINT			
7	6	5	4	3	2	1	0
R	R	R	RW	R	R	R	R
0	0	0	GINT	0	0	0	0

LEGEND: R/W = Read/Write; R = Read only

Table 1-116. Register Field Descriptions

Bit	Field	Access	Reset	Description
63:48	VOUT DROOP	RW	NVM	Shadow register for VOUT DROOP. SLINEAR11 format. Updates to this field update the VOUT DROOP, and updates to VOUT DROOP update this field. Refer to the command description for VOUT DROOP for supported values.
47:32	ACLL	RW	NVM	AC load line setting in SLINEAR11 format. Refer to the table below for supported values. Reset exponent = -6.

Table 1-116. Register Field Descriptions (continued)

Bit	Field	Access	Reset	Description
31	Reserved	R	0b	Reserved
30:28	DCM INT TC	RW	NVM	Integrator time constant in DCM mode. See the table below.
27:24	DYN INT TC	RW	NVM	Dynamic integration time constant. See the table below.
23:20	INT TC	RW	NVM	Normal integration time constant. See the table below.
19:17	RAMP	RW	NVM	Ramp amplitude. See the table below.
15:14	INT GAIN	RW	NVM	Integration path gain. See the table below.
13:12	AC GAIN	RW	NVM	AC path gain. See the table below.
11:8	VDINT	RW	NVM	Dynamic integration voltage setting. See the table below.
7:5	Reserved	R	0b	Reserved
4	GINT	RW	NVM	Scaling factor for Static and Dynamic Integration Time Constant 0b: 1.0x DYN INT TC; 1.0x INT TC 1b: 6.0x DYN INT TC; 6.0x INT TC
3:0	Reserved	R	0b	Reserved

PAGE = FFh

When PAGE = FFh, all USER DATA commands are treated as if PAGE = 00h, meaning data received applies to PAGE =00h, and reads to this command reflect the data for PAGE =00h.

Table 1-117. AC load line settings

ACLL (decoded)	Effective AC load line (mΩ)	Nominal SLINEAR11 (hex)
0 mΩ ≤ ACLL < 0.0078125 mΩ	0	Do not use this setting
0.0078125 mΩ ≤ ACLL < 0.0234375 mΩ	0.0156	D001h
0.0234375 mΩ ≤ ACLL < 0.0390625 mΩ	0.0313	D002h
0.0390625 mΩ ≤ ACLL < 0.0546875 mΩ	0.0469	D003h
0.0546875 mΩ ≤ ACLL < 0.0703125 mΩ	0.0625	D004h
0.0703125 mΩ ≤ ACLL < 0.0859375 mΩ	0.0781	D005h
0.0859375 mΩ ≤ ACLL < 0.1015625 mΩ	0.0938	D006h
0.1015625 mΩ ≤ ACLL < 0.1171875 mΩ	0.1094	D007h
0.1171875 mΩ ≤ ACLL < 0.1328125 mΩ	0.125	D008h
0.1328125 mΩ ≤ ACLL < 0.1484375 mΩ	0.1406	D009h
0.1484375 mΩ ≤ ACLL < 0.1640625 mΩ	0.1563	D00Ah
0.1640625 mΩ ≤ ACLL < 0.1796875 mΩ	0.1719	D00Bh
0.1796875 mΩ ≤ ACLL < 0.1953125 mΩ	0.1875	D00Ch
0.1953125 mΩ ≤ ACLL < 0.2109375 mΩ	0.2031	D00Dh
0.2109375 mΩ ≤ ACLL < 0.2265625 mΩ	0.2188	D00Eh
0.2265625 mΩ ≤ ACLL < 0.2421875 mΩ	0.2344	D00Fh
0.2421875 mΩ ≤ ACLL < 0.2578125 mΩ	0.25	D010h
0.2578125 mΩ ≤ ACLL < 0.2734375 mΩ	0.2656	D011h
0.2734375 mΩ ≤ ACLL < 0.2890625 mΩ	0.2813	D012h
0.2890625 mΩ ≤ ACLL < 0.3046875 mΩ	0.2969	D013h
0.3046875 mΩ ≤ ACLL < 0.3203125 mΩ	0.3125	D014h
0.3203125 mΩ ≤ ACLL < 0.3359375 mΩ	0.3281	D015h
0.3359375 mΩ ≤ ACLL < 0.3515625 mΩ	0.3438	D016h
0.3515625 mΩ ≤ ACLL < 0.3671875 mΩ	0.3594	D017h
0.3671875 mΩ ≤ ACLL < 0.3828125 mΩ	0.375	D018h
0.3828125 mΩ ≤ ACLL < 0.3984375 mΩ	0.3906	D019h

Table 1-117. AC load line settings (continued)

ACLL (decoded)	Effective AC load line (mΩ)	Nominal SLINEAR11 (hex)
0.3984375 mΩ ≤ ACLL < 0.4140625 mΩ	0.4063	D01Ah
0.4140625 mΩ ≤ ACLL < 0.4296875 mΩ	0.4219	D01Bh
0.4296875 mΩ ≤ ACLL < 0.4453125 mΩ	0.4375	D01Ch
0.4453125 mΩ ≤ ACLL < 0.4609375 mΩ	0.4531	D01Dh
0.4609375 mΩ ≤ ACLL < 0.4765625 mΩ	0.4688	D01Eh
0.4765625 mΩ ≤ ACLL < 0.4921875 mΩ	0.4844	D01Fh
0.4921875 mΩ ≤ ACLL < 0.5078125 mΩ	0.5	D020h
0.5078125 mΩ ≤ ACLL < 0.5234375 mΩ	0.5156	D021h
0.5234375 mΩ ≤ ACLL < 0.5390625 mΩ	0.5313	D022h
0.5390625 mΩ ≤ ACLL < 0.5546875 mΩ	0.5469	D023h
0.5546875 mΩ ≤ ACLL < 0.5703125 mΩ	0.5625	D024h
0.5703125 mΩ ≤ ACLL < 0.5859375 mΩ	0.5781	D025h
0.5859375 mΩ ≤ ACLL < 0.6015625 mΩ	0.5938	D026h
0.6015625 mΩ ≤ ACLL < 0.6171875 mΩ	0.6094	D027h
0.6171875 mΩ ≤ ACLL < 0.6328125 mΩ	0.625	D028h
0.6328125 mΩ ≤ ACLL < 0.6484375 mΩ	0.6406	D029h
0.6484375 mΩ ≤ ACLL < 0.6640625 mΩ	0.6563	D02Ah
0.6640625 mΩ ≤ ACLL < 0.6796875 mΩ	0.6719	D02Bh
0.6796875 mΩ ≤ ACLL < 0.6953125 mΩ	0.6875	D02Ch
0.6953125 mΩ ≤ ACLL < 0.7109375 mΩ	0.7031	D02Dh
0.7109375 mΩ ≤ ACLL < 0.7265625 mΩ	0.7188	D02Eh
0.7265625 mΩ ≤ ACLL < 0.7421875 mΩ	0.7344	D02Fh
0.7421875 mΩ ≤ ACLL < 0.7578125 mΩ	0.75	D030h
0.7578125 mΩ ≤ ACLL < 0.7734375 mΩ	0.7656	D031h
0.7734375 mΩ ≤ ACLL < 0.7890625 mΩ	0.7813	D032h
0.7890625 mΩ ≤ ACLL < 0.8046875 mΩ	0.7969	D033h
0.8046875 mΩ ≤ ACLL < 0.8203125 mΩ	0.8125	D034h
0.8203125 mΩ ≤ ACLL < 0.8359375 mΩ	0.8281	D035h
0.8359375 mΩ ≤ ACLL < 0.8515625 mΩ	0.8438	D036h
0.8515625 mΩ ≤ ACLL < 0.8671875 mΩ	0.8594	D037h
0.8671875 mΩ ≤ ACLL < 0.8828125 mΩ	0.875	D038h
0.8828125 mΩ ≤ ACLL < 0.8984375 mΩ	0.8906	D039h
0.8984375 mΩ ≤ ACLL < 0.9140625 mΩ	0.9063	D03Ah
0.9140625 mΩ ≤ ACLL < 0.9296875 mΩ	0.9219	D03Bh
0.9296875 mΩ ≤ ACLL < 0.9453125 mΩ	0.9375	D03Ch
0.9453125 mΩ ≤ ACLL < 0.9609375 mΩ	0.9531	D03Dh
0.9609375 mΩ ≤ ACLL < 0.9765625 mΩ	0.9688	D03Eh
0.9765625 mΩ ≤ ACLL < 0.9921875 mΩ	0.9844	D03Fh
0.9921875 mΩ ≤ ACLL < 1.015625 mΩ	1	D040h
1.015625 mΩ ≤ ACLL < 1.046875 mΩ	1.0313	D042h
1.046875 mΩ ≤ ACLL < 1.078125 mΩ	1.0625	D044h
1.078125 mΩ ≤ ACLL < 1.109375 mΩ	1.0938	D046h
1.109375 mΩ ≤ ACLL < 1.140625 mΩ	1.125	D048h
1.140625 mΩ ≤ ACLL < 1.171875 mΩ	1.1563	D04Ah
1.171875 mΩ ≤ ACLL < 1.203125 mΩ	1.1875	D04Ch

Table 1-117. AC load line settings (continued)

ACLL (decoded)	Effective AC load line (mΩ)	Nominal SLINEAR11 (hex)
1.203125 mΩ ≤ ACLL < 1.234375 mΩ	1.2188	D04Eh
1.234375 mΩ ≤ ACLL < 1.265625 mΩ	1.25	D050h
1.265625 mΩ ≤ ACLL < 1.296875 mΩ	1.2813	D052h
1.296875 mΩ ≤ ACLL < 1.328125 mΩ	1.3125	D054h
1.328125 mΩ ≤ ACLL < 1.359375 mΩ	1.3438	D056h
1.359375 mΩ ≤ ACLL < 1.390625 mΩ	1.375	D058h
1.390625 mΩ ≤ ACLL < 1.421875 mΩ	1.4063	D05Ah
1.421875 mΩ ≤ ACLL < 1.453125 mΩ	1.4375	D05Ch
1.453125 mΩ ≤ ACLL < 1.484375 mΩ	1.4688	D05Eh
1.484375 mΩ ≤ ACLL < 1.515625 mΩ	1.5	D060h
1.515625 mΩ ≤ ACLL < 1.546875 mΩ	1.5313	D062h
1.546875 mΩ ≤ ACLL < 1.578125 mΩ	1.5625	D064h
1.578125 mΩ ≤ ACLL < 1.609375 mΩ	1.5938	D066h
1.609375 mΩ ≤ ACLL < 1.640625 mΩ	1.625	D068h
1.640625 mΩ ≤ ACLL < 1.671875 mΩ	1.6563	D06Ah
1.671875 mΩ ≤ ACLL < 1.703125 mΩ	1.6875	D06Ch
1.703125 mΩ ≤ ACLL < 1.734375 mΩ	1.7188	D06Eh
1.734375 mΩ ≤ ACLL < 1.765625 mΩ	1.75	D070h
1.765625 mΩ ≤ ACLL < 1.796875 mΩ	1.7813	D072h
1.796875 mΩ ≤ ACLL < 1.828125 mΩ	1.8125	D074h
1.828125 mΩ ≤ ACLL < 1.859375 mΩ	1.8438	D076h
1.859375 mΩ ≤ ACLL < 1.890625 mΩ	1.875	D078h
1.890625 mΩ ≤ ACLL < 1.921875 mΩ	1.9063	D07Ah
1.921875 mΩ ≤ ACLL < 1.953125 mΩ	1.9375	D07Ch
1.953125 mΩ ≤ ACLL < 1.984375 mΩ	1.9688	D07Eh
1.984375 mΩ ≤ ACLL < 2.03125 mΩ	2	D080h
2.03125 mΩ ≤ ACLL < 2.09375 mΩ	2.0625	D084h
2.09375 mΩ ≤ ACLL < 2.15625 mΩ	2.125	D088h
2.15625 mΩ ≤ ACLL < 2.21875 mΩ	2.1875	D08Ch
2.21875 mΩ ≤ ACLL < 2.28125 mΩ	2.25	D090h
2.28125 mΩ ≤ ACLL < 2.34375 mΩ	2.3125	D094h
2.34375 mΩ ≤ ACLL < 2.40625 mΩ	2.375	D098h
2.40625 mΩ ≤ ACLL < 2.46875 mΩ	2.4375	D09Ch
2.46875 mΩ ≤ ACLL < 2.53125 mΩ	2.5	D0A0h
2.53125 mΩ ≤ ACLL < 2.59375 mΩ	2.5625	D0A4h
2.59375 mΩ ≤ ACLL < 2.65625 mΩ	2.625	D0A8h
2.65625 mΩ ≤ ACLL < 2.71875 mΩ	2.6875	D0ACh
2.71875 mΩ ≤ ACLL < 2.78125 mΩ	2.75	D0B0h
2.78125 mΩ ≤ ACLL < 2.84375 mΩ	2.8125	D0B4h
2.84375 mΩ ≤ ACLL < 2.90625 mΩ	2.875	D0B8h
2.90625 mΩ ≤ ACLL < 2.96875 mΩ	2.9375	D0BCh
2.96875 mΩ ≤ ACLL < 3.03125 mΩ	3	D0C0h
3.03125 mΩ ≤ ACLL < 3.09375 mΩ	3.0625	D0C4h
3.09375 mΩ ≤ ACLL < 3.15625 mΩ	3.125	D0C8h
3.15625 mΩ ≤ ACLL < 3.21875 mΩ	3.1875	D0CCh

Table 1-117. AC load line settings (continued)

ACLL (decoded)	Effective AC load line (mΩ)	Nominal SLINEAR11 (hex)
3.21875 mΩ ≤ ACLL < 3.28125 mΩ	3.25	D0D0h
3.28125 mΩ ≤ ACLL < 3.34375 mΩ	3.3125	D0D4h
3.34375 mΩ ≤ ACLL < 3.40625 mΩ	3.375	D0D8h
3.40625 mΩ ≤ ACLL < 3.46875 mΩ	3.4375	D0DCh
3.46875 mΩ ≤ ACLL < 3.53125 mΩ	3.5	D0E0h
3.53125 mΩ ≤ ACLL < 3.59375 mΩ	3.5625	D0E4h
3.59375 mΩ ≤ ACLL < 3.65625 mΩ	3.625	D0E8h
3.65625 mΩ ≤ ACLL < 3.71875 mΩ	3.6875	D0ECh
3.71875 mΩ ≤ ACLL < 3.78125 mΩ	3.75	D0F0h
3.78125 mΩ ≤ ACLL < 3.84375 mΩ	3.8125	D0F4h
3.84375 mΩ ≤ ACLL < 3.90625 mΩ	3.875	D0F8h
3.90625 mΩ ≤ ACLL < 3.96875 mΩ	3.9375	D0FCh
3.96875 mΩ ≤ ACLL < 4.0625 mΩ	4	D100h
4.0625 mΩ ≤ ACLL < 4.1875 mΩ	4.125	D108h
4.1875 mΩ ≤ ACLL < 4.3125 mΩ	4.25	D110h
4.3125 mΩ ≤ ACLL < 4.4375 mΩ	4.375	D118h
4.4375 mΩ ≤ ACLL < 4.5625 mΩ	4.5	D120h
4.5625 mΩ ≤ ACLL < 4.6875 mΩ	4.625	D128h
4.6875 mΩ ≤ ACLL < 4.8125 mΩ	4.75	D130h
4.8125 mΩ ≤ ACLL < 4.9375 mΩ	4.875	D138h
4.9375 mΩ ≤ ACLL < 5.0625 mΩ	5	D140h
5.0625 mΩ ≤ ACLL < 5.1875 mΩ	5.125	D148h
5.1875 mΩ ≤ ACLL < 5.3125 mΩ	5.25	D150h
5.3125 mΩ ≤ ACLL < 5.4375 mΩ	5.375	D158h
5.4375 mΩ ≤ ACLL < 5.5625 mΩ	5.5	D160h
5.5625 mΩ ≤ ACLL < 5.6875 mΩ	5.625	D168h
5.6875 mΩ ≤ ACLL < 5.8125 mΩ	5.75	D170h
5.8125 mΩ ≤ ACLL < 5.9375 mΩ	5.875	D178h
5.9375 mΩ ≤ ACLL < 6.0625 mΩ	6	D180h
6.0625 mΩ ≤ ACLL < 6.1875 mΩ	6.125	D188h
6.1875 mΩ ≤ ACLL < 6.3125 mΩ	6.25	D190h
6.3125 mΩ ≤ ACLL < 6.4375 mΩ	6.375	D198h
6.4375 mΩ ≤ ACLL < 6.5625 mΩ	6.5	D1A0h
6.5625 mΩ ≤ ACLL < 6.6875 mΩ	6.625	D1A8h
6.6875 mΩ ≤ ACLL < 6.8125 mΩ	6.75	D1B0h
6.8125 mΩ ≤ ACLL < 6.9375 mΩ	6.875	D1B8h
6.9375 mΩ ≤ ACLL < 7.0625 mΩ	7	D1C0h
7.0625 mΩ ≤ ACLL < 7.1875 mΩ	7.125	D1C8h
7.1875 mΩ ≤ ACLL < 7.3125 mΩ	7.25	D1D0h
7.3125 mΩ ≤ ACLL < 7.4375 mΩ	7.375	D1D8h
7.4375 mΩ ≤ ACLL < 7.5625 mΩ	7.5	D1E0h
7.5625 mΩ ≤ ACLL < 7.6875 mΩ	7.625	D1E8h
7.6875 mΩ ≤ ACLL < 7.8125 mΩ	7.75	D1F0h
7.8125 mΩ ≤ ACLL < 7.9375 mΩ	7.875	D1F8h
7.9375 mΩ ≤ ACLL ≤ 8 mΩ	8	D200h

Table 1-117. AC load line settings (continued)

ACLL (decoded)	Effective AC load line (mΩ)	Nominal SLINEAR11 (hex)
ACLL > 8 mΩ	Invalid/unsupported	Invalid/unsupported

Table 1-118. Dynamic Integration Voltage Settings

VDINT	Dynamic Integration Voltage Setting (mV)
000b	60
001b	80
010b	100
011b	120
100b	140
101b	160
110b	180
111b	Disabled

Table 1-119. Integration time constant settings

INT TC, DYN INT TC, DCM INT TC	Integration time constant (µs)
0000b	1
0001b	2
0010b	3
0011b	4
0100b	5
0101b	6
0110b	7
0111b	8
1000b	9
1001b	10
1010b	11
1011b	12
1100b	13
1101b	14
1110b	15
1111b	16

Table 1-120. Integration and AC gain settings

INT GAIN AC GAIN	Gain setting (V/V)
00b	0.5
01b	1.0
10b	1.5
11b	2.0

Table 1-121. Ramp Settings

RAMP	Ramp Amplitude (mV)
000b	80
001b	120
010b	160
011b	200

Table 1-121. Ramp Settings (continued)

RAMP	Ramp Amplitude (mV)
100b	240
101b	280
110b	320
111b	360

1.2.90 (B2h) USER_DATA_02 (NONLINEAR_CONFIG)

CMD Address	B2h
Write Transaction:	Write Block
Read Transaction:	Read Block
Format:	Unsigned Binary (5 bytes)
Paged:	Yes
Phased:	No
NVM Back-up:	EEPROM
Updates:	On-the-fly

Configure the device behavior during severe load transient events which saturate the control loop.

(B2h) USER_DATA_02 (NONLINEAR_CONFIG) Register Map

39	38	37	36	35	34	33	32
RW	RW	R	RW	RW	RW	RW	RW
MINTON		0	USR2				
31	30	29	28	27	26	25	24
R	R	R	RW	RW	RW	RW	RW
0	0	0	TBLANK				
23	22	21	20	19	18	17	16
RW	RW	RW	RW	RW	RW	RW	RW
MINOFF				OSR			
15	14	13	12	11	10	9	8
RW	RW	R	RW	RW	RW	RW	RW
OCL INT		0	USR1				
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
OSR TRUNC	TI ONLY	OSRBB	TBB OSR			USR1 PH	

LEGEND: R/W = Read/Write; R = Read only

Table 1-122. Register Field Descriptions

Bit	Field	Access	Reset	Description
39:38	MINTON	RW	NVM	Select the controller minimum on-time. 00b: 30 ns 01b: 40 ns 10b: 50 ns 11b: 60 ns
37	Reserved	R	0	Reserved
36:32	USR2	RW	NVM	Undershoot reduction level 2 (USR2) threshold. See the table below.
31:29	Reserved	R	0	Reserved
28:24	TBLANK	RW	NVM	Select the leading edge blanking time. The units are 5 ns per LSB. Do not use settings below 20 ns nominal.
23:20	MINOFF	RW	NVM	Controller minimum off-time. See the table below.
19:16	OSR	RW	NVM	Overshoot reduction (OSR) threshold. See the table below.

Table 1-122. Register Field Descriptions (continued)

Bit	Field	Access	Reset	Description
15:14	OCL INT	RW	NVM	PAGE 0 only (setting applies to both channels) 00b, 01b: Loop integration continues during OCL conditions 10b: Open integration when ALL phases enter OCL, resume when ANY phase exits OCL. 11b: Open integration when ANY phases enter OCL, resume when ANY phase exits OCL.
13	Reserved	R	0	Reserved
12:8	USR1	RW	NVM	Undershoot reduction level 1 (USR1) threshold. See the table below.
7	OSR TRUNC	RW	NVM	0b: Pulse truncation is DISABLED during OSR 1b: Pulse truncation is ENABLED during OSR
6	TI ONLY	RW	NVM	TI only setting. Do not modify this field from the default value.
5	OSRBB	RW	NVM	0b: Body braking is DISABLED 1b: Body braking is ENABLED
4:2	TBB OSR	RW	NVM	OSR body braking time duration. See the table below. 000b: 0.4 µs 001b: 0.5 µs 010b: 0.6 µs 011b: 0.9 µs 100b: 1.0 µs 101b: 1.1 µs 110b: 1.9 µs 111b: 2.2 µs
1:0	USR1 PH	RW	NVM	Phases enabled during USR1. See the table below.

PAGE = FFh

When PAGE = FFh, all USER_DATA commands are treated as if PAGE = 00h, meaning data received applies to PAGE = 00h, and reads to this command reflect the data for PAGE = 00h.

Table 1-123. Overshoot reduction (OSR) thresholds

OSR	OSR threshold (mV)
0000b	20
0001b	30
0010b	40
0011b	50
0100b	60
0101b	70
0110b	80
0111b	90
1000b	100
1001b	110
1010b	120
1011b	130
1100b	140
1101b	150
1110b	160
1111b	OSR disabled

Table 1-124. Undershoot reduction level 2 (USR2) thresholds

USR2	USR2 threshold (mV)
00000b	15
00001b	17.5

Table 1-124. Undershoot reduction level 2 (USR2) thresholds (continued)

USR2	USR2 threshold (mV)
00010b	20
00011b	22.5
00100b	25
00101b	27.5
00110b	30
00111b	32.5
01000b	35
01001b	37.5
01010b	40
01011b	42.5
01100b	45
01101b	47.5
01110b	50
01111b	52.5
10000b	55
10001b	57.5
10010b	60
10011b	62.5
10100b	65
10101b	67.5
10110b	70
10111b	72.5
11000b	75
11001b	77.5
Others	Disabled

Table 1-125. Undershoot reduction level 1 (USR1) thresholds

USR1	USR1 threshold (mV)
00000b	Not recommended
00001b	Not recommended
00010b	15
00011b	17.5
00100b	20
00101b	22.5
00110b	25
00111b	27.5
01000b	30
01001b	32.5
01010b	35
01011b	37.5
01100b	40
01101b	42.5
01110b	45
01111b	47.5
10000b	50
10001b	52.5

Table 1-125. Undershoot reduction level 1 (USR1) thresholds (continued)

USR1	USR1 threshold (mV)
10010b	55
10011b	57.5
10100b	60
10101b	62.5
10110b	65
10111b	67.5
11000b	70
11001b	72.5
Others	Disabled

Table 1-126. Phases added by USR1

USR1_PH	Number of phases added by USR1
00b	3
01b	4
10b	5
11b	All phases

Table 1-127. Minimum off time setting

MINOFF	Minimum Off Time (ns)
0000b	30
0001b	45
0010b	60
0011b	75
0100b	90
0101b	105
0110b	120
0111b	135
Other	Reserved

1.2.91 (B3h) USER_DATA_03 (PHASE_CONFIG)

CMD Address	B3h
Write Transaction:	Write Block
Read Transaction:	Read Block
Format:	Unsigned Binary (24 bytes)
Paged:	No
Phased:	No
NVM Back-up:	EEPROM or pinstrap depending on MFR_SPECIFIC_EE (PIN_DETECT_OVERRIDE). NVM only for TPS53676.
Updates:	Updates not accepted with power conversion active.

Configure phase assignments: Assign phases to channels, phase number, and firing position. Note this register has pinstrapping available, and may be derived from either NVM or pinstrapping at boot-up depending on the configuration of MFR_SPECIFIC_EE (PIN_DETECT_OVERRIDE).

191	190	189	188	187	186	185	184
RW	RW	R	R	RW	RW	RW	RW
PH EN12	TI ONLY	0	0	PHASE12			
183	182	181	180	179	178	177	176
R	R	R	RW	RW	RW	RW	RW
0	0	0	PAGE12	ORDER12			
175	174	173	172	171	170	169	168
RW	RW	R	R	RW	RW	RW	RW
PH EN11	TI ONLY	0	0	PHASE11			
167	166	165	164	163	162	161	160
R	R	R	RW	RW	RW	RW	RW
0	0	0	PAGE11	ORDER11			
159	158	157	156	155	154	153	152
RW	RW	R	R	RW	RW	RW	RW
PH EN10	TI ONLY	0	0	PHASE10			
151	150	149	148	147	146	145	144
R	R	R	RW	RW	RW	RW	RW
0	0	0	PAGE10	ORDER10			
143	142	141	140	139	138	137	136
RW	RW	R	R	RW	RW	RW	RW
PH EN9	TI ONLY	0	0	PHASE9			
135	134	133	132	131	130	129	128
R	R	R	RW	RW	RW	RW	RW
0	0	0	PAGE9	ORDER9			
127	126	125	124	123	122	121	120
RW	RW	R	R	RW	RW	RW	RW
PH EN8	TI ONLY	0	0	PHASE8			
119	118	117	116	115	114	113	112
R	R	R	RW	RW	RW	RW	RW
0	0	0	PAGE8	ORDER8			

(B3h) USER DATA 03 (PHASE_CONFIG) Data Bytes Per Phase

111	110	109	108	107	106	105	104
RW	RW	R	R	RW	RW	RW	RW
PH EN7	TI ONLY	0	0	PHASE7			
103	102	101	100	99	98	97	96
R	R	R	RW	RW	RW	RW	RW
0	0	0	PAGE7	ORDER7			
95	94	93	92	91	90	89	88
RW	RW	R	R	RW	RW	RW	RW
PH EN6	TI ONLY	0	0	PHASE6			
87	86	85	84	83	82	81	80
R	R	R	RW	RW	RW	RW	RW
0	0	0	PAGE6	ORDER6			
79	78	77	76	75	74	73	72
RW	RW	R	R	RW	RW	RW	RW
PH EN5	TI ONLY	0	0	PHASE5			
71	70	69	68	67	66	65	64
R	R	R	RW	RW	RW	RW	RW
0	0	0	PAGE5	ORDER5			
63	62	61	60	59	58	57	56
RW	RW	R	R	RW	RW	RW	RW
PH EN4	TI ONLY	0	0	PHASE4			
55	54	53	52	51	50	49	48
R	R	R	RW	RW	RW	RW	RW
0	0	0	PAGE4	ORDER4			
47	46	45	44	43	42	41	40
RW	RW	R	R	RW	RW	RW	RW
PH EN3	TI ONLY	0	0	PHASE3			
39	38	37	36	35	34	33	32
R	R	R	RW	RW	RW	RW	RW
0	0	0	PAGE3	ORDER3			
31	30	29	28	27	26	25	24
RW	RW	R	R	RW	RW	RW	RW
PH EN2	TI ONLY	0	0	PHASE2			
23	22	21	20	19	18	17	16
R	R	R	RW	RW	RW	RW	RW
0	0	0	PAGE2	ORDER2			
15	14	13	12	11	10	9	8
RW	RW	R	R	RW	RW	RW	RW
PH EN1	TI ONLY	0	0	PHASE1			
7	6	5	4	3	2	1	0
R	R	R	RW	RW	RW	RW	RW

(B3h) USER DATA 03 (PHASE_CONFIG) Data Bytes Per Phase (continued)

0	0	0	PAGE1	ORDER1

LEGEND: R/W = Read/Write; R = Read only

Table 1-128. Register Field Descriptions

Bit	Field	Access	Reset	Description
191	PH EN12	RW	NVM	**Set this bit to 0b for TPS53676** Enable bit for the physical phase attached to pins 1 and 38. 0b: Phase is NOT enabled 1b: Phase is enabled
190	TI ONLY	RW	NVM	TI only bits. Do not modify this field from its default value.
189:188	Reserved	RW	0	Reserved. Set to 0
187:184	PHASE12	RW	Derived	**Don't care for TPS53676** PHASE assignment for the physical phase attached to pins 1 and 38. 0h = PHASE 0, ...
183:181	Reserved	RW	0	Reserved. Set to 0
180	PAGE12	RW	NVM	**Don't care for TPS53676** PAGE assignment for the physical phase attached to pins 1 and 38. 0b = Channel A 1b = Channel B
179:176	ORDER12	RW	NVM	**Don't care for TPS53676** Firing order assignment for the physical phase attached to pins 1 and 38. 0h = Order 0, ...
175	PH EN11	RW	NVM	**Set this bit to 0b for TPS53676** Enable bit for the physical phase attached to pins 2 and 37. 0b: Phase is NOT enabled 1b: Phase is enabled
174	TI ONLY	RW	NVM	TI only bits. Do not modify this field from its default value.
173:172	Reserved	RW	0	Reserved. Set to 0
171:168	PHASE11	RW	Derived	**Don't care for TPS53676** PHASE assignment for the physical phase attached to pins 2 and 37. 0h = PHASE 0, ...
167:165	Reserved	RW	0	Reserved. Set to 0
164	PAGE11	RW	NVM	**Don't care for TPS53676** PAGE assignment for the physical phase attached to pins 2 and 37. 0b = Channel A 1b = Channel B
163:160	ORDER11	RW	NVM	**Don't care for TPS53676** Firing order assignment for the physical phase attached to pins 2 and 37. 0h = Order 0, ...
159	PH EN10	RW	NVM	**Set this bit to 0b for TPS53676** Enable bit for the physical phase attached to pins 3 and 36. 0b: Phase is NOT enabled 1b: Phase is enabled
158	TI ONLY	RW	NVM	TI only bits. Do not modify this field from its default value.
157:156	Reserved	RW	0	Reserved. Set to 0
155:152	PHASE10	RW	Derived	**Don't care for TPS53676** PHASE assignment for the physical phase attached to pins 3 and 36. 0h = PHASE 0, ...
151:149	Reserved	RW	0	Reserved. Set to 0
148	PAGE10	RW	NVM	**Don't care for TPS53676** PAGE assignment for the physical phase attached to pins 3 and 36. 0b = Channel A 1b = Channel B

Table 1-128. Register Field Descriptions (continued)

Bit	Field	Access	Reset	Description
147:144	ORDER10	RW	NVM	**Don't care for TPS53676** Firing order assignment for the physical phase attached to pins 3 and 36. 0h = Order 0, ...
143	PH EN9	RW	NVM	**Set this bit to 0b for TPS53676** Enable bit for the physical phase attached to pins 4 and 35. 0b: Phase is NOT enabled 1b: Phase is enabled
142	TI ONLY	RW	NVM	TI only bits. Do not modify this field from its default value.
141:140	Reserved	RW	0	Reserved. Set to 0
139:136	PHASE9	RW	Derived	**Don't care for TPS53676** PHASE assignment for the physical phase attached to pins 4 and 35. 0h = PHASE 0, ...
135:133	Reserved	RW	0	Reserved. Set to 0
132	PAGE9	RW	NVM	**Don't care for TPS53676** PAGE assignment for the physical phase attached to pins 4 and 35. 0b = Channel A 1b = Channel B
131:128	ORDER9	RW	NVM	**Don't care for TPS53676** Firing order assignment for the physical phase attached to pins 4 and 35. 0h = Order 0, ...
127	PH EN8	RW	NVM	**Set this bit to 0b for TPS53676** Enable bit for the physical phase attached to pins 5 and 34. 0b: Phase is NOT enabled 1b: Phase is enabled
126	TI ONLY	RW	NVM	TI only bits. Do not modify this field from its default value.
125:124	Reserved	RW	0	Reserved. Set to 0
123:120	PHASE8	RW	Derived	**Don't care for TPS53676** PHASE assignment for the physical phase attached to pins 5 and 34. 0h = PHASE 0, ...
119:117	Reserved	RW	0	Reserved. Set to 0
116	PAGE8	RW	NVM	**Don't care for TPS53676** PAGE assignment for the physical phase attached to pins 5 and 34. 0b = Channel A 1b = Channel B
115:112	ORDER8	RW	NVM	Firing order assignment for the physical phase attached to pins 5 and 34. 0h = Order 0, ...
111	PH EN7	RW	NVM	Enable bit for the physical phase attached to pins 6 and 33. 0b: Phase is NOT enabled 1b: Phase is enabled
110	TI ONLY	RW	NVM	TI only bits. Do not modify this field from its default value.
109:108	Reserved	RW	0	Reserved. Set to 0
107:104	PHASE7	RW	Derived	PHASE assignment for the physical phase attached to pins 6 and 33. 0h = PHASE 0, ...
103:101	Reserved	RW	0	Reserved. Set to 0
100	PAGE7	RW	NVM	PAGE assignment for the physical phase attached to pins 6 and 33. 0b = Channel A 1b = Channel B
99:96	ORDER7	RW	NVM	Firing order assignment for the physical phase attached to pins 6 and 33. 0h = Order 0, ...
95	PH EN6	RW	NVM	Enable bit for the physical phase attached to pins 7 and 32. 0b: Phase is NOT enabled 1b: Phase is enabled
94	TI ONLY	RW	NVM	TI only bits. Do not modify this field from its default value.
93:92	Reserved	RW	0	Reserved. Set to 0

Table 1-128. Register Field Descriptions (continued)

Bit	Field	Access	Reset	Description
91:88	PHASE6	RW	Derived	PHASE assignment for the physical phase attached to pins 7 and 32. 0h = PHASE 0, ...
87:85	Reserved	RW	0	Reserved. Set to 0
84	PAGE6	RW	NVM	PAGE assignment for the physical phase attached to pins 7 and 32. 0b = Channel A 1b = Channel B
83:80	ORDER6	RW	NVM	Firing order assignment for the physical phase attached to pins 7 and 32. 0h = Order 0, ...
79	PH EN5	RW	NVM	Enable bit for the physical phase attached to pins 8 and 31. 0b: Phase is NOT enabled 1b: Phase is enabled
78	TI ONLY	RW	NVM	TI only bits. Do not modify this field from its default value.
77:76	Reserved	RW	0	Reserved. Set to 0
75:72	PHASE5	RW	Derived	PHASE assignment for the physical phase attached to pins 8 and 31. 0h = PHASE 0, ...
71:69	Reserved	RW	0	Reserved. Set to 0
68	PAGE5	RW	NVM	PAGE assignment for the physical phase attached to pins 8 and 31. 0b = Channel A 1b = Channel B
67:64	ORDER5	RW	NVM	Firing order assignment for the physical phase attached to pins 8 and 31. 0h = Order 0, ...
63	PH EN4	RW	NVM	Enable bit for the physical phase attached to pins 9 and 30. 0b: Phase is NOT enabled 1b: Phase is enabled
62	TI ONLY	RW	NVM	TI only bits. Do not modify this field from its default value.
61:60	Reserved	RW	0	Reserved. Set to 0
59:56	PHASE4	RW	Derived	PHASE assignment for the physical phase attached to pins 9 and 30. 0h = PHASE 0, ...
55:53	Reserved	RW	0	Reserved. Set to 0
52	PAGE4	RW	NVM	PAGE assignment for the physical phase attached to pins 9 and 30. 0b = Channel A 1b = Channel B
51:48	ORDER4	RW	NVM	Firing order assignment for the physical phase attached to pins 9 and 30. 0h = Order 0, ...
47	PH EN3	RW	NVM	Enable bit for the physical phase attached to pins 10 and 29. 0b: Phase is NOT enabled 1b: Phase is enabled
46	TI ONLY	RW	NVM	TI only bits. Do not modify this field from its default value.
45:44	Reserved	RW	0	Reserved. Set to 0
43:40	PHASE3	RW	Derived	PHASE assignment for the physical phase attached to pins 10 and 29. 0h = PHASE 0, ...
39:37	Reserved	RW	0	Reserved. Set to 0
36	PAGE3	RW	NVM	PAGE assignment for the physical phase attached to pins 10 and 29. 0b = Channel A 1b = Channel B
35:32	ORDER3	RW	NVM	Firing order assignment for the physical phase attached to pins 10 and 29. 0h = Order 0, ...
31	PH EN2	RW	NVM	Enable bit for the physical phase attached to pins 11 and 28. 0b: Phase is NOT enabled 1b: Phase is enabled
30	TI ONLY	RW	NVM	TI only bits. Do not modify this field from its default value.
29:28	Reserved	RW	0	Reserved. Set to 0

Table 1-128. Register Field Descriptions (continued)

Bit	Field	Access	Reset	Description
27:24	PHASE2	RW	Derived	PHASE assignment for the physical phase attached to pins 11 and 28. 0h = PHASE 0, ...
23:21	Reserved	RW	0	Reserved. Set to 0
20	PAGE2	RW	NVM	PAGE assignment for the physical phase attached to pins 11 and 28. 0b = Channel A 1b = Channel B
19:16	ORDER2	RW	NVM	Firing order assignment for the physical phase attached to pins 11 and 28. 0h = Order 0, ...
15	PH EN1	RW	NVM	Enable bit for the physical phase attached to pins 12 and 27. 0b: Phase is NOT enabled 1b: Phase is enabled
14	TI ONLY	RW	NVM	TI only bits. Do not modify this field from its default value.
13:12	Reserved	RW	0	Reserved. Set to 0
11:8	PHASE1	RW	Derived	PHASE assignment for the physical phase attached to pins 12 and 27. 0h = PHASE 0, ...
7:5	Reserved	RW	0	Reserved. Set to 0
4	PAGE1	RW	NVM	PAGE assignment for the physical phase attached to pins 12 and 27. 0b = Channel A 1b = Channel B
3:0	ORDER1	RW	NVM	Firing order assignment for the physical phase attached to pins 12 and 27. 0h = Order 0, ...

WARNING

There are several restrictions to phase configuration. The user must make ensure that all conditions below are met in the data words sent to this command in order for TPS536xx to behave properly. Refer to the examples below.

Data Validity:

- Channel A must have less than or equal to 12 phases for TPS536C7 or 7 phases for TPS53676; channel B must have less than or equal to 6 phases for TPS536C7 or 3 phases for TPS53676.
- The number of phases assigned to either channel A or channel B must be fewer than 12 phases for TPS536C7 or 7 phases for TPS53676.
- For one channel systems, use channel A. It is permissible to have no phases assigned to channel B or no phases assigned to channel B being enabled.
- Within each channel, the firing order assignments must start at zero, be continuous (do not skip order assignments), and be unique (do not assign multiple phases to the same fire order).
- Phase assignments for channel A must start at zero and count upward monotonically for each enabled phase starting from APWM1, APWM2, ... Phase assignments for channel B must start at zero and count downward monotonically starting from APWM12/BPWM1, APWM11/BPWM2, ...

Table 1-129. Example #1: 8+2 (TPS536C7 example)

Physical Phase	Enable	Page	Phase	Order
Pins 12, 27 (APWM1)	1	0	0	0
Pins 11, 28 (APWM2)	1	0	1	2
Pins 10, 29 (APWM3)	1	0	2	4
Pins 9, 30 (APWM4)	1	0	3	6
Pins 8, 31 (APWM5)	1	0	4	1
Pins 7, 32 (APWM6)	1	0	5	3
Pins 6, 33 (APWM7/ BPWM6)	1	0	6	5

Table 1-129. Example #1: 8+2 (TPS536C7 example) (continued)

Physical Phase	Enable	Page	Phase	Order
Pins 5, 34 (APWM8/ BPWM5)	1	0	7	7
Pins 4, 35 (APWM9/ BPWM4)	0	x	x	x
Pins 3, 36 (APWM10/ BPWM3)	0	x	x	x
Pins 2, 37 (APWM11/ BPWM2)	1	1	1	1
Pins 1, 37 (APWM12/ BPWM1)	1	1	0	0

Table 1-130. Example #2: 4+1 (TPS53676 example)

Physical Phase	Enable	Page	Phase	Order
Pins 12, 27 (APWM1)	1	0	0	0
Pins 11, 28 (APWM2)	1	0	1	1
Pins 10, 29 (APWM3)	1	0	2	2
Pins 9, 30 (APWM4)	1	0	3	3
Pins 8, 31 (APWM5 / BPWM3)	0	x	x	x
Pins 7, 32 (APWM6 / BPWM2)	0	x	x	x
Pins 6, 33 (APWM7 / BPWM1)	1	1	0	0
Pins 5, 34 (NC)	0	x	x	x
Pins 4, 35 (NC)	0	x	x	x
Pins 3, 36 (NC)	0	x	x	x
Pins 2, 37 (NC)	0	x	x	x
Pins 1, 37 (NC)	0	x	x	x

In the event the requested configuration is invalid, the TPS536xx responds as follows:

- Reject the update to USER_DATA_03 (PHASE_CONFIG) and NACK the last data byte
- Set the MFR bit in STATUS_WORD
- Set the EXT bit in STATUS_MFR_SPECIFIC
- Set the NO UPDATE bit in MFR_SPECIFIC_DD (STATUS_EXTENDED)
- Notify the host per PMBus 1.3.1 Part II specification, section 10.2.

During power conversion the USER_DATA_03 (PHASE_CONFIG) command may not be changed. Attempts to update USER_DATA_03 (PHASE_CONFIG) during regulation triggers the NO UPDATE fault condition. This trigger causes the TPS536xx to:

- Reject the update to USER_DATA_03 (PHASE_CONFIG) and NACK the last data byte
- Set the CML and MFR bits in STATUS_WORD
- Set the CML OTHER bit in STATUS_CML
- Set the EXT bit in STATUS_MFR_SPECIFIC
- Set the NO_UPDATE bit in MFR_SPECIFIC_DD (STATUS_EXTENDED)
- Notify the host per PMBus 1.3.1 Part II specification, section 10.2.

1.2.92 (B4h) USER_DATA_04 (DVID_CONFIG)

CMD Address	B4h
Write Transaction:	Write Block
Read Transaction:	Read Block
Format:	Unsigned Binary (6 bytes)
Paged:	Yes
Phased:	No
NVM Back-up:	EEPROM
Updates:	on-the-fly

Configure dynamic options relating to output voltage slewing

(B4h) USER DATA 04 (DVID CONFIG) Register Map

47	46	45	44	43	42	41	40
R	R	R	RW	RW	RW	RW	RW
0	0	0	DCLL DACDWN				
39	38	37	36	35	34	33	32
R	R	R	RW	RW	RW	RW	RW
0	0	0	DCLL DACUP				
31	30	29	28	27	26	25	24
RW	RW	R	R	RW	RW	RW	RW
DACWN DLY		0	0	ACLL DACDWN			
23	22	21	20	19	18	17	16
RW	RW	R	R	RW	RW	RW	RW
DACUP DLY		0	0	ACLL DACUP			
15	14	13	12	11	10	9	8
R	RW	RW	R	RW	RW	RW	RW
0	DAC0V DET	BUMP RED	0	OFS DACUP		OFS DACDWN	
7	6	5	4	3	2	1	0
R	R	R	R	R	R	RW	RW
0	0	0	0	0	0	OFS WAKE	

LEGEND: R/W = Read/Write; R = Read only

Table 1-131. Register Field Descriptions

Bit	Field	Access	Reset	Description
47:45	Reserved	R	0b	Reserved
44:40	DCLL DACDWN	RW	NVM	DC Loadline during downward moving DAC transitions.
39:37	Reserved	R	0b	Reserved
36:32	DCLL DACUP	RW	NVM	DC Loadline during upward moving DAC transitions.
31:30	DACDWN DLY	RW	NVM	DAC Down Recovery Delay. See the table below
29:28	Reserved	R	0b	Reserved
27:24	ACLL DACDWN	RW	NVM	AC Loadline during downward moving DAC transitions.
23:22	DACUP DLY	RW	NVM	DAC UP Recovery Delay. See the table below

Table 1-131. Register Field Descriptions (continued)

Bit	Field	Access	Reset	Description
19:16	ACLL DACUP	RW	NVM	AC Loadline during upward moving DAC transitions.
15	Reserved	R	0b	Reserved
14	DAC 0V DET	RW	NVM	0b: DAC ramps to 0V during soft-off or DVID down to zero 1b: Tri-state PWMs when DAC reaches 100-mV during soft-off or DVID down to zero. Intended to prevent negative excursion on output voltage.
13	BUMP RED	RW	NVM	0b: DISABLE soft-start bump reduction feature. 1b: ENABLE soft-start bump reduction feature. Enable fast PWM tri-state if output voltage exceeds DAC during soft-start.
12	Reserved	R	0b	Reserved
11:10	OFS DACUP	RW	NVM	DAC Offset during upward moving DAC transitions. See the table below.
9:8	OFS DACDWN	RW	NVM	DAC Offset during downward moving DAC transitions. See the table below.
7:2	Reserved	R	0b	Reserved
1:0	OFS WAKE	RW	NVM	DAC Offset during startup. See the table below.

PAGE = FFh

When PAGE = FFh, all USER DATA commands are treated as if PAGE = 0x00, meaning data received applies to PAGE =0x00, and reads to this command reflect the data for PAGE =0x00.

Table 1-132. DAC UP + DAC DOWN Offset Values

OFS DACUP, OFS DACDOWN	VID Offset (mV)
00b	0
01b	10
10b	20
11b	30

Table 1-133. Dynamic DCLL Settings (DCLL DACUP/ DCLL DACDWN)

DCLL DACDWN, DCLL DACUP (dec)	VOUT DROOP 0 to 1 mΩ	VOUT DROOP 1 to 2 mΩ	VOUT DROOP 2 to 4 mΩ	VOUT DROOP 4 to 8 mΩ
0	0.00000	0.00000	0.00000	0.00000
1	0.03125	0.06250	0.12500	0.25000
2	0.06250	0.12500	0.25000	0.50000
3	0.09375	0.18750	0.37500	0.75000
4	0.12500	0.25000	0.50000	1.00000
5	0.15625	0.31250	0.62500	1.25000
6	0.18750	0.37500	0.75000	1.50000
7	0.21875	0.43750	0.87500	1.75000
8	0.25000	0.50000	1.00000	2.00000
9	0.28125	0.56250	1.12500	2.25000
10	0.31250	0.62500	1.25000	2.50000
11	0.34375	0.68750	1.37500	2.75000
12	0.37500	0.75000	1.50000	3.00000
13	0.40625	0.81250	1.62500	3.25000
14	0.43750	0.87500	1.75000	3.50000
15	0.46875	0.93750	1.87500	3.75000
16	0.50000	1.00000	2.00000	4.00000

Table 1-133. Dynamic DCLL Settings (DCLL DACUP/ DCLL DACDWN) (continued)

DCLL DACDWN, DCLL DACUP (dec)	VOUT DROOP 0 to 1 mΩ	VOUT DROOP 1 to 2 mΩ	VOUT DROOP 2 to 4 mΩ	VOUT DROOP 4 to 8 mΩ
17	0.53125	1.06250	2.12500	4.25000
18	0.56250	1.12500	2.25000	4.50000
19	0.59375	1.18750	2.37500	4.75000
20	0.62500	1.25000	2.50000	5.00000
21	0.65625	1.31250	2.62500	5.25000
22	0.68750	1.37500	2.75000	5.50000
23	0.71875	1.43750	2.87500	5.75000
24	0.75000	1.50000	3.00000	6.00000
25	0.78125	1.56250	3.12500	6.25000
26	0.81250	1.62500	3.25000	6.50000
27	0.84375	1.68750	3.37500	6.75000
28	0.87500	1.75000	3.50000	7.00000
29	0.90625	1.81250	3.62500	7.25000
30	0.93750	1.87500	3.75000	7.50000
31	0.96875	1.93750	3.87500	7.75000

Table 1-134. Dynamic ACLL Settings

ACLL DACDWN, ACLL DACUP (dec)	ACLL 0 to 1 mΩ	ACLL 1 to 2 mΩ	ACLL 2 to 4 mΩ	ACLL 4 to 8 mΩ
0	0.00000	0.00000	0.00000	0.00000
1	0.06250	0.12500	0.25000	0.50000
2	0.12500	0.25000	0.50000	1.00000
3	0.18750	0.37500	0.75000	1.50000
4	0.25000	0.50000	1.00000	2.00000
5	0.31250	0.62500	1.25000	2.50000
6	0.37500	0.75000	1.50000	3.00000
7	0.43750	0.87500	1.75000	3.50000
8	0.50000	1.00000	2.00000	4.00000
9	0.56250	1.12500	2.25000	4.50000
10	0.62500	1.25000	2.50000	5.00000
11	0.68750	1.37500	2.75000	5.50000
12	0.75000	1.50000	3.00000	6.00000
13	0.81250	1.62500	3.25000	6.50000
14	0.87500	1.75000	3.50000	7.00000
15	0.93750	1.87500	3.75000	7.50000

Table 1-135. DAC Up Recovery Delay

DACUP DLY	DAC Up Recovery Delay (PWM1 cycles)
00b	1
01b	2
10b	4
11b	8

Table 1-136. DAC Down Recovery Delay

DACDWN DLY	DAC Down Recovery Delay (PWM1 cycles)
00b	1

Table 1-136. DAC Down Recovery Delay (continued)

DACDWN DLY	DAC Down Recovery Delay (PWM1 cycles)
01b	2
10b	4
11b	8

Table 1-137. VID offset during Soft-Start (OFS WAKE)

OFS WAKE	VID offset during Soft-Start (mV)
00b	0
01b	30
10b	60
11b	90

1.2.93 (B7h) USER_DATA_07 (PHASE_SHED_CONFIG)

CMD Address	B7h
Write Transaction:	Write Block
Read Transaction:	Read Block
Format:	Unsigned Binary (13 bytes)
Paged:	Yes
Phased:	No
NVM Back-up:	EEPROM
Updates:	on-the-fly

USER_DATA_07 (PHASE_SHED_CONFIG) provides a block for programming the currents of dynamic phase-adding or phase dropping.

103	102	101	100	99	98	97	96
RW	RW	RW	RW	RW	RW	RW	RW
DPA HYST11				DPA HYST12			
95	94	93	92	91	90	89	88
RW	RW	RW	RW	RW	RW	RW	RW
DPA HYST9				DPA HYST10			
87	86	85	84	83	82	81	80
RW	RW	RW	RW	RW	RW	RW	RW
DPA HYST7				DPA HYST8			
79	78	77	76	75	74	73	72
RW	RW	RW	RW	RW	RW	RW	RW
DPA HYST5				DPA HYST6			
71	70	69	68	67	66	65	64
RW	RW	RW	RW	RW	RW	RW	RW
DPA HYST3				DPA HYST4			
63	62	61	60	59	58	57	56
RW	RW	RW	RW	RW	RW	RW	8
TI ONLY				DPA HYST2			
55	54	53	52	51	50	49	48
R	R	RW	RW	RW	RW	RW	RW
PH ADD11				PH ADD12			
47	46	45	44	43	42	41	40
RW	RW	RW	RW	RW	RW	RW	RW
PH ADD9				PH ADD10			
39	38	37	36	35	34	33	32
RW	RW	RW	RW	RW	RW	RW	RW
PH ADD7				PH ADD8			
31	30	29	28	27	26	25	24
RW	RW	RW	RW	RW	RW	RW	RW
PH ADD5				PH ADD6			
23	22	21	20	19	18	17	16

RW	RW	RW	RW	RW	RW	RW	RW
PH ADD3				PH ADD4			

(B7h) USER_DATA_07 (PHASE_SHED_CONFIG) Register Map

15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
DPS HYST				PH ADD2			
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
TDPS FIL		START PH		MIN PH		0	DPS EN

LEGEND: R/W = Read/Write; R = Read only

Table 1-138. Register Field Descriptions

Bit	Field	Access	Reset	Description
103:100	DPA HYST11	RW	NVM	**Not meaningful for TPS53676** 11th Phase Add hysteresis. LSB = 1A
99:96	DPA HYST12	RW	NVM	**Not meaningful for TPS53676** 12th Phase Add hysteresis. LSB = 1A
95:92	DPA HYST9	RW	NVM	**Not meaningful for TPS53676** 9th Phase Add hysteresis. LSB = 1A
91:88	DPA HYST10	RW	NVM	**Not meaningful for TPS53676** 10h Phase Add hysteresis. LSB = 1A
87:84	DPA HYST7	RW	NVM	7th Phase Add/ hysteresis. LSB = 1A
83:80	DPA HYST8	RW	NVM	**Not meaningful for TPS53676** 8th Phase Add hysteresis. LSB = 1A
79:76	DPA HYST5	RW	NVM	5th Phase Add hysteresis. LSB = 1A
75:72	DPA HYST6	RW	NVM	6th Phase Add hysteresis. LSB = 1A
71:68	DPA HYST3	RW	NVM	3rd Phase Add hysteresis. LSB = 1A
67:64	DPA HYST4	RW	NVM	4th Phase Add hysteresis. LSB = 1A
63:60	TI ONLY	RW	NVM	TI only configuration bits. Do not change the value of this field.
59:56	DPA HYST2	RW	NVM	2nd Phase Add hysteresis. LSB = 1A
55:52	PH ADD11	RW	NVM	**Not meaningful for TPS53676** 11th Phase add threshold. See the table below.
51:48	PH ADD12	RW	NVM	**Not meaningful for TPS53676** 12th Phase add threshold. See the table below.
47:44	PH ADD9	RW	NVM	**Not meaningful for TPS53676** 9th Phase add threshold. See the table below.
43:40	PH ADD10	RW	NVM	**Not meaningful for TPS53676** 10th Phase add threshold. See the table below.
39:36	PH ADD7	RW	NVM	7th Phase add threshold. See the table below.
35:32	PH ADD8	RW	NVM	**Not meaningful for TPS53676** 8th Phase add threshold. See the table below.
31:28	PH ADD5	RW	NVM	5th Phase add threshold. See the table below.
27:24	PH ADD6	RW	NVM	6th Phase add threshold. See the table below.
23:20	PH ADD3	RW	NVM	3rd Phase add threshold. See the table below.
19:16	PH ADD4	RW	NVM	4th Phase add threshold. See the table below.
15:14	DPS HYST	RW	NVM	DPS Hysteresis 00b: 0A (not recommended) 01b: 1A 10b: 2A 11b: 3A

Table 1-138. Register Field Descriptions (continued)

Bit	Field	Access	Reset	Description
13:12	ZC TH	RW	NVM	Phase current zero-crossing thresholds (when DCM is enabled) by MIN PH 00b: 2 A 01b: 3 A 10b: 4 A 11b:5 A
11:8	PH ADD2	RW	NVM	2nd Phase add threshold. See the table below.
7:6	TDPS FIL	RW	NVM	DPS filter time constant for phase adding. See the table below.
5:4	START PH	RW	NVM	Active phases during startup 00b: 4 01b: 6 phases 10b: 8 phases (not valid for TPS53676) 11b: All available phases (based on PHASE CONFIG)
3:2	MIN PH	RW	NVM	Minimum number of phases, during DPS operation. See the table below.
1	Reserved	R	0	Reserved
0	DPS EN	RW	NVM	0b: Phase shedding is DISABLED for the current PAGE 1b: Phase shedding is ENABLED for the current PAGE

PAGE = FFh

When PAGE = FFh, all USER DATA commands are treated as if PAGE = 0x00, meaning data received applies to PAGE =0x00, and reads to this command reflect the data for PAGE =0x00.

Table 1-139. Phase Add Thresholds (Amperes)

Code	PH ADD2	PH ADD3	PH ADD4	PH ADD5	PH ADD6	PH ADD7	PH ADD8	PH ADD9	PH ADD10	PH ADD11	PH ADD12
0000b	12	30	46	62	78	105	145	188	225	265	305
0001b	13	32	48	64	81	110	150	194	230	270	310
0010b	14	34	50	66	84	115	155	200	235	275	315
0011b	15	36	52	68	87	120	160	206	240	280	320
0100b	16	38	54	70	90	125	165	212	245	285	325
0101b	17	40	56	72	93	130	170	218	250	290	330
0110b	18	42	58	74	96	135	175	224	255	295	335
0111b	19	44	60	76	99	140	180	230	260	300	340
1000b	20	50	80	90	110	160	220	250	280	320	360
1001b	21	60	100	100	120	180	240	270	300	340	380
1010b	22	70	120	110	130	200	260	290	340	360	420
1011b	23	80	140	120	140	220	280	330	380	400	440
1100b	24	90	160	140	160	240	340	370	420	440	480
1101b	25	100	180	160	180	280	380	410	460	480	520
1110b	26	110	200	180	200	320	420	450	500	520	560
1111b	27	120	220	200	220	360	460	490	540	560	600

Table 1-140. Minimum Number of Phases

MIN PH	Minimum number of phases
00b	1 Phase
01b	2 Phases
10b	4 Phases
11b (not valid for TPS53676)	8 Phases

Table 1-141. DPS Phase add filter time constant

MIN PH	DPS Filter time constant (µs)
00b	0.5
01b	1.0
10b	1.5
11b	2.0

1.2.94 (B8h) USER_DATA_08 (AVSBUS_CONFIG)

CMD Address	B8h
Write Transaction:	Write Block
Read Transaction:	Read Block
Format:	Unsigned Binary (1 byte)
Paged:	No
Phased:	No
NVM Back-up:	EEPROM
Updates:	Updates take effect only after NVM store and power cycle

Configure options related to the AVSBus Interface. **This command is not meaningful for TPS536C7.**

(B8h) USER_DATA_08 (AVSBUS_CONFIG) Register Map

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	RW
0	0	0	0	0	0	0	3 WIRE

LEGEND: R/W = Read/Write; R = Read only

Table 1-142. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:1	Reserved	R	0	Reserved
0	3 WIRE	RW	NVM	0b: AVSBus interface is configured for 2 Wire mode 1b: AVSBus interface is configured for 3 Wire mode

1.2.95 (BAh) USER_DATA_10 (ISHARE_CONFIG)

CMD Address	BAh
Write Transaction:	Write Block
Read Transaction:	Read Block
Format:	Unsigned Binary (1 byte)
Paged:	Yes
Phased:	Yes
NVM Back-up:	EEPROM
Updates:	on-the-fly

USER_DATA_10 (ISHARE_CONFIG) allows the user to adjust the ISHARE loop to adjust current balancing. USER_DATA_10 (ISHARE_CONFIG) is a phased command to allow assignment of ISHARE gain to individual phases in the controller.

(BAh) USER_DATA_10 (ISHARE_CONFIG) Register Map

7	6	5	4	3	2	1	0
R	RW	RW	R	RW	RW	RW	RW
0	TI ONLY		0	TSHARE GAIN			

LEGEND: R/W = Read/Write; R = Read only

Table 1-143. Register Field Descriptions

Bit	Field	Access	Reset	Description
7	Reserved	R	0	Reserved
6:5	TI ONLY	RW	NVM	TI only configuration bits. Do not change the value of this field.
4	Reserved	R	0	Reserved
3:0	TSHARE GAIN	RW	NVM	Sets the thermal sharing gain for the current phase. See the table below.

Table 1-144. Thermal Share Settings

TSHARE GAIN	Thermal Balance Gain K_T
0000b	0.8
0001b	0.85
0010b	0.90
0011b	0.95
0100b	1.0
0101b	1.05
0110b	1.10
0111b	1.15
1000b	1.20
Other	Reserved

Paged command behavior:

PAGE = 00h or FFh: Writes to this command update (BAh) USER_DATA_10 (ISHARE_CONFIG) for Channel A (PAGE=0). Reads to this command return the value of (BAh) USER_DATA_10 (ISHARE_CONFIG) for Channel A (PAGE=0).

PAGE = 01h: Writes to this command update (BAh) USER_DATA_10 (ISHARE_CONFIG) for Channel B (PAGE=1). Reads to this command return the value of (BAh) USER_DATA_10 (ISHARE_CONFIG) for Channel B (PAGE=1).

Phased command behavior:

PHASE = 00h to (highest order phase assigned to the current page): Writes to this command modify the ISHARE settings for individual phases. Reads to this command return the configured ISHARE settings for individual phases.

PHASE = 80h or FFh: Writes to (BAh) USER_DATA_10 (ISHARE_CONFIG) modify the current sense offset for all individual phases assigned to the current PAGE . Reads to this command return the configured ISHARE settings for PHASE =0.

1.2.96 (BBh) USER_DATA_11 (MFR_PROTECTION_CONFIG)

CMD Address	BBh
Write Transaction:	Write Block
Read Transaction:	Read Block
Format:	Unsigned Binary (10 bytes)
Paged:	No
Phased:	No
NVM Back-up:	EEPROM
Updates:	on-the-fly

Configure any protection features not included in the PMBus spec.

(BBh) USER_DATA_11 (MFR_PROTECTION_CONFIG) Register Map

79	78	77	76	75	74	73	72
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
71	70	69	68	67	66	65	64
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
63	62	61	60	59	58	57	56
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
55	54	53	52	51	50	49	48
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
47	46	45	44	43	42	41	40
RW	RW	R	RW	RW	RW	RW	RW
ISHAREW		0	OVFIX CHB				
39	38	37	36	35	34	33	32
R	R	R	R	R	R	RW	RW
0	0	0	0	0	0	PSFLT RESP	
31	30	29	28	27	26	25	24
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
23	22	21	20	19	18	17	16
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
RW	RW	R	RW	RW	RW	RW	RW
HICCUP		0	OVFIX CHA				
7	6	5	4	3	2	1	0
R	R	R	RW	RW	RW	RW	RW
0	0	0	TI ONLY			OCL CYCL	

LEGEND: R/W = Read/Write; R = Read only

Table 1-145. Register Field Descriptions

Bit	Field	Access	Reset	Description
79:48	Reserved	R	0	Reserved. Set to 0.
47:46	ISHAREW	RW	NVM	ISHARE Warning threshold. See the table below.
45	Reserved	R	0	Reserved. Set to 0.
44:40	OVFIX CHB	RW	NVM	Fixed OVP threshold for channel B. See the table below.
33:32	PSFLT RESP	RW	NVM	Fault response setting for PS fault (TAO HIGH). See the table below
31:16	Reserved	R	0	Reserved. Set to 0.
15:14	HICCUP	RW	NVM	Selects the Hiccup wait time for all hiccup faults. 00b: 5 ms 01b: 10 ms 10b: 25 ms 11b: 50 ms
12:8	OVFIX CHA	RW	NVM	Fixed OV threshold for channel A. See the table below.
7:5	Reserved	R	0	Reserved. Set to 0.
4:2	TI ONLY	RW	NVM	TI only configuration bits. Do not change the value of this field.
1:0	OCL CYCL	RW	NVM	Cycle counter for Phase OCL Warning condition. See the table below.

Table 1-146. MFR Fault Response Settings

PHFLT RESP	Converter Response Response
00b	Continue uninterrupted
01b	Hiccup immediately
10b	Latch off immediately
11b	Reserved

Table 1-147. Number of Cycles before fault declared

PHOCL CYCL	Number of cycles before fault is declared
00b	1
01b	2
10b	4
11b	8

Table 1-148. ISHARE Warning threshold

ISHAREW	ISHARE Warning Threshold (A)
00b	5 A
01b	10 A
10b	20 A
11b	Reserved

Table 1-149. Fixed OVP Thresholds

OVFIX CHA, OVFIX CHB	Fixed OVP threshold (V)
00000b	3.7
00001b	3.6
00010b	3.5
00011b	3.4
00100b	3.3
00101b	3.2
00110b	3.1
00111b	3

Table 1-149. Fixed OVP Thresholds (continued)

OVFIX CHA, OVFIX CHB	Fixed OVP threshold (V)
01000b	2.9
01001b	2.8
01010b	2.7
01011b	2.6
01100b	2.5
01101b	2.4
01110b	2.3
01111b	2.2
10000b	2.1
10001b	2
10010b	1.9
10011b	1.8
10100b	1.7
10101b	1.6
10110b	1.5
10111b	1.4
11000b	1.3
11001b	1.2
11010b	1.1
11011b	1
11100b	0.9
11101b	0.8
11110b	0.7
11111b	0.6

1.2.97 (BDh) USER_DATA_13 (MFR_CALIBRATION_CONFIG)

CMD Address	BDh
Write Transaction:	Write Block
Read Transaction:	Read Block
Format:	Unsigned Binary (15 bytes)
Paged:	No
Phased:	No
NVM Back-up:	EEPROM
Updates:	on-the-fly

The MFR_CALIBRATION_CONFIG command contains any non-PMBus standard calibration factors which may be applied to the device.

119	118	117	116	115	114	113	112
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
111	110	109	108	107	106	105	104
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
103	102	101	100	99	98	97	96
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
95	94	93	92	91	90	89	88
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
87	86	85	84	83	82	81	80
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
79	78	77	76	75	74	73	72
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
71	70	69	68	67	66	65	64
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
63	62	61	60	59	58	57	56
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
55	54	53	52	51	50	49	48
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
47	46	45	44	43	42	41	40
RW	RW	RW	RW	RW	RW	RW	RW
IIN OFS							

(B3h) USER_DATA_13 (MFR_CALIBRATION_CONFIG) Data Bytes Per Phase

39	38	37	36	35	34	33	32
RW	RW	RW	RW	RW	RW	RW	RW
GIINMAX							
31	30	29	28	27	26	25	24
RW	R	R	R	R	RW	RW	RW
GIINMAX	0	0	0	0	GIINSHUNT		
23	22	21	20	19	18	17	16
RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
CALCIIN EFF CHB				CALCIIN EFF CHA			
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0

LEGEND: R/W = Read/Write; R = Read only

Table 1-150. Register Field Descriptions

Bit	Field	Access	Reset	Description
119:48	Reserved	R	0	Reserved. Set to 0
47:40	IIN OFS	RW	NVM	Offset calibration for input current measurement. Two's complement with LSB = 0.0625 A
39:31	GIINMAX	RW	NVM	Digital gain adjustment for input current measurement. LSB = 0.5
30:27	Reserved	R	0	Reserved. Set to 0
26:24	GIINSHUNT	RW	NVM	Analog gain adjustment for input current measurement. See the table below.
23:16	Reserved	R	0	Reserved. Set to 0
15:12	CALCIIN EFF CHB	RW	NVM	Calculated IIN efficiency assumption for channel B. See the table below.
11:8	CALCIIN EFF CHA	RW	NVM	Calculated IIN efficiency assumption for channel A. See the table below.
7:0	R	0	Reserved. Set to 0	

Table 1-151. Analog Input Current Sensor Gain Values

GIINSHUNT	Input Current Sensor Analog Gain (V/V)
000b	20
001b	30
010b	40
011b	50
100b	60
101b	70
110b	80
111b	100

Table 1-152. Calculated input current gain values

CALCIIN EFF CHA, CALCIIN EFF CHB	Calculated IIN efficiency assumption (%)
0000b	89.0%
0001b	89.5%
0010b	90.0%
0011b	90.5%
0100b	91.0%
0101b	91.5%
0110b	92.0%
0111b	92.5%
1000b	93.0%
1001b	93.5%
1010b	94.0%
1011b	94.5%
1100b	95.0%
1101b	95.5%
1110b	96.0%
1111b	96.5%

1.2.98 (CDh) MFR_SPECIFIC_CD (MULTIFUNCTION_PIN_CONFIG_1)

CMD Address	CDh
Write Transaction:	Write Block
Read Transaction:	Read Block
Format:	Unsigned Binary (32 bytes)
Paged:	No
Phased:	No
Updates:	Updates take effect only after NVM store and power cycle
NVM Back-up:	Yes

Configure multi-function pins. Most of this command comprises TI-only bit fields. TI recommends NOT to modify these fields from the default values. However, the specified fields can be used to configure a SYNC or RESET# pin for example.

255	254	253	252	251	250	249	248
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							
247	246	245	244	243	242	241	240
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							
239	238	237	236	235	234	233	232
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							
231	230	229	228	227	226	225	224
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							
223	222	221	220	219	218	217	216
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							
215	214	213	212	211	210	209	208
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							
207	206	205	204	203	202	201	200
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							
199	198	197	196	195	194	193	192
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							
191	190	189	188	187	186	185	184
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							
183	182	181	180	179	178	177	176
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							

(CDh) MFR_SPECIFIC_CD (MULTIFUNCTION_PIN_CONFIG_1) Register Map

175	174	173	172	171	170	169	168
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							
167	166	165	164	163	162	161	160
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							
159	158	157	156	155	154	153	152
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							
151	150	149	148	147	146	145	144
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY		PIN43				TI ONLY	
143	142	141	140	139	138	137	136
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							
135	134	133	132	131	130	129	128
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY						PIN19	
127	126	125	124	123	122	121	120
RW	RW	RW	RW	RW	RW	RW	RW
PIN19							
119	118	117	116	115	114	113	112
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							
111	110	109	108	107	106	105	104
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							
103	102	101	100	99	98	97	96
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							
95	94	93	92	91	90	89	88
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							
87	86	85	84	83	82	81	80
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							
79	78	77	76	75	74	73	72
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							
71	70	69	68	67	66	65	64
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							

(CDh) MFR_SPECIFIC_CD (MULTIFUNCTION_PIN_CONFIG_1) Register Map (continued)

63	62	61	60	59	58	57	56
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							
55	54	53	52	51	50	49	48
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							
47	46	45	44	43	42	41	40
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							
39	38	37	36	35	34	33	32
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							
31	30	29	28	27	26	25	24
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							
23	22	21	20	19	18	17	16
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							
15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							

LEGEND: R/W = Read/Write; R = Read only

Table 1-153. Register Field Descriptions

Bit	Field	Access	Reset	Description
255:150	TI ONLY	RW	NVM	TI only fields. Do not modify from default values.
149:146	PIN43	RW	NVM	Pin 43 configuration: 0010b: ATSEN. Temperature sense for channel A 0100b: BTSEN. Temperature sense for channel B 0110b: TSEN. Temperature sense for channels A and B Others: Do not use. TPS536xx does not validate data in this field.
145:130	TI ONLY	RW	NVM	TI only fields. Do not modify from default values.
129:120	PIN19	RW	NVM	Pin 19 configuration: 01 0000 0100b: BVR_EN 00 0000 1000b: SYNC_IN 00 0000 1001b: SYNC_OUT 01 X000 1100b: RESET#
119:0	TI ONLY	RW	NVM	TI only fields. Do not modify from default values.

1.2.99 (CEh) MFR_SPECIFIC_CD (MULTIFUNCTION_PIN_CONFIG_2)

CMD Address	CEh
Write Transaction:	Write Block
Read Transaction:	Read Block
Format:	Unsigned Binary (31 bytes)
Paged:	No
Phased:	No
Updates:	Updates take effect only after NVM store and power cycle
NVM Back-up:	Yes

Configure multi-function pins. Most of this command comprises TI-only bit fields. Ti recommends NOT to modify these fields from the default values.

247	246	245	244	243	242	241	240
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							
239	238	237	236	235	234	233	232
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							
231	230	229	228	227	226	225	224
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							
223	222	221	220	219	218	217	216
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							
215	214	213	212	211	210	209	208
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							
207	206	205	204	203	202	201	200
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							
199	198	197	196	195	194	193	192
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							
191	190	189	188	187	186	185	184
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							
183	182	181	180	179	178	177	176
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							

(CEh) MFR_SPECIFIC_CE (MULTIFUNCTION_PIN_CONFIG_2) Register Map

175	174	173	172	171	170	169	168
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							

(CEh) MFR_SPECIFIC_CE (MULTIFUNCTION_PIN_CONFIG_2) Register Map (continued)

167	166	165	164	163	162	161	160
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							
159	158	157	156	155	154	153	152
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							
151	150	149	148	147	146	145	144
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY		PIN43				TI ONLY	
143	142	141	140	139	138	137	136
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							
135	134	133	132	131	130	129	128
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							
127	126	125	124	123	122	121	120
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							
119	118	117	116	115	114	113	112
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							
111	110	109	108	107	106	105	104
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							
103	102	101	100	99	98	97	96
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							
95	94	93	92	91	90	89	88
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							
87	86	85	84	83	82	81	80
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							
79	78	77	76	75	74	73	72
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							
71	70	69	68	67	66	65	64
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							
63	62	61	60	59	58	57	56
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							

(CEh) MFR_SPECIFIC_CE (MULTIFUNCTION_PIN_CONFIG_2) Register Map (continued)

55	54	53	52	51	50	49	48
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							
47	46	45	44	43	42	41	40
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							
39	38	37	36	35	34	33	32
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							
31	30	29	28	27	26	25	24
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							
23	22	21	20	19	18	17	16
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							
15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY							
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY		PIN44				TI ONLY	

LEGEND: R/W = Read/Write; R = Read only

Table 1-154. Register Field Descriptions

Bit	Field	Access	Reset	Description
255:6	TI ONLY	RW	NVM	TI only fields. Do not modify from default values.
5:2	PIN44	RW	NVM	Pin 44 configuration 0010b: ATSEN. Channel A temperature sense 0100b: BTSEN. Channel B temperature sense Other: Do not use. TPS536xx does not perform data validation.
1:0	TI ONLY	RW	NVM	TI only fields. Do not modify from default values.

1.2.100 (CFh) MFR_SPECIFIC_CF (SMBALERT_MASK_EXTENDED)

CMD Address	CFh
Write Transaction:	Write Block
Read Transaction:	Read Block
Format:	Unsigned Binary (7 bytes)
Paged:	No
Phased:	No
Updates:	On-the-fly
NVM Back-up:	Yes On POR, all mask bits follow the value of the SMBALERT_MASK_MFR [6] NVM bit. Individual mask bits are usable on-the-fly but do not have individual NVM backup.

SMBALERT_MASK bits for bits in the (DDh) MFR_SPECIFIC_DD (STATUS_EXTENDED) command block.

(DDh) MFR_SPECIFIC_DD (STATUS_EXTENDED) Register Map

55	54	53	52	51	50	49	48
RW	RW	RW	RW	RW	RW	RW	R
IV ACCESS	BAD GRP	RD GRP	CML OTHER	ABORTED	ARB LOST	NACK COUNT	0
47	46	45	44	43	42	41	40
R	R	RW	RW	RW	RW	RW	R
0	0	BYTE NUM SMALL	BYTE NUM BIG	BLK SIZE SMALL	BLK SIZE BIG	LOCKED	0
39	38	37	36	35	34	33	32
RW	RW	RW	RW	R	R	R	R
VSP OPEN CHB	VSP OPEN CHA	VSN OPEN CHB	VSN OPEN CHA	0	0	0	0
31	30	29	28	27	26	25	24
R	R	R	RW	R	RW	RW	RW
0	0	0	SYNC FLT	0	NO UPDATE	IV BOOT	IV ADDR
23	22	21	20	19	18	17	16
R	R	R	R	RW	RW	R	R
0	0	0	0	PH CFG ERR	CFG FILE ERR	0	0
15	14	13	12	11	10	9	8
RW	RW	R	R	R	R	R	R
TAO LOW CHB	TAO LOW CHA	0		0	0	0	0
7	6	5	4	3	2	1	0
R	R	RW	RW	RW	RW	RW	RW
0	0	PRE OVP CHB	PRE OVP CHA	OV TRK CHB	OV TRK CHA	OV FIX CHB	OV FIX CHA

LEGEND: R/W = Read/Write; R = Read only

Table 1-155. Register Field Descriptions

Bit	Field	Access	Reset	Description
55	IV ACCESS	RW	0b	SMBALERT mask bit. Invalid PMBus Access (attempt to write read-only command) 0b: Condition MAY assert SMB_ALERT# 1b: Condition MAY NOT assert SMB_ALERT#

Table 1-155. Register Field Descriptions (continued)

Bit	Field	Access	Reset	Description
54	BAD GRP	RW	0b	SMBALERT mask bit. Bad Group Command transaction occurred 0b: Condition MAY assert SMB_ALERT# 1b: Condition MAY NOT assert SMB_ALERT#
53	RD GRP	RW	0b	SMBALERT mask bit. Group command with READ transaction occurred 0b: Condition MAY assert SMB_ALERT# 1b: Condition MAY NOT assert SMB_ALERT#
52	CML OTHER	RW	0b	SMBALERT mask bit. A CML error other than those explicitly listed occurred. 0b: Condition MAY assert SMB_ALERT# 1b: Condition MAY NOT assert SMB_ALERT#
51	ABORTED	RW	0b	SMBALERT mask bit. PMBus Transaction aborted by master 0b: Condition MAY assert SMB_ALERT# 1b: Condition MAY NOT assert SMB_ALERT#
50	ARB LOST	RW	0b	SMBALERT mask bit. PMBus Data Arbitration Lost 0b: Condition MAY assert SMB_ALERT# 1b: Condition MAY NOT assert SMB_ALERT#
49	NACK COUNT	RW	0b	SMBALERT mask bit. Master NACK'd Block Size byte. 0b: Condition MAY assert SMB_ALERT# 1b: Condition MAY NOT assert SMB_ALERT#
48:46	Reserved	R	0b	Reserved
45	BYTE NUM SMALL	RW	0b	SMBALERT mask bit. Too Few bytes received. 0b: Condition MAY assert SMB_ALERT# 1b: Condition MAY NOT assert SMB_ALERT#
44	BYTE NUM BIG	RW	0b	SMBALERT mask bit. Too Many bytes received. 0b: Condition MAY assert SMB_ALERT# 1b: Condition MAY NOT assert SMB_ALERT#
43	BLK SIZE SMALL	RW	0b	SMBALERT mask bit. Block Size too small for command. 0b: Condition MAY assert SMB_ALERT# 1b: Condition MAY NOT assert SMB_ALERT#
42	BLK SIZE BIG	RW	0b	SMBALERT mask bit. Block Size too big for command. 0b: Condition MAY assert SMB_ALERT# 1b: Condition MAY NOT assert SMB_ALERT#
41	LOCKED	RW	0b	SMBALERT mask bit. Attempted write to write-protected register. 0b: Condition MAY assert SMB_ALERT# 1b: Condition MAY NOT assert SMB_ALERT#
40	Reserved	R	0b	Reserved
39	VSP OPEN CHB	RW	0b	SMBALERT mask bit. VSP OPEN Channel B. 0b: Condition MAY assert SMB_ALERT# 1b: Condition MAY NOT assert SMB_ALERT#
38	VSP OPEN CHA	RW	0b	SMBALERT mask bit. VSP OPEN Channel A. 0b: Condition MAY assert SMB_ALERT# 1b: Condition MAY NOT assert SMB_ALERT#
37	VSN OPEN CHB	RW	0b	SMBALERT mask bit. VSN OPEN Channel B. 0b: Condition MAY assert SMB_ALERT# 1b: Condition MAY NOT assert SMB_ALERT#

Table 1-155. Register Field Descriptions (continued)

Bit	Field	Access	Reset	Description
36	VSN OPEN CHA	RW	0b	SMBALERT mask bit. VSN OPEN Channel A. 0b: Condition MAY assert SMB_ALERT# 1b: Condition MAY NOT assert SMB_ALERT#
35:29	Reserved	R	0b	Reserved
28	SYNC FLT	RW	0b	SMBALERT mask bit. Sync Fault. 0b: Condition MAY assert SMB_ALERT# 1b: Condition MAY NOT assert SMB_ALERT#
27	Reserved	R	0b	Reserved
26	NO UPDATE	RW	0b	SMBALERT mask bit. UPDATE NOT ALLOWED. 0b: Condition MAY assert SMB_ALERT# 1b: Condition MAY NOT assert SMB_ALERT#
24	IV ADDR	RW	0b	SMBALERT mask bit. Invalid ADDR pin detection. 0b: Condition MAY assert SMB_ALERT# 1b: Condition MAY NOT assert SMB_ALERT#
23:20	Reserved	R	0b	Reserved
19	PH CFG ERR	RW	0b	SMBALERT mask bit. Invalid PHASE_CONFIG. 0b: Condition MAY assert SMB_ALERT# 1b: Condition MAY NOT assert SMB_ALERT#
18	CFG FILE ERR	RW	0b	SMBALERT mask bit. Invalid Config File. 0b: Condition MAY assert SMB_ALERT# 1b: Condition MAY NOT assert SMB_ALERT#
17:16	Reserved	R	0b	Reserved
15	TAO LOW CHB	RW	0b	SMBALERT mask bit. TAO Low (channel B). 0b: Condition MAY assert SMB_ALERT# 1b: Condition MAY NOT assert SMB_ALERT#
14	TAO LOW CHA	RW	0b	SMBALERT mask bit. TAO Low (channel A). 0b: Condition MAY assert SMB_ALERT# 1b: Condition MAY NOT assert SMB_ALERT#
13:6	Reserved	R	0b	Reserved
5	PRE OVP CHB	RW	0b	SMBALERT mask bit. Pre-biased over-voltage fault (Channel B) 0b: Condition MAY assert SMB_ALERT# 1b: Condition MAY NOT assert SMB_ALERT#
4	PRE OVP CHA	RW	0b	SMBALERT mask bit. Pre-biased over-voltage fault (Channel A) 0b: Condition MAY assert SMB_ALERT# 1b: Condition MAY NOT assert SMB_ALERT#
3	OV TRK CHB	RW	0b	SMBALERT mask bit. Tracking over-voltage fault (Channel B) 0b: Condition MAY assert SMB_ALERT# 1b: Condition MAY NOT assert SMB_ALERT#
2	OV TRK CHA	RW	0b	SMBALERT mask bit. Tracking over-voltage fault (Channel A) 0b: Condition MAY assert SMB_ALERT# 1b: Condition MAY NOT assert SMB_ALERT#
1	OV FIX CHB	RW	0b	SMBALERT mask bit. Fixed over-voltage fault (Channel B) 0b: Condition MAY assert SMB_ALERT# 1b: Condition MAY NOT assert SMB_ALERT#

Table 1-155. Register Field Descriptions (continued)

Bit	Field	Access	Reset	Description
0	OV FIX CHA	RW	0b	SMBALERT mask bit. Fixed over-voltage fault (Channel A) 0b: Condition MAY assert SMB_ALERT# 1b: Condition MAY NOT assert SMB_ALERT#

1.2.101 (D1h) MFR_SPECIFIC_D1 (READ_VOUT_MIN_MAX)

CMD Address	D1h
Write Transaction:	Write Block
Read Transaction:	Read Block
Format:	SLINEAR11
Paged:	Yes
Phased:	No
Updates:	On-the-fly
NVM Back-up:	No

This command returns the highest and lowest READ_VOUT values recorded.

(D1h) MFR_SPECIFIC_D1 (READ_VOUT_MIN_MAX) Register Map

31	30	29	28	27	26	25	24
RW	RW	RW	RW	RW	RW	RW	RW
READ VOUT MIN (High Byte)							
23	22	21	20	19	18	17	16
RW	RW	RW	RW	RW	RW	RW	RW
READ VOUT MIN (Low Byte)							
15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
READ VOUT MAX (High Byte)							
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
READ VOUT MAX (Low Byte)							

LEGEND: R/W = Read/Write; R = Read only

Table 1-156. Register Field Descriptions

Bit	Field	Access	Reset	Description
31:16	READ VOUT MIN	RW	0000h	Minimum recorded READ_VOUT. Format is SLINEAR11
15:0	READ VOUT MAX	RW	0000h	Maximum recorded READ_VOUT. Format is SLINEAR11

Control of Peak Logging:

Issue a write transaction with the following values to control peak logging functions. Logging is not automatically started or stopped by TPS536xx.

Table 1-157. Logging Control

Value Written	Behavior
0000 0001h	Pause minimum value logging and resume maximum value logging
0000 0002h	Pause maximum value logging and resume minimum value logging
0000 0004h	Pause minimum and maximum value logging
0000 0008h	Resume minimum value logging (if paused) and resume maximum value logging
0000 0010h	Resume maximum value logging (if paused) and resume minimum value logging
0000 0020h	Resume minimum and maximum value logging (if paused)

Table 1-157. Logging Control (continued)

Value Written	Behavior
0000 0040h	Reset the minimum value logging
0000 0080h	Reset the maximum value logging
0000 0100h	Reset both minimum and maximum value logging
Other	Invalid/Unsupported data.

1.2.102 (D2h) MFR_SPECIFIC_D2 (READ_IOUT_MIN MAX)

CMD Address	D2h
Write Transaction:	Write Block
Read Transaction:	Read Block
Format:	SLINEAR11
Paged:	Yes
Phased:	No
Updates:	On-the-fly
NVM Back-up:	No

This command returns the highest and lowest READ_IOUT values recorded.

(D2h) MFR_SPECIFIC_D2 (READ_IOUT_MIN_MAX) Register Map

31	30	29	28	27	26	25	24
RW	RW	RW	RW	RW	RW	RW	RW
READ IOUT MIN (High Byte)							
23	22	21	20	19	18	17	16
RW	RW	RW	RW	RW	RW	RW	RW
READ IOUT MIN (Low Byte)							
15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
READ IOUT MAX (High Byte)							
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
READ IOUT MAX (Low Byte)							

LEGEND: R/W = Read/Write; R = Read only

Table 1-158. Register Field Descriptions

Bit	Field	Access	Reset	Description
31:16	READ IOUT MIN	RW	0000h	Minimum recorded READ_IOUT in SLINEAR11 format.
15:0	READ IOUT MAX	RW	0000h	Maximum recorded READ_IOUT in SLINEAR11 format.

Control of Peak Logging:

Issue a write transaction with the following values to control peak logging functions. Logging is not automatically started or stopped by TPS536xx.

Table 1-159. Logging Control

Value Written	Behavior
0000 0001h	Pause minimum value logging and resume maximum value logging
0000 0002h	Pause maximum value logging and resume minimum value logging
0000 0004h	Pause minimum and maximum value logging
0000 0008h	Resume minimum value logging (if paused) and resume maximum value logging
0000 0010h	Resume maximum value logging (if paused) and resume minimum value logging
0000 0020h	Resume minimum and maximum value logging (if paused)

Table 1-159. Logging Control (continued)

Value Written	Behavior
0000 0040h	Reset the minimum value logging
0000 0080h	Reset the maximum value logging
0000 0100h	Reset both minimum and maximum value logging
Other	Invalid/Unsupported data.

1.2.103 (D3h) MFR_SPECIFIC_D3 (READ_TEMPERATURE_MIN_MAX)

CMD Address	D3h
Write Transaction:	Write Block
Read Transaction:	Read Block
Format:	SLINEAR11
Paged:	Yes
Phased:	No
Updates:	On-the-fly
NVM Back-up:	No

This command returns the highest and lowest READ_TEMPERATURE_1 / READ_TEMPERATURE_2 values recorded.

(D3h) MFR_SPECIFIC_D3 (READ_TEMPERATURE_MIN_MAX) Register Map

31	30	29	28	27	26	25	24
RW	RW	RW	RW	RW	RW	RW	RW
READ TEMP MIN (High Byte)							
23	22	21	20	19	18	17	16
RW	RW	RW	RW	RW	RW	RW	RW
READ TEMP MIN (Low Byte)							
15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
READ TEMP MAX (High Byte)							
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
READ TEMP MAX (Low Byte)							

LEGEND: R/W = Read/Write; R = Read only

Table 1-160. Register Field Descriptions

Bit	Field	Access	Reset	Description
31:16	READ TEMP MIN	RW	0000h	Minimum recorded READ_TEMPERATURE_1 / READ_TEMPERATURE_2. SLINEAR11 format.
15:0	READ TEMP MAX	RW	0000h	Maximum recorded READ_TEMPERATURE_1 / READ_TEMPERATURE_2. SLINEAR11 format.

Control of Peak Logging:

Issue a write transaction with the following values to control peak logging functions. Logging is not automatically started or stopped by TPS536xx.

Table 1-161. Logging Control

Value Written	Behavior
0000 0001h	Pause minimum value logging and resume maximum value logging
0000 0002h	Pause maximum value logging and resume minimum value logging
0000 0004h	Pause minimum and maximum value logging
0000 0008h	Resume minimum value logging (if paused) and resume maximum value logging
0000 0010h	Resume maximum value logging (if paused) and resume minimum value logging

Table 1-161. Logging Control (continued)

Value Written	Behavior
0000 0020h	Resume minimum and maximum value logging (if paused)
0000 0040h	Reset the minimum value logging
0000 0080h	Reset the maximum value logging
0000 0100h	Reset both minimum and maximum value logging
Other	Invalid/Unsupported data.

1.2.104 (D5h) MFR_SPECIFIC_D5 (READ_VIN_MIN_MAX)

CMD Address	D5h
Write Transaction:	Write Block
Read Transaction:	Read Block
Format:	SLINEAR11
Paged:	No
Phased:	No
Updates:	On-the-fly
NVM Back-up:	No

This command returns the highest and lowest READ_VIN values recorded.

(D5h) MFR_SPECIFIC_D5 (READ_VIN_MIN_MAX) Register Map

31	30	29	28	27	26	25	24
RW	RW	RW	RW	RW	RW	RW	RW
READ VIN MIN (High Byte)							
23	22	21	20	19	18	17	16
RW	RW	RW	RW	RW	RW	RW	RW
READ VIN MIN (Low Byte)							
15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
READ VIN MAX (High Byte)							
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
READ VIN MAX (Low Byte)							

LEGEND: R/W = Read/Write; R = Read only

Table 1-162. Register Field Descriptions

Bit	Field	Access	Reset	Description
31:16	READ VIN MIN	RW	00h	Minimum recorded READ VIN. SLINEAR11 format.
15:0	READ VIN MAX	RW	00h	Maximum recorded READ VIN. SLINEAR11 format.

Control of Peak Logging:

Issue a write transaction with the following values to control peak logging functions. Logging is not automatically started or stopped by TPS536xx.

Table 1-163. Logging Control

Value Written	Behavior
0000 0001h	Pause minimum value logging and resume maximum value logging
0000 0002h	Pause maximum value logging and resume minimum value logging
0000 0004h	Pause minimum and maximum value logging
0000 0008h	Resume minimum value logging (if paused) and resume maximum value logging
0000 0010h	Resume maximum value logging (if paused) and resume minimum value logging
0000 0020h	Resume minimum and maximum value logging (if paused)

Table 1-163. Logging Control (continued)

Value Written	Behavior
0000 0040h	Reset the minimum value logging
0000 0080h	Reset the maximum value logging
0000 0100h	Reset both minimum and maximum value logging
Other	Invalid/Unsupported data.

1.2.105 (D4h) MFR_SPECIFIC_D4 (READ_MFR_VOUT)

CMD Address	D4h
Write Transaction:	NA
Read Transaction:	Read Word
Format:	SLINEAR11
Paged:	Yes
Phased:	No
NVM Back-up:	No

The READ_VOUT command returns the actual, measured output voltage in the linear format.

(D4h) MFR_SPECIFIC_D4 (READ_MFR_VOUT) Register Map

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
READ VOUT EXP					READ VOUT MAN		
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
READ VOUT MAN							

LEGEND: R/W = Read/Write; R = Read only

Table 1-164. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:11	READ VOUT EXP	R	Current Status	Linear format two's complement exponent.
10:0	READ VOUT MAN	R	Current Status	Linear format two's complement mantissa.

Attempts to write read-only commands cause the CML OTHER fault condition, TPS536xx responds as follows:

- Set the CML bit in STATUS_BYTE
- Set the CML OTHER bit in STATUS_CML

Notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3

1.2.106 (D6h) MFR_SPECIFIC_D6 (READ_IIN_MIN_MAX)

CMD Address	D6h
Write Transaction:	Write Block
Read Transaction:	Read Block
Format:	SLINEAR11
Paged:	No
Phased:	No
Updates:	On-the-fly
NVM Back-up:	No

This command returns the highest and lowest READ_IIN values recorded.

Note

Peak data logged when using calculated input current (CALCIIN_RD = 1b) is not meaningful.

(D6h) MFR_SPECIFIC_D6 (READ_IIN_MIN_MAX) Register Map

31	30	29	28	27	26	25	24
RW	RW	RW	RW	RW	RW	RW	RW
READ IIN MIN (High Byte)							
23	22	21	20	19	18	17	16
RW	RW	RW	RW	RW	RW	RW	RW
READ IIN MIN (Low Byte)							
15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
READ IIN MAX (High Byte)							
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
READ IIN MAX (Low Byte)							

LEGEND: R/W = Read/Write; R = Read only

Table 1-165. Register Field Descriptions

Bit	Field	Access	Reset	Description
31:16	READ IIN MIN	RW	00h	Minimum recorded READ_IIN. SLINEAR11 format.
15:0	READ IIN MAX	RW	00h	Maximum recorded READ_IIN. SLINEAR11 format.

Control of Peak Logging:

Issue a write transaction with the following values to control peak logging functions. Logging is not automatically started or stopped by TPS536xx.

Table 1-166. Logging Control

Value Written	Behavior
0000 0001h	Pause minimum value logging and resume maximum value logging
0000 0002h	Pause maximum value logging and resume minimum value logging
0000 0004h	Pause minimum and maximum value logging
0000 0008h	Resume minimum value logging (if paused) and resume maximum value logging

Table 1-166. Logging Control (continued)

Value Written	Behavior
0000 0010h	Resume maximum value logging (if paused) and resume minimum value logging
0000 0020h	Resume minimum and maximum value logging (if paused)
0000 0040h	Reset the minimum value logging
0000 0080h	Reset the maximum value logging
0000 0100h	Reset both minimum and maximum value logging
Other	Invalid/Unsupported data.

1.2.107 (D7h) MFR_SPECIFIC_D7 (READ_PIN_MIN_MAX)

CMD Address	D7h
Write Transaction:	Write Block
Read Transaction:	Read Block
Format:	SLINEAR11
Paged:	No
Phased:	No
Updates:	On-the-fly
NVM Back-up:	No

This command returns the highest and lowest READ_PIN values recorded.

(D7h) MFR_SPECIFIC_D7 (READ_PIN_MIN_MAX) Register Map

31	30	29	28	27	26	25	24
RW	RW	RW	RW	RW	RW	RW	RW
READ PIN MIN (High Byte)							
23	22	21	20	19	18	17	16
RW	RW	RW	RW	RW	RW	RW	RW
READ PIN MIN (Low Byte)							
15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
READ PIN MAX (High Byte)							
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
READ PIN MAX (Low Byte)							

LEGEND: R/W = Read/Write; R = Read only

Table 1-167. Register Field Descriptions

Bit	Field	Access	Reset	Description
31:16	READ PIN MIN	RW	0000h	Minimum recorded READ PIN. SLINEAR11 format.
15:0	READ PIN MAX	RW	0000h	Maximum recorded READ PIN. SLINEAR11 format.

Control of Peak Logging:

Issue a write transaction with the following values to control peak logging functions. Logging is not automatically started or stopped by TPS536xx.

Table 1-168. Logging Control

Value Written	Behavior
0000 0001h	Pause minimum value logging and resume maximum value logging
0000 0002h	Pause maximum value logging and resume minimum value logging
0000 0004h	Pause minimum and maximum value logging
0000 0008h	Resume minimum value logging (if paused) and resume maximum value logging
0000 0010h	Resume maximum value logging (if paused) and resume minimum value logging
0000 0020h	Resume minimum and maximum value logging (if paused)

Table 1-168. Logging Control (continued)

Value Written	Behavior
0000 0040h	Reset the minimum value logging
0000 0080h	Reset the maximum value logging
0000 0100h	Reset both minimum and maximum value logging
Other	Invalid/Unsupported data.

1.2.108 (D8h) MFR_SPECIFIC_D8 (READ_POUT_MIN_MAX)

CMD Address	D8h
Write Transaction:	Write Block
Read Transaction:	Read Block
Format:	SLINEAR11
Paged:	Yes
Phased:	No
Updates:	On-the-fly
NVM Back-up:	No

This command returns the highest and lowest READ_POUT values recorded.

(D8h) MFR_SPECIFIC_D8 (READ_POUT_MIN_MAX) Register Map

31	30	29	28	27	26	25	24
RW	RW	RW	RW	RW	RW	RW	RW
READ POUT MIN (High Byte)							
23	22	21	20	19	18	17	16
RW	RW	RW	RW	RW	RW	RW	RW
READ POUT MIN (Low Byte)							
15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
READ POUT MAX (High Byte)							
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
READ POUT MAX (Low Byte)							

LEGEND: R/W = Read/Write; R = Read only

Table 1-169. Register Field Descriptions

Bit	Field	Access	Reset	Description
31:16	READ POUT MIN	RW	00h	Minimum recorded READ_POUT. SLINEAR11 format.
15:0	READ POUT MAX	RW	00h	Maximum recorded READ_POUT. SLINEAR11 format.

Control of Peak Logging:

Issue a write transaction with the following values to control peak logging functions. Logging is not automatically started or stopped by TPS536xx.

Table 1-170. Logging Control

Value Written	Behavior
0000 0001h	Pause minimum value logging and resume maximum value logging
0000 0002h	Pause maximum value logging and resume minimum value logging
0000 0004h	Pause minimum and maximum value logging
0000 0008h	Resume minimum value logging (if paused) and resume maximum value logging
0000 0010h	Resume maximum value logging (if paused) and resume minimum value logging
0000 0020h	Resume minimum and maximum value logging (if paused)

Table 1-170. Logging Control (continued)

Value Written	Behavior
0000 0040h	Reset the minimum value logging
0000 0080h	Reset the maximum value logging
0000 0100h	Reset both minimum and maximum value logging
Other	Invalid/Unsupported data.

1.2.109 (DAh) MFR_SPECIFIC_DA (READ_ALL)

CMD Address	DAh
Write Transaction:	NA
Read Transaction:	Read Block
Format:	Unsigned Binary (14 bytes)
Paged:	Yes
Phased:	No
NVM Back-up:	No

READ_ALL provides for a 14-byte block BLOCK read of STATUS_WORD and Telemetry values to improve bus utilization for poling by combining multiple READ functions into a single command, eliminating the need for multiple address and command code bytes.

111	110	109	108	107	106	105	104
R	R	R	R	R	R	R	R
READ PIN (MSB)							
103	102	101	100	99	98	97	96
R	R	R	R	R	R	R	R
READ PIN (LSB)							
95	94	93	92	91	90	89	88
R	R	R	R	R	R	R	R
READ POUT (MSB)							
87	86	85	84	83	82	81	80
R	R	R	R	R	R	R	R
READ POUT (LSB)							
79	78	77	76	75	74	73	72
R	R	R	R	R	R	R	R
READ TEMP 1 (MSB)							
71	70	69	68	67	66	65	64
R	R	R	R	R	R	R	R
READ TEMP 1 (LSB)							

(DAh) MFR SPECIFIC DA (READ ALL) Register Map

63	62	61	60	59	58	57	56
R	R	R	R	R	R	R	R
READ IIN (MSB)							
55	54	53	52	51	50	49	48
R	R	R	R	R	R	R	R
READ IIN (LSB)							
47	46	45	44	43	42	41	40
R	R	R	R	R	R	R	R
READ VIN (MSB)							
39	38	37	36	35	34	33	32
R	R	R	R	R	R	R	R
READ VIN (LSB)							

(DAh) MFR SPECIFIC DA (READ ALL) Register Map (continued)

31	30	29	28	27	26	25	24
R	R	R	R	R	R	R	R
READ IOUT (MSB)							
23	22	21	20	19	18	17	16
R	R	R	R	R	R	R	R
READ IOUT (LSB)							
15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
READ MFR VOUT (MSB)							
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
READ MFR VOUT (LSB)							

LEGEND: R/W = Read/Write; R = Read only

Table 1-171. Register Field Descriptions

Bit	Field	Access	Reset	Description
111:96	READ PIN	R	Current Status	READ_PIN . SLINEAR11 format
95:80	READ POUT	R	Current Status	READ_POUT . SLINEAR11 format
79:64	READ TEMP 1	R	Current Status	READ_TEMPERATURE_1 . SLINEAR11 format
63:48	READ IIN	R	Current Status	READ_IIN . SLINEAR11 format
47:32	READ VIN	R	Current Status	READ_VIN . SLINEAR11 format
31:16	READ IOUT	R	Current Status	READ_IOUT . SLINEAR11 format
15:0	READ MFR VOUT	R	Current Status	MFR_SPECIFIC_D4 (READ_MFR_VOUT) . SLINEAR11 format

Attempts to write read-only commands cause the CML OTHER fault condition, TPS536xx responds as follows:

- Set the CML bit in STATUS_BYTE
- Set the CML OTHER bit in STATUS_CML

Notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3

1.2.110 (DBh) MFR_SPECIFIC_DB (STATUS_ALL)

CMD Address	DBh
Write Transaction:	NA
Read Transaction:	Read Block
Format:	Unsigned Binary (18 bytes)
Paged:	Yes
Phased:	No
NVM Back-up:	No

STATUS_ALL provides for a 14-byte block of STATUS command codes. This can reduce bus utilization to read multiple faults.

143	142	141	140	139	138	137	136
R	R	R	R	R	R	R	R
STATUS EXTENDED (MSB)							
135	134	133	132	131	130	129	128
R	R	R	R	R	R	R	R
STATUS EXTENDED							
127	126	125	124	123	122	121	120
R	R	R	R	R	R	R	R
STATUS EXTENDED							
119	118	117	116	115	114	113	112
R	R	R	R	R	R	R	R
STATUS EXTENDED							
111	110	109	108	107	106	105	104
R	R	R	R	R	R	R	R
STATUS EXTENDED							
103	102	101	100	99	98	97	96
R	R	R	R	R	R	R	R
STATUS EXTENDED							
95	94	93	92	91	90	89	88
R	R	R	R	R	R	R	R
STATUS EXTENDED (LSB)							

(DBh) MFR SPECIFIC DB (STATUS ALL) Register Map

87	86	85	84	83	82	81	80
R	R	R	R	R	R	R	R
STATUS PHASES (MSB)							
79	78	77	76	75	74	73	72
R	R	R	R	R	R	R	R
STATUS PHASES							
71	70	69	68	67	66	65	64
R	R	R	R	R	R	R	R
STATUS OTHER							
63	62	61	60	59	58	57	56

(DBh) MFR SPECIFIC DB (STATUS ALL) Register Map (continued)

R	R	R	R	R	R	R	R
STATUS CML							
55	54	53	52	51	50	49	48
R	R	R	R	R	R	R	R
STATUS MFR							
47	46	45	44	43	42	41	40
R	R	R	R	R	R	R	R
STATUS TEMPERATURE							
39	38	37	36	35	34	33	32
R	R	R	R	R	R	R	R
STATUS INPUT							
31	30	29	28	27	26	25	24
R	R	R	R	R	R	R	R
STATUS IOUT							
23	22	21	20	19	18	17	16
R	R	R	R	R	R	R	R
STATUS VOUT							
15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
STATUS WORD (MSB)							
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
STATUS WORD (LSB)							

LEGEND: R/W = Read/Write; R = Read only

Table 1-172. Register Field Descriptions

Bit	Field	Access	Reset	Description
143:88	STATUS EXTENDED	R	Current Status	MFR_SPECIFIC_DD (STATUS_EXTENDED)
87:72	STATUS PHASES	R	Current Status	MFR_SPECIFIC_DC (STATUS_PHASES)
71:64	STATUS OTHER	R	Current Status	STATUS_OTHER
63:56	STATUS CML	R	Current Status	STATUS_CML
55:48	STATUS MFR	R	Current Status	STATUS_MFR_SPECIFIC
47:40	STATUS TEMPERATURE	R	Current Status	STATUS_TEMPERATURE
39:32	STATUS INPUT	R	Current Status	STATUS_INPUT
31:24	STATUS IOUT	R	Current Status	STATUS_IOUT
23:16	STATUS VOUT	R	Current Status	STATUS_VOUT

Table 1-172. Register Field Descriptions (continued)

Bit	Field	Access	Reset	Description
15:0	STATUS WORD	R	Current Status	STATUS_WORD

Attempts to write read-only commands cause the CML OTHER fault condition, TPS536xx responds as follows:

- Set the CML bit in STATUS_BYTE
- Set the CML OTHER bit in STATUS_CML
- Notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3

Writes to STATUS ALL do not clear asserted status bits.

1.2.111 (DCh) MFR_SPECIFIC_DC (STATUS_PHASES)

CMD Address	DCh
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	Unsigned Binary (2 bytes)
Paged:	Yes
Phased:	Yes
Updates:	On-the-fly
NVM Back-up:	No

When PHASE = FFh or 80h, reads to this command return a data word detailing which phases have experienced fault conditions. When PHASE != FFh, reads to this command return a data word detailing which fault(s) the current PHASE has experienced. PHASE number assignment is per PHASE_CONFIG . Bits corresponding to unused (unassigned or disabled) phase numbers are always equal to 0b.

(DCh) MFR_SPECIFIC_DC (STATUS_PHASES), PHASE = 80h or FFh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	PH12	PH11	PH10	PH9	PH8	PH7	PH6	PH5	PH4	PH3	PH2	PH1

LEGEND: R/W = Read/Write; R = Read only

Table 1-173. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:12	Reserved	R	0b	Reserved
11	PH12	RW	0b	**Don't care for TPS53676** 0b. The power stage assigned to PHASE =12d has NOT experienced a fault 1b. The power stage assigned to PHASE =12d has experienced a fault. Set PHASE =12d, and read this command again for more information.
10	PH11	RW	0b	**Don't care for TPS53676** 0b. The power stage assigned to PHASE =10d has NOT experienced a fault 1b. The power stage assigned to PHASE =10d has experienced a fault. Set PHASE =10d, and read this command again for more information.
9	PH10	RW	0b	**Don't care for TPS53676** 0b. The power stage assigned to PHASE =9d has NOT experienced a fault 1b. The power stage assigned to PHASE =9d has experienced a fault. Set PHASE =9d, and read this command again for more information.
8	PH9	RW	0b	**Don't care for TPS53676** 0b. The power stage assigned to PHASE =8d has NOT experienced a fault 1b. The power stage assigned to PHASE =8d has experienced a fault. Set PHASE =8d, and read this command again for more information.
7	PH8	RW	0b	**Don't care for TPS53676** 0b. The power stage assigned to PHASE =7d has NOT experienced a fault 1b. The power stage assigned to PHASE =7d has experienced a fault. Set PHASE =7d, and read this command again for more information.
6	PH7	RW	0b	0b. The power stage assigned to PHASE =6d has NOT experienced a fault 1b. The power stage assigned to PHASE =6d has experienced a fault. Set PHASE =6d, and read this command again for more information.
5	PH6	RW	0b	0b. The power stage assigned to PHASE =5d has NOT experienced a fault 1b. The power stage assigned to PHASE =5d has experienced a fault. Set PHASE =5d, and read this command again for more information.
4	PH5	RW	0b	0b. The power stage assigned to PHASE =4d has NOT experienced a fault 1b. The power stage assigned to PHASE =4d has experienced a fault. Set PHASE =4d, and read this command again for more information.

Table 1-173. Register Field Descriptions (continued)

Bit	Field	Access	Reset	Description
3	PH4	RW	0b	0b. The power stage assigned to PHASE =3d has NOT experienced a fault 1b. The power stage assigned to PHASE =3d has experienced a fault. Set PHASE =3d, and read this command again for more information.
2	PH3	RW	0b	0b. The power stage assigned to PHASE =2d has NOT experienced a fault 1b. The power stage assigned to PHASE =2d has experienced a fault. Set PHASE =2d, and read this command again for more information.
1	PH2	RW	0b	0b. The power stage assigned to PHASE =1d has NOT experienced a fault 1b. The power stage assigned to PHASE =1d has experienced a fault. Set PHASE =1d, and read this command again for more information.
0	PH1	RW	0b	0b. The power stage assigned to PHASE =0d has NOT experienced a fault 1b. The power stage assigned to PHASE =0d has experienced a fault. Set PHASE =0d, and read this command again for more information.

When PHASE is set to a number other than FFh or 80h, the STATUS_PHASES command returns phased fault information for the phyiscal phase referenced by the current When PHASE setting.

(DCh) MFR_SPECIFIC_DC (STATUS_PHASES), PHASE ≠ FFh ≠ 80h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R	RW	RW	R	R	R	R	RW	R
0	0	0	0	0	0	0	0	ISH HI	ISH LO	0	0	0	0	OCL	0

LEGEND: R/W = Read/Write; R = Read only

Table 1-174. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:8	Reserved	R	0	Reserved for future use.
7	ISH HI	RW	0b	ISHARE (higher than IAVG) warning status bit 0b: Condition did NOT occur 1b: Condition has occurred
6	ISH LO	RW	0b	ISHARE (lower than IAVG) warning status bit 0b: Condition did NOT occur 1b: Condition has occurred
5:2	Reserved	R	0	Reserved
1	OCL	RW	0b	Per-phase OCL warning status bit 0b: Condition did NOT occur 1b: Condition has occurred
0	Reserved	R	0	Reserved

1.2.112 (DDh) MFR_SPECIFIC_DD (STATUS_EXTENDED)

CMD Address	DDh
Write Transaction:	Write Block
Read Transaction:	Read Block
Format:	Unsigned Binary (7 bytes)
Paged:	No
Phased:	No
Updates:	On-the-fly
NVM Back-up:	No

STATUS_EXTENDED provides a data block indicating the failure of one or more of the devices non standard fault detection features. All supported bits may be cleared either by CLEAR_FAULTS , or individually by writing 1b to the (DDh) MFR_SPECIFIC_DD (STATUS_EXTENDED) register in their position, per the PMBus 1.3.1 Part II specification section 10.2.4. The (CFh) MFR_SPECIFIC_CF (SMBALERT_MASK_EXTENDED) command provides SMBALERT masking capability.

(DDh) MFR_SPECIFIC_DD (STATUS_EXTENDED) Register Map

55	54	53	52	51	50	49	48
RW	RW	RW	RW	RW	RW	RW	R
IV ACCESS	BAD GRP	RD GRP	CML OTHER	ABORTED	ARB LOST	NACK COUNT	0
47	46	45	44	43	42	41	40
R	R	RW	RW	RW	RW	RW	R
0	0	BYTE NUM SMALL	BYTE NUM BIG	BLK SIZE SMALL	BLK SIZE BIG	LOCKED	0
39	38	37	36	35	34	33	32
RW	RW	RW	RW	R	R	R	R
VSP OPEN CHB	VSP OPEN CHA	VSN OPEN CHB	VSN OPEN CHA	0	0	0	0
31	30	29	28	27	26	25	24
R	R	R	RW	R	RW	RW	RW
0	0	0	SYNC FLT	0	NO UPDATE	IV BOOT	IV ADDR
23	22	21	20	19	18	17	16
R	R	R	R	RW	RW	R	R
0	0	0	0	PH CFG ERR	CFG FILE ERR	0	0
15	14	13	12	11	10	9	8
RW	RW	R	R	R	R	R	R
TAO LOW CHB	TAO LOW CHA	0		0	0	0	0
7	6	5	4	3	2	1	0
R	R	RW	RW	RW	RW	RW	RW
0	0	PRE OVP CHB	PRE OVP CHA	OV TRK CHB	OV TRK CHA	OV FIX CHB	OV FIX CHA

LEGEND: R/W = Read/Write; R = Read only

Table 1-175. Register Field Descriptions

Bit	Field	Access	Reset	Description
55	IV ACCESS	RW	0b	Invalid PMBus Access (attempt to write read-only command) 0b: Condition has NOT occurred. 1b: Condition has occurred.

Table 1-175. Register Field Descriptions (continued)

Bit	Field	Access	Reset	Description
54	BAD GRP	RW	0b	Bad Group Command transaction occurred 0b: Condition has NOT occurred. 1b: Condition has occurred.
53	RD GRP	RW	0b	Group command with READ transaction occurred 0b: Condition has NOT occurred. 1b: Condition has occurred.
52	CML OTHER	RW	0b	A CML error other than those explicitly listed occurred. 0b: Condition has NOT occurred. 1b: Condition has occurred.
51	ABORTED	RW	0b	PMBus Transaction aborted by master 0b: Condition has NOT occurred. 1b: Condition has occurred.
50	ARB LOST	RW	0b	PMBus Data Arbitration Lost 0b: Condition has NOT occurred. 1b: Condition has occurred.
49	NACK COUNT	RW	0b	Master NACK'd Block Size byte. 0b: Condition has NOT occurred. 1b: Condition has occurred.
48:46	Reserved	R	0b	Reserved
45	BYTE NUM SMALL	RW	0b	Too Few bytes received. 0b: Condition has NOT occurred. 1b: Condition has occurred.
44	BYTE NUM BIG	RW	0b	Too Many bytes received . 0b: Condition has NOT occurred. 1b: Condition has occurred.
43	BLK SIZE SMALL	RW	0b	Block Size too small for command . 0b: Condition has NOT occurred. 1b: Condition has occurred.
42	BLK SIZE BIG	RW	0b	Block Size too big for command . 0b: Condition has NOT occurred. 1b: Condition has occurred.
41	LOCKED	RW	0b	Attempted write to write-protected register . 0b: Condition has NOT occurred. 1b: Condition has occurred.
40	Reserved	R	0b	Reserved
39	VSP OPEN CHB	RW	0b	VSP OPEN Channel B . 0b: Condition has NOT occurred. 1b: Condition has occurred.
38	VSP OPEN CHA	RW	0b	VSP OPEN Channel A . 0b: Condition has NOT occurred. 1b: Condition has occurred.
37	VSN OPEN CHB	RW	0b	VSN OPEN Channel B . 0b: Condition has NOT occurred. 1b: Condition has occurred.
36	VSN OPEN CHA	RW	0b	VSN OPEN Channel A . 0b: Condition has NOT occurred. 1b: Condition has occurred.
35:29	Reserved	R	0b	Reserved
28	SYNC FLT	RW	0b	Sync Fault . 0b: Condition has NOT occurred. 1b: Condition has occurred.
27	Reserved	R	0b	Reserved
26	NO UPDATE	RW	0b	UPDATE NOT ALLOWED . 0b: Condition has NOT occurred. 1b: Condition has occurred.

Table 1-175. Register Field Descriptions (continued)

Bit	Field	Access	Reset	Description
24	IV ADDR	RW	0b	Invalid ADDR pin detection . 0b: Condition has NOT occurred. 1b: Condition has occurred.
23:20	Reserved	R	0b	Reserved
19	PH CFG ERR	RW	0b	Invalid PHASE CONFIG . 0b: Condition has NOT occurred. 1b: Condition has occurred.
18	CFG FILE ERR	RW	0b	Invalid Config File . 0b: Condition has NOT occurred. 1b: Condition has occurred.
17:16	Reserved	R	0b	Reserved
15	TAO LOW CHB	RW	0b	TAO Low (channel B) . 0b: Condition has NOT occurred. 1b: Condition has occurred.
14	TAO LOW CHA	RW	0b	TAO Low (channel A) . 0b: Condition has NOT occurred. 1b: Condition has occurred.
13:6	Reserved	R	0b	Reserved
5	PRE OVP CHB	RW	0b	Pre-biased over-voltage fault (Channel B) 0b: Condition has NOT occurred. 1b: Condition has occurred.
4	PRE OVP CHA	RW	0b	Pre-biased over-voltage fault (Channel A) 0b: Condition has NOT occurred. 1b: Condition has occurred.
3	OV TRK CHB	RW	0b	Tracking over-voltage fault (Channel B) 0b: Condition has NOT occurred. 1b: Condition has occurred.
2	OV TRK CHA	RW	0b	Tracking over-voltage fault (Channel A) 0b: Condition has NOT occurred. 1b: Condition has occurred.
1	OV FIX CHB	RW	0b	Fixed over-voltage fault (Channel B) 0b: Condition has NOT occurred. 1b: Condition has occurred.
0	OV FIX CHA	RW	0b	Fixed over-voltage fault (Channel A) 0b: Condition has NOT occurred. 1b: Condition has occurred.

1.2.113 (E0h) MFR_SPECIFIC_E0 (AVSBUS_LOG)

CMD Address	E0h
Write Transaction:	N/A
Read Transaction:	Read Block
Format:	Unsigned Binary (8 bytes)
Paged:	No
Phased:	No
Updates:	N/A
NVM Back-up:	No

Returns a log of recent AVSBus transations with a timestamp. Up to 32 packets are supported. Update the LOG_OFS field in the MFR_SPECIFIC_ED (MISC_OPTIONS) command to index the log. This command is not meaningful for TPS536C7.

(E0h) MFR_SPECIFIC_E0 (AVSBUS_LOG) Register Map

63	62	61	60	59	58	57	56
R	R	R	R	R	R	R	R
RX FRAME							
55	54	53	52	51	50	49	48
R	R	R	R	R	R	R	R
RX FRAME							
47	46	45	44	43	42	41	40
R	R	R	R	R	R	R	R
RX FRAME							
39	38	37	36	35	34	33	32
R	R	R	R	R	R	R	R
RX FRAME							
31	30	29	28	27	26	25	24
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
23	22	21	20	19	18	17	16
R	R	R	R	R	R	R	R
TIME STAMP (Low Byte)							
15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
TIME STAMP							
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
TIME STAMP (High Byte)							

LEGEND: R/W = Read/Write; R = Read only

Table 1-176. Register Field Descriptions

Bit	Field	Access	Reset	Description
63:32	RX FRAME	R	0	AVSBus master frame received by TPS536xx.
31:24	Reserved	R	0	Not used and set to 0.

Table 1-176. Register Field Descriptions (continued)

Bit	Field	Access	Reset	Description
23:0	TIME STAMP	R	0	Relative packet time stamp. Timer rolls over after reaching 24 bits. LSB = 1 µs.

1.2.114 (E3h) MFR_SPECIFIC_E3 (VR_FAULT_CONFIG)

CMD Address	E3h
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	Unsigned Binary (2 bytes)
Paged:	No
Phased:	No
NVM Back-up:	Yes
Updates:	Updates only accepted with power conversion disabled. Note the command may be accepted when PAGE = 00h or 01h, and the other rail is converting power.

Provide limited programmability of which faults assert the VR_FAULT# alert.

(E3h) MFR_SPECIFIC_E3 (VR_FAULT_CONFIG) Register Map

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
R	R	R	R	R	RW	RW	RW
0	0	0	0	0	VR FLT OTF	VR FLT OC	VR FLT CHB

LEGEND: R/W = Read/Write; R = Read only

Table 1-177. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:3	Reserved	R	0	Reserved
2	VR FLT OTF	RW	NVM	0b: VR_FAULT# does NOT assert due to over-temperature faults 1b: VR_FAULT# does assert due to over-temperature faults
1	VR FLT OC	RW	NVM	0b: VR_FAULT# does NOT assert due to over-current faults 1b: VR_FAULT# does assert due to over-current faults
0	VR FLT CHB	RW	NVM	0b: VR_FAULT# asserts due to conditions present only on channel A 1b: VR_FAULT# asserts due to conditions present on channels A and B

1.2.115 (E4h) MFR_SPECIFIC_E4 (SYNC_CONFIG)

CMD Address	E4h
Write Transaction:	Write Block
Read Transaction:	Read Block
Format:	Unsigned Binary (6 bytes)
Paged:	No
Phased:	No
NVM Back-up:	No
Updates:	Updates accepted only with power conversion disabled. Requires NVM store and power cycle to take effect. Note the command may be accepted when PAGE = 00h or 01h, and the other rail is converting power.

Configure options related to input synchronization. Refer to Figure 1-28 for a block diagram of the TPS536xx synchronization options. Configure this command for internal synchronization and closed loop frequency operation when no SYNC pin is assigned.

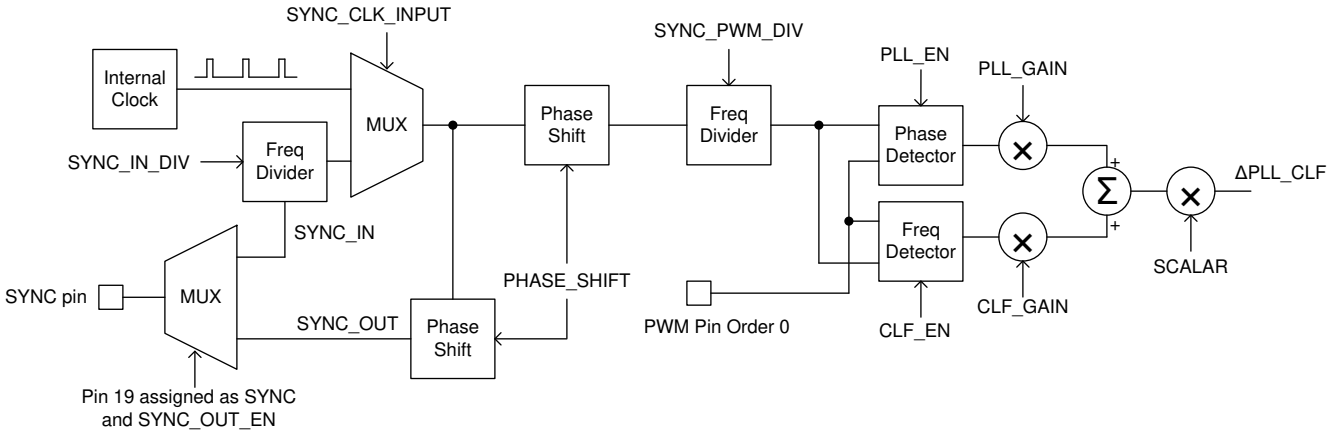

Figure 1-28. SYNC options description (one per channel)

(E4h) MFR_SPECIFIC_E4 (SYNC_CONFIG) Register Map

47	46	45	44	43	42	41	40
RW	RW	RW	RW	RW	RW	RW	RW
SYNC OUT EN	SYNC IN DIV						CLF GAIN CHB
39	38	37	36	35	34	33	32
RW	RW	RW	RW	RW	RW	RW	RW
PLL GAIN CHB		SCALAR CHA			SCALAR CHB		
31	30	29	28	27	26	25	24
RW	RW	RW	RW	RW	RW	RW	RW
PHASE SHIFT CHB				SYNC PWM DIV CHB			
23	22	21	20	19	18	17	16
RW	RW	RW	RW	RW	RW	RW	RW
PHASE SHIFT CHA				SYNC PWM DIV CHA			
15	14	13	12	11	10	9	8
RW	RW	R	RW	RW	RW	RW	RW
PLL GAIN CHA		0	CLF EN CHB	PLL EN CHB	CLF GAIN CHA	CLF EN CHA	PLL EN CHA
7	6	5	4	3	2	1	0

(E4h) MFR_SPECIFIC_E4 (SYNC_CONFIG) Register Map (continued)

RW	RW	RW	R	R	R	R	R
SYNC OUT SEL	SYNC CLK INPUT CHB	SYNC CLK INPUT CHA	0	0	0	0	0

LEGEND: R/W = Read/Write; R = Read only

Table 1-178. Register Field Descriptions

Bit	Field	Access	Reset	Description
47	SYNC OUT EN	RW	NVM	Enable SYNC output 0b: Disabled 1b: Enabled
46:41	SYNC IN DIV	RW	NVM	SYNC in division ratio Value must be 0 to 15d.
40	CLF GAIN CHB	RW	NVM	CLF loop gain channel B 0b: 1.0 1b: 0.5
39:38	PLL GAIN CHB	RW	NVM	PLL loop gain channel B 00b: 1.0 01b: 2.0 10b: 4.0 11b: 8.0
37:35	SCALAR CHA	RW	NVM	Scalar selection for channel A 000b: 1/1 001b: 5/4 010b: 9/8 011b: 17/16 100b: Do not use 101b: 3/4 110b: 7/8 111b: 15/16
34:32	SCALAR CHB	RW	NVM	Scalar selection for channel B 000b: 1/1 001b: 5/4 010b: 9/8 011b: 17/16 100b: Do not use 101b: 3/4 110b: 7/8 111b: 15/16
31:28	PHASE SHIFT CHB	RW	NVM	Phase shift selection for channel B. See the table below.
27:24	SYNC PWM DIV CHB	RW	NVM	SYNC PWM frequency divider channel B 0h to Ah: PWM and Sync divided by 2^(N) Others: Reserved
23:20	PHASE SHIFT CHA	RW	NVM	Phase shift selection for channel A. See the table below.
19:16	SYNC PWM DIV CHA	RW	NVM	SYNC PWM frequency divider channel A 0h to Ah: PWM and Sync divided by 2^(N) Others: Reserved
15:14	PLL GAIN CHA	RW	NVM	PLL loop gain channel A 00b: 1.0 01b: 2.0 10b: 4.0 11b: 8.0
13	Reserved	R	0b	Reserved
12	CLF EN CHB	RW	NVM	CLF loop enable channel B 0b: Disabled 1b: Enabled

Table 1-178. Register Field Descriptions (continued)

Bit	Field	Access	Reset	Description
11	PLL EN CHB	RW	NVM	PLL loop enable channel B 0b: Disabled 1b: Enabled
10	CLF GAIN CHA	RW	NVM	CLF loop gain channel A 0b: 1.0 1b: 0.5
9	CLF EN CHA	RW	NVM	CLF loop enable channel A 0b: Disabled 1b: Enabled
8	PLL EN CHA	RW	NVM	PLL loop enable channel A 0b: Disabled 1b: Enabled
7	SYNC OUT SEL	RW	NVM	0b: SYNC out synchronized to channel A 1b: SYNC out synchronized to channel B
6	SYNC CLK INPUT CHB	RW	NVM	0b: Synchronize to external clock on SYNC pin channel B 1b: Synchronize to internally generated clock channel B
5	SYNC CLK INPUT CHA	RW	NVM	0b: Synchronize to external clock on SYNC pin channel A 1b: Synchronize to internally generated clock channel A
4:0	Reserved	R	0b	Reserved

Table 1-179. Phase shift selections

PHASE SHIFT CHA, PHASE SHIFT CHB	Phase shift (degrees)
0000b	0°
0001b	30°
0010b	60°
0011b	90°
0100b	120°
0101b	150°
0110b	180°
0111b	210°
1000b	240°
1001b	270°
1010b	300°
1011b	330°
1100b	360°
1101b	Reserved
1110b	Reserved
1111b	Reserved

Attempts to write (E4h) MFR_SPECIFIC_E4 (SYNC_CONFIG) to any value outside those specified as valid, are considered invalid/unsupported data and cause TPS536xx to respond by flagging the appropriate status bits, and notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

1.2.116 (EDh) MFR_SPECIFIC_ED (MISC_OPTIONS)

CMD Address	EDh
Write Transaction:	Write Block
Read Transaction:	Read Block
Format:	Unsigned Binary (5 bytes)
Paged:	No
Phased:	No
NVM Backup:	EEPROM
Updates:	on-the-fly

Configure miscellaneous settings.

(EHh) MFR_SPECIFIC_ED (MISC_OPTIONS) Register Map

39	38	37	36	35	34	33	32
RW	RW	RW	RW	RW	RW	RW	RW
AUTO DCM CHA		AUTO DCM CHB		TI ONLY			CALC IIN RD
31	30	29	28	27	26	25	24
RW	RW	RW	RW	RW	RW	RW	RW
CALC IIN FLT	CALC IIN OPT		LOG OFS				
23	22	21	20	19	18	17	16
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
TI ONLY		TRIM EXT		VOTR DOWN CHA		VOTR DOWN CHB	
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
AVSBUS EN CHA	AVSBUS EN CHB	REQ PEC	RST OSD	VOUT SRC CHA		VOUT SRC CHB	

LEGEND: R/W = Read/Write; R = Read only

Table 1-180. Register Field Descriptions

Bit	Field	Access	Reset	Description
39:38	AUTO DCM CHA	RW	NVM	Auto DCM settings for channel A 00b: All phases FCCM 01b: Phase order 0 auto-DCM only 10b: All phases auto-DCM 11b: All phases auto DCM during soft-start only then FCCM
37:36	AUTO DCM CHB	RW	NVM	Auto DCM settings for channel B 00b: All phases FCCM 01b: Phase order 0 auto-DCM only 10b: All phases auto-DCM 11b: All phases auto DCM during soft-start only then FCCM
35:33	TI ONLY	RW	NVM	TI only configuration settings. Do not modify the value of this field.
32	CALCIIN RD	RW	NVM	0b: Report READ_IIN as measured from input current sensor 1b: Report READ_IIN as calculated by the device with assumed power conversion efficiency
31	CALC IIN FLT	RW	NVM	Allow triggering of input current fault based on calculated IIN 0b: Disabled 1b: Enabled

Table 1-180. Register Field Descriptions (continued)

Bit	Field	Access	Reset	Description
30:29	CALC IIN OPT	RW	NVM	00b: Reserved 01b: Report calculated IIN for channel A only 01b: Report calculated IIN for channel B only 01b: Report calculated IIN for channel A+B
28:24	LOG OFS	RW	0	Not meaningful for TPS536C7. Each LSB in this field offsets the MFR_SPECIFIC_E0 (AVSBUS_LOG) command by another 8 bytes.
23:16	Reserved	R	0	Reserved. Set to 0.
15:14	TI ONLY	RW	NVM	TI only configuration settings. Do not modify the value of this field.
13	TRIM EXT	RW	NVM	Extend the range of VOUT_TRIM . Refer to the description of VOUT_TRIM for more information.
11:10	VOTR DOWN CHA	RW	NVM	00b: Downward VOUT_COMMAND transitions on channel A occur at 1.0x VOUT_TRANSITION_RATE 01b: Downward VOUT_COMMAND transitions on channel A occur at 0.5x VOUT_TRANSITION_RATE 10b: Downward VOUT_COMMAND transitions on channel A occur at 0.25x VOUT_TRANSITION_RATE 11b: Downward VOUT_COMMAND transitions on channel A occur at 0.125x VOUT_TRANSITION_RATE
9:8	VOTR DOWN CHB	RW	NVM	00b: Downward VOUT_COMMAND transitions on channel B occur at 1.0x VOUT_TRANSITION_RATE 01b: Downward VOUT_COMMAND transitions on channel B occur at 0.5x VOUT_TRANSITION_RATE 10b: Downward VOUT_COMMAND transitions on channel B occur at 0.25x VOUT_TRANSITION_RATE 11b: Downward VOUT_COMMAND transitions on channel B occur at 0.125x VOUT_TRANSITION_RATE
7	AVSBUS EN CHA	RW	NVM	Global enable for AVSBus on channel A. **Set this bit to 0b for TPS536C7** 0b: Disabled 1b: Enabled
6	AVSBUS EN CHB	RW	NVM	Global enable for AVSBus on channel B. **Set this bit to 0b for TPS536C7** 0b: Disabled 1b: Enabled
5	REQ PEC	RW	NVM	0b: Do NOT require PEC for all PMBus transactions 1b: Require PEC or all PMBus transactions (NACK transactions sent without a PEC byte)
4	RST OSD	RW	NVM	0b: Output voltage does NOT reset to the V_{BOOT} value following a shutdown for any reason. 1b: Output voltage does reset to the V_{BOOT} value following a shutdown for any reason.
3:2	VOUT SRC CHA	RW	NVM	Channel A output voltage bus control NVM setting. This sets the reset value for OPERATION[PAGE=0] only. Hand-off of control is on-the-fly must be done by updating the OPERATION command. **Set this field to 00b for TPS536C7**. 0b: PMBus controls the output voltage. OPERATION[PAGE 0][5:2] is initialized to 0000b. 1b: PMBus controls the output voltage. OPERATION[PAGE 0][5:2] is initialized to 1100b.
1:0	VOUT SRC CHB	RW	NVM	Channel B output voltage bus control NVM setting. This sets the RESET value for OPERATION[PAGE=1] only. Hand-off of control is on-the-fly must be done by updating the OPERATION command. **Set this field to 00b for TPS536C7**. 00b: PMBus controls the output voltage. OPERATION[PAGE 1][5:2] is initialized to 0000b. 10b: PMBus controls the output voltage. OPERATION[PAGE 1][5:2] is initialized to 1100b.

1.2.117 (EEh) MFR SPECIFIC_EE (PIN_DETECT_OVERRIDE)

CMD Address	EEh
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
Paged:	No
Phased:	No
NVM Backup:	EEPROM
Updates:	on-the-fly (pin detection occurs on POR only).

PMBUS specified that NVM (Default or User) stored values will over-write Pin Programmed Values. Setting a “1” in each bit of this register will prevent DEFAULT or USER STORE values from over-writing the Pin-Programmed Value associated that bit.

(EEh) MFR_SPECIFIC_EE (PIN_DETECT_OVERRIDE) Register Map

7	6	5	4	3	2	1	0
R	R	R	RW	R	RW	RW	RW
0	0	0	PD PHASE	0	TI ONLY	PD ADDR	PD BOOT

LEGEND: R/W = Read/Write; R = Read only

Table 1-181. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:5	Reserved	R	0	Reserved. Set to 0.
4	PD PHASE	RW	NVM	**Set this bit to 0b for TPS53676** 0b: At power-up the USER_DATA_03 (PHASE_CONFIG) command will be restored from NVM. 1b: At power-up the USER_DATA_03 (PHASE_CONFIG) command will be restored based on pin detection of the ADDR_CONFIG pin.
3	Reserved	R	0	Reserved. Set to 0.
2	TI ONLY	RW	NVM	TI reserved bit. Do not change the value of this bit.
1	PD ADDR	RW	NVM	0b: At power-up the MFR_SPECIFIC_EF (SLAVE_ADDRESS) command will be restored from NVM. 1b: At power-up the MFR_SPECIFIC_EF (SLAVE_ADDRESS) command will be restored based on pin detection of the ADDR_CONFIG pin.
0	PD BOOT	RW	NVM	0b: At power-up the Channel A V_{BOOT} command will be restored from VOUT_COMMAND NVM. 1b: At power-up the Channel A V_{BOOT} command will be restored based on pin detection of the VBOOT CHA pin.

1.2.118 (EFh) MFR_SPECIFIC_EF (SLAVE_ADDRESS)

CMD Address	EFh
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 bytes)
Paged:	No
Phased:	No
NVM Backup:	EEPROM or pin detection based on MFR_SPECIFIC_EE (PIN_DETECT_OVERRIDE)
Updates:	on-the-fly, only takes effect at power-on.

The SLAVE_ADDRESS command may be used to program or read-back the slave address of digital communication. Note, when a slave address is updated, the TPS536xx does not start responding to the new address immediately.

An NVM store operation must be performed, and TPS536xx will begin responding to the new slave address following the next power-on. Note that these bus addresses are also covered by pin programming. An option in MFR_SPECIFIC_EE (PIN_DETECT_OVERRIDE) allows the user to either use the NVM stored slave address or force a new pin detection at each power-on.

(EFh) MFR_SPECIFIC_EF (SLAVE_ADDRESS) Register Map

7	6	5	4	3	2	1	0
R	RW	RW	RW	RW	RW	RW	RW
0	ADDR PMBUS						

LEGEND: R/W = Read/Write; R = Read only

Table 1-182. Register Field Descriptions

Bit	Field	Access	Reset	Description
6:0	ADDR PMBUS	RW	NVM/ Pinstrap	PMBus Slave address

1.2.119 (F0h) MFR_SPECIFIC_F0 (NVM_CHECKSUM)

CMD Address	F0h
Write Transaction:	NA
Read Transaction:	Read Word
Format:	Unsigned Binary (2 bytes)
Paged:	No
Phased:	No
NVM Back-up:	EEPROM
Updates:	At boot-up, and following NVM Store/Restore operations.

NVM_CHECKSUM reports the CRC-16 (polynomial 0x8005) checksum for the current NVM settings.

(F0h) MFR_SPECIFIC_F0 (NVM_CHECKSUM) Register Map

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
NVM CRC							
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
NVM CRC							

LEGEND: R/W = Read/Write; R = Read only

Table 1-183. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:0	NVM CRC	R	Per NVM Settings	CRC16 for EEPROM settings.

1.2.120 (F5h) MFR_SPECIFIC_F5 (USER_NVM_INDEX)

CMD Address	F5h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
Paged:	No
Phased:	No
NVM Back-up:	No

The MFR_SPECIFIC_F5 command, combined with MFR_SPECIFIC_F6 allows the user to read and write large blocks of user-NVM.

The value of the USER_NVM_INDEX command selects an “index” used for sending/reading 32-byte blocks of user data to the device. The “index” value will auto-increment upon successful receipt of a USER_NVM_EXECUTE command, until the last necessary USER_NVM_EXECUTE has occurred.

(F5h) MFR_SPECIFIC_F5 (USER_NVM_INDEX) – USER MODE Register Map

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
USER_NVM_INDEX							

LEGEND: R/W = Read/Write; R = Read only

Table 1-184. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:0	USER_ NVM_ INDEX	RW	00h	User NVM programming index. When the index = 0, USER_ NVM_ EXECUTE accesses the first 32-byte block of user data, when the index = 1, USER_ NVM_ EXECUTE accesses the second 32-byte block of user data, and so on…

1.2.121 (F6h) MFR_SPECIFIC_F6 (USER_NVM_EXECUTE)

CMD Address	F6h
Write Transaction:	Write Block
Read Transaction:	Read Block
Format:	Unsigned Binary (32 bytes)
Paged:	No
Phased:	No
NVM Back-up:	No

The MFR_SPECIFIC_F6 (USER_NVM_EXECUTE) command, combined with MFR_SPECIFIC_F5 (USER_NVM_INDEX) allows the user to read and write large blocks of user memory for expedited NVM programming in a manufacturing environment. Upon successful write or read of a MFR_SPECIFIC_F6 (USER_NVM_EXECUTE) command, the MFR_SPECIFIC_F5 (USER_NVM_INDEX) is auto-incremented. The block values written to/read from user-NVM are indexed into memory by the MFR_SPECIFIC_F5 (USER_NVM_INDEX) value. This allows the user to program the entire NVM without changing the index value. The following pages describe the mapping of user NVM for each available index.

1.2.122 Raw non-volatile memory programming

TPS53688 has 256 bytes of internal EEPROM non-volatile memory (NVM). Each PMBus command with NVM backup is mapped into the NVM array. For example, if a command supports 16 possible values, there are 4 corresponding bits for that field. The NVM array is designed withstand being overwritten greater than 1,000 times over the lifetime of the device.

The MFR_SPECIFIC_F5 (USER_NVM_INDEX) and MFR_SPECIFIC_F6 (USER_NVM_EXECUTE) commands provide access to read and write the raw data bytes. These commands allow the entire configuration data for the device to be read/written with a minimum number of transactions, to save programming time. The MFR_SPECIFIC_F6 (USER_NVM_EXECUTE) command is a 32 byte block which accesses blocks of raw NVM data. The MFR_SPECIFIC_F5 (USER_NVM_INDEX) command is an auto-incrementing byte command which which selects which 32 bytes of memory are being accessed via the MFR_SPECIFIC_F6 (USER_NVM_EXECUTE) command.

The first 9 bytes of data returned by MFR_SPECIFIC_F6 (USER_NVM_EXECUTE) with index zero, are identifying information for the configuration. Bytes 0 to 6 represent the IC_DEVICE_ID. Bytes 7-8 represent the IC_DEVICE_REV. Byte 9 represents the currently configured PMBus slave address. Replace these bytes with FFh during the write process. The following two bytes, 10 and 11 represent the NVM array CRC value.

The *Fusion Digital Power Designer* software provided for this device is capable of exporting raw configuration data, as well as XML configuration files containing the value of each PMBus command.

Follow the procedures below to read-back and write NVM data for TPS53688 devices.

Procedure: Read all configuration data

1. Configure the device as desired through PMBus commands, then issue STORE_USER_ALL. Power cycle the device or issue RESTORE_USER_ALL with power conversion disabled to ensure operating memory and non-volatile memory bytes are matching.
2. Write the MFR_SPECIFIC_F5 (USER_NVM_INDEX) command to 00h.
3. Read back and record the MFR_SPECIFIC_F6 (USER_NVM_EXECUTE) command (index = 0).
4. Read back and record the MFR_SPECIFIC_F6 (USER_NVM_EXECUTE) command (index = 1).
5. Read back and record the MFR_SPECIFIC_F6 (USER_NVM_EXECUTE) command (index = 2).
6. Read back and record the MFR_SPECIFIC_F6 (USER_NVM_EXECUTE) command (index = 3).
7. Read back and record the MFR_SPECIFIC_F6 (USER_NVM_EXECUTE) command (index = 4).
8. Read back and record the MFR_SPECIFIC_F6 (USER_NVM_EXECUTE) command (index = 5).
9. Read back and record the MFR_SPECIFIC_F6 (USER_NVM_EXECUTE) command (index = 6).
10. Read back and record the MFR_SPECIFIC_F6 (USER_NVM_EXECUTE) command (index = 7).

11. Read back and record the MFR_SPECIFIC_F6 (USER_NVM_EXECUTE) command (index = 8). Note the last 23 bytes of this command are not used by the device. TI recommends replacing these bytes with 00h for consistency across different configurations.

Procedure: Write all configuration data

1. Apply +3.3V to the VCC pin of TPS53688
2. Ensure power conversion is disabled for both channels.
3. Write the MFR_SPECIFIC_F5 (USER_NVM_INDEX) command to 00h.
4. Write the previously recorded MFR_SPECIFIC_F6 (USER_NVM_EXECUTE) (index = 0). Replace the first 9 bytes with FFh.
5. Write the previously recorded MFR_SPECIFIC_F6 (USER_NVM_EXECUTE) (index = 1).
6. Write the previously recorded MFR_SPECIFIC_F6 (USER_NVM_EXECUTE) (index = 2).
7. Write the previously recorded MFR_SPECIFIC_F6 (USER_NVM_EXECUTE) (index = 3).
8. Write the previously recorded MFR_SPECIFIC_F6 (USER_NVM_EXECUTE) (index = 4).
9. Write the previously recorded MFR_SPECIFIC_F6 (USER_NVM_EXECUTE) (index = 5).
10. Write the previously recorded MFR_SPECIFIC_F6 (USER_NVM_EXECUTE) (index = 6).
11. Write the previously recorded MFR_SPECIFIC_F6 (USER_NVM_EXECUTE) (index = 7).
12. Write the previously recorded MFR_SPECIFIC_F6 (USER_NVM_EXECUTE) (index = 8). Replace the last 23 bytes with 00h. An NVM store operation is automatically performed once the last block is successfully received.
13. Wait 100 ms for non-volatile memory programming to complete successfully. Ensure that the +3.3V power supply to the device is not interrupted during this time to guarantee proper memory storage and retention.
14. **Do not** issue an NVM store operation at this point. This will overwrite the NVM array with the data values in operating memory.
15. Power cycle the device or issue RESTORE_USER_ALL to continue operation with the newly programmed values. Note that multifunction pin configurations require a power cycle to take effect.

1.2.123 (FAh) MFR_SPECIFIC_FA (NVM_LOCK)

CMD Address	FAh
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	Unsigned Binary (2 bytes)
Paged:	No
Phased:	No
NVM Back-up:	Yes

The MFR_SPECIFIC_FA command can be optionally used to set a password for NVM programming. To prevent a hacker from simply sending the password command with all possible passwords, the device goes into a special extra-secure state when an incorrect password is received. In this state, all passwords are rejected, even the valid one. The device must be power cycled to clear this state so that another password attempt may be made.

When NVM security is enabled, the MFR_WRITE_PROTECT command determines which write commands are accepted. The most conservative setting disables writes to any command other than PAGE and PHASE , which are necessary for reading certain parameters.

(FAh) MFR_SPECIFIC_FA (NVM_LOCK) Register Map

15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
NVM LOCK							
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
NVM LOCK							

LEGEND: R/W = Read/Write; R = Read only

Table 1-185. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:0	NVM_ LOCK	RW	0000h	See below.

Enabling NVM Security

When security has not yet been enabled or has been disabled, writing to the MFR_SPECIFIC_FA command sets the new password. After the password is set to any value other than FFFFh, security is enabled. After security has been enabled, a STORE_USER_ALL command must be issued to store the security setting after the device is reset

- Set the NVM password. Write MFR_SPECIFIC_FA to a value other than FFFFh.
- Issue STORE_USER_ALL
- Wait 100ms for the NVM store to complete
- Power cycle

Disabling NVM Security

- Write the password MFR_SPECIFIC_FA to temporarily disable NVM security.

Note that NVM security will be re-enabled at the next power-on unless MFR_SPECIFIC_FA command is set to FFFFh and an NVM store operation is performed.

Determining Whether NVM Security is Active

Reads to the MFR_SPECIFIC_FA command returns one of three values:

- 0000h = NVM Security is Disabled
- 0001h = NVM Security is Enabled
- 0002h = MFR_SPECIFIC_FA is locked due to incorrect password entry

Table 1-186. (10h) WRITE_PROTECT, (FBh) MFR_WRITE_PROTECT and (FAh) NVM_LOCK functionality

(FAh) NVM_LOCK	(10h) WRITE_PROTECT	(FBh) MFR_WRITE_PROTECT	Command Access
Writeable Unlocked	Writeable 00h (all commands writeable)	Writeable X (Don't care)	All commands writeable
Writeable Unlocked	Writeable 20h, 40h, 80h	Writeable X (Don't care)	Based on (10h) WRITE_PROTECT
Writeable Unlocked	Writeable 03h	Writeable Per MFR_WRITE_PROTECT command map	Based on (FBh) MFR_WRITE_PROTECT
Writeable Locked	Read-only 00h (all commands writeable)	Read-only X (Don't care)	All commands writeable
Writeable Locked	Read-only 20h, 40h, 80h	Read-only X (Don't care)	Based on (10h) WRITE_PROTECT
Writeable Locked	Read-only 03h	Read-only Per MFR_WRITE_PROTECT command map	Based on (FBh) MFR_WRITE_PROTECT
Read-only (Incorrect Password Issued) Locked	Read-only 00h (all commands writeable)	Read-only X (Don't care)	All commands writeable
Read-only (Incorrect Password Issued) Locked	Read-only 20h, 40h, 80h	Read-only X (Don't care)	Based on (10h) WRITE_PROTECT
Read-only (Incorrect Password Issued) Locked	Read-only 03h	Read-only Per MFR_WRITE_PROTECT command map	Based on (FBh) MFR_WRITE_PROTECT

1.2.124 (FBh) MFR_SPECIFIC_FB (MFR_SPECIFIC_WRITE PROTECT)

CMD Address	FBh
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	Unsigned Binary (2 bytes)
Paged:	No
Phased:	No
NVM Back-up:	Yes

MFR_SPECIFIC_FB (MFR_SPECIFIC_WRITE_PROTECT) provides the user with greater resolution to Write Protect features than the Standard PMBus Function. MFR_SPECIFIC_FB (MFR_SPECIFIC_WRITE_PROTECT) may act in conjunction with MFR_SPECIFIC_FA (NVM_LOCK) or it may be enabled without MFR_SPECIFIC_FA (NVM_LOCK).

(FBh) MFR SPECIFIC FB (MFR SPECIFIC WRITE PROTECT) Register Map

15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
WP ALL	WP WP	WP VOUT	WP CAL	WP OUTFLT	WP INFLT	WP OTHFLT	WP CFG
7	6	5	4	3	2	1	0
RW	RW	RW	R	RW	R	R	R
WP SEQ	WP ONOFF	WP MFR	0	WP DBG	0	WP NVM	0

LEGEND: R/W = Read/Write; R = Read only

Table 1-187. Register Field Descriptions

Bit	Field	Access	Reset	Description
15	WP ALL	RW	NVM	0b: No change. 1b: All writes are rejected, except those needed to read certain parameters, or clear faults. These include: (00h) PAGE, (03h) CLEAR_FAULTS, (04h) PHASE, (1Bh) SMBALERT_MASK, (78h) STATUS_BYTE, (79h) STATUS_WORD, (7Ah) STATUS_VOUT, (7Bh) STATUS_IOUT, (7Ch) STATUS_INPUT, (7Dh) STATUS_TEMPERATURE, (7Eh) STATUS_CML, (80h) STATUS_MFR_SPECIFIC, (CFh) MFR_SPECIFIC_CF (SMBALERT_MASK_EXTENDED), (DCh) MFR_SPECIFIC_DC (STATUS_PHASES), (DDh) MFR_SPECIFIC_DD (STATUS_EXTENDED)
14	WP WP	RW	NVM	0b: No Change 1b: The PMBus std. WRITE_PROTECT is read-only
13	WP VOUT	RW	NVM	0b: No change. 1b: VOUT_COMMAND, VOUT_MARGIN_HIGH, VOUT_MARGIN_LOW are read only.
12	WP CAL	RW	NVM	0b: No change. 1b: Calibration related commands are read-only. These include: (22h) VOUT_TRIM, (38h) IOUT_CAL_GAIN, (39h) IOUT_CAL_OFFSET, (BDh) USER_DATA_13 (MFR_CALIBRATION_CONFIG)
11	WP OUTFLT	RW	NVM	0b: No change. 1b: Output fault commands are read-only. These include: (24h) VOUT_MAX, (2Bh) VOUT_MIN, (40h) VOUT_OV_FAULT_LIMIT, (41h) VOUT_OV_FAULT_RESPONSE, (42h) VOUT_OV_WARN_LIMIT, (43h) VOUT_UV_WARN_LIMIT, (44h) VOUT_UV_FAULT_LIMIT, (45h) VOUT_UV_FAULT_RESPONSE, (46h) IOUT_OC_FAULT_LIMIT, (47h) IOUT_OC_FAULT_RESPONSE, (4Ah) IOUT_OC_WARN_LIMIT, (4Bh) IOUT_UC_FAULT_LIMIT, (4Ch) IOUT_UC_FAULT_RESPONSE, (62h) TON_MAX_FAULT_LIMIT, (63h) TON_MAX_FAULT_RESPONSE

Table 1-187. Register Field Descriptions (continued)

Bit	Field	Access	Reset	Description
10	WP INFLT	RW	NVM	0b: No change. 1b: Input related faults are read-only. These include: (35h) VIN_ON, (36h) VIN_OFF, (55h) VIN_OV_FAULT_LIMIT, (56h) VIN_OV_FAULT_RESPONSE, (57h) VIN_OV_WARN_LIMIT, (58h) VIN_UV_WARN_LIMIT, (59h) VIN_UV_FAULT_LIMIT, (5Ah) VIN_UV_FAULT_RESPONSE, (5Bh) IIN_OC_FAULT_LIMIT, (5Ch) IIN_OC_FAULT_RESPONSE, (5Dh) IIN_OC_WARN_LIMIT, (6Bh) PIN_OP_WARN_LIMIT
9	WP OTHFLT	RW	NVM	0b: No change. 1b: Other fault related commands are read-only. These include: (4Fh) OT_FAULT_LIMIT, (50h) OT_FAULT_RESPONSE, (51h) OT_WARN_LIMIT, (BBh) MFR_PROTECTION_CONFIG
8	WP CFG	RW	NVM	0b: No change. 1b: Configuration related commands are read-only. These include: (20h) VOUT_MODE, (27h) VOUT_TRANSITION_RATE, (28h) VOUT_DROOP, (29h) VOUT_SCALE_LOOP, (33h) FREQUENCY_SWITCH, (B1h) USER_DATA_01 (COMPENSATION_CONFIG), (B2h) USER_DATA_02 (NONLINEAR_CONFIG), (B3h) USER_DATA_03 (PHASE_CONFIG), (B4h) USER_DATA_04 (DVID_CONFIG), (B7h) USER_DATA_07 (PHASE_SHED_CONFIG), (BAh) USER_DATA_10 (ISHARE_CONFIG), (E3h) MFR_SPECIFIC_E3 (VR_FAULT_CONFIG), (E4h) MFR_SPECIFIC_E4 (SYNC_CONFIG), (EDh) MFR_SPECIFIC_ED (MISC_OPTIONS), (EEh) MFR_SPECIFIC_EE (PIN_DETECT_OVERRIDE), (EFh) MFR_SPECIFIC_EF (SLAVE_ADDRESS), (F5h) MFR_SPECIFIC_F5 (USER_NVM_INDEX), (F6h) MFR_SPECIFIC_F6 (USER_NVM_EXECUTE), (CDh) MFR_SPECIFIC_CD (MULTIFUNCITON_PIN_CONFIG)
7	WP SEQ	RW	NVM	0b: No change. 1b: Sequencing commands are read-only These include: (60h) TON_DELAY, (61h) TON_RISE, (64h) TOFF_DELAY, (65h) TOFF_FALL
6	WP ONOFF	RW	NVM	0b: No change. 1b: OPERATION and ON_OFF_CONFIG are read-only
5	WP MFR	RW	NVM	0b: No change. 1b: End-manufacturer-related commands are read-only: (99h) MFR_ID, (9Ah) MFR_MODEL, (9Bh) MFR_REVISION, (9Dh) MFR_DATE
3	WP DBG	RW	NVM	0b: No Change 1b: Test/Debug related commands are read-only.
1	WP NVM	RW	NVM	0b: No Change 1b: NVM related commands are rejected. These include: (11h) STORE_DEFAULT ALL, (12h) RESTORE_DEFAULT ALL, (15h) STORE_USER ALL, (16h) RESTORE_USER ALL
0	Reserved	R	0b	Reserved

Table 1-188. (10h) WRITE_PROTECT, (FBh) MFR_WRITE_PROTECT and (FAh) NVM_LOCK functionality

(FAh) NVM_LOCK	(10h) WRITE_PROTECT	(FBh) MFR_WRITE_PROTECT	Command Access
Writeable Unlocked	Writeable 00h (all commands writeable)	Writeable X (Don't care)	All commands writeable
Writeable Unlocked	Writeable 20h, 40h, 80h	Writeable X (Don't care)	Based on (10h) WRITE_PROTECT
Writeable Unlocked	Writeable 03h	Writeable Per MFR_WRITE_PROTECT command map	Based on (FBh) MFR_WRITE_PROTECT
Writeable Locked	Read-only 00h (all commands writeable)	Read-only X (Don't care)	All commands writeable
Writeable Locked	Read-only 20h, 40h, 80h	Read-only X (Don't care)	Based on (10h) WRITE_PROTECT

Table 1-188. (10h) WRITE_PROTECT, (FBh) MFR_WRITE_PROTECT and (FAh) NVM_LOCK functionality (continued)

(FAh) NVM_LOCK	(10h) WRITE_PROTECT	(FBh) MFR_WRITE_PROTECT	Command Access
Writeable Locked	Read-only 03h	Read-only Per MFR_WRITE_PROTECT command map	Based on (FBh) MFR_WRITE_PROTECT
Read-only (Incorrect Password Issued) Locked	Read-only 00h (all commands writeable)	Read-only X (Don't care)	All commands writeable
Read-only (Incorrect Password Issued) Locked	Read-only 20h, 40h, 80h	Read-only X (Don't care)	Based on (10h) WRITE_PROTECT
Read-only (Incorrect Password Issued) Locked	Read-only 03h	Read-only Per MFR_WRITE_PROTECT command map	Based on (FBh) MFR_WRITE_PROTECT

This page intentionally left blank.

Chapter 2

AVSBus Interface (TPS53676 only)

2.1 AVSBus Interface

The TPS53676 device is designed to be compatible with the timing and physical layer electrical characteristics of the Power Management Bus (PMBus) Specification, part III (AVSBus) revision 1.3.1 available at http://pmbus.org. AVS_VDDIO and logic levels of 1.14 V to (VCC pin voltage, 3.6 V maximum) are supported. Clock operation up to 50 MHz is supported. TPS53676 requires approximately 14 ns (maximum) from a clock edge to a transition of the AVS_SDATA pin, and at very high-frequency operation, it may be necessary to increase the clock high time (t_{high}) to compensate. Refer to the *technical reference manual* for more information.

The AVSBus communication interface is similar to the *de-facto* Serial Peripheral Interface (SPI) standard with the following configuration:

- No chip select (CSO#) pin is used. AVSBus is a point-to-point protocol.
- AVS_CLK idles LOW
- AVS_MDATA and AVS_SDATA idle HIGH
- A transmitter launches data on the rising edge of AVS_CLK
- A receiver captures data on the falling edge of AVS_CLK
- MSB transmitted first

Refer to to the PMBus specification revision 1.3.1, part III for more information.

To enable AVSBus control in the device:

- Ensure the AVSBUS EN CHA / AVSBUS EN CHB options in the MISC_OPTIONS PMBus command are set to 1b in NVM.
- Set the value of VOUT SRC CHA / VOUT SRC CHB to 10b in NVM. This setting in itself only sets the default value of the OPERATION command bits 5:2.
- Set the OPERATION[5:2] bits to 1100b to hand-off output voltage control to the AVSBus Interface.

Note

Transferring output voltage control from PMBus to AVSBus during power conversion causes the output voltage to transition to a low value, until the host issues the next AVSBus voltage command. Internal architecture limitations determine this behavior. As a result, while output voltage control may be changed without a power cycle, TI recommends that changes between PMBus and AVSBus control occur without power conversion being active.

2.2 AVSBus transaction types

Supported AVSBus Commands

The table below summarizes the AVS command transactions supported by TPS53676.

Description	Select [3:0]	Cmd Group [0]	Cmd Type [3:0]	Access Cmd[1:0]	Data Format [15:0]
Vout Set or Read the voltage target	0000b: Channel A 0001b: Channel B 1111b: Broadcast	0b Standard	0000b Voltage	00b: Read 01b: Write and hold 11b: Write and commit	Direct Format 1 mV per LSB
Slew Rate Set or Read the rising and falling DVID slew rates	0000b: Channel A 0001b: Channel B 1111b: Broadcast	0b Standard	0001b Vout Transition Rate	00b: Read 01b: Write and hold 11b: Write and commit	Direct Format 1 mV / µs per LSB
Current Set or Read the output current	0000b: Channel A 0001b: Channel B	0b Standard	0010b Read Current	00b: Read	Direct Format 10 mA per LSB
Temperature Set or Read the current power stage temperature	0000b: Channel A 0001b: Channel B	0b Standard	0011b Read Temperature	00b: Read	Direct Format 0.1°C per LSB
Reset Reset the channel to its VBOOT	0000b: Channel A 0001b: Channel B 1111b: Broadcast	0b Standard	0100b Voltage Reset	01b: Write and hold 11b: Write and commit	Data-less. Use 0000h in AVS_MDATA frame
Power Mode	Not supported - Ack and do nothing.				
AVSBus Status	0000b: Channel A 0001b: Channel B 1111b: Broadcast	0b Standard	1110b Status	00b: Read 01b: Write and hold 11b: Write and commit	See register description. Write 1b to clear.
AVSBus Version Read	1111b: All channels	0b Standard	1111b Version Read	00b: Read	0000b v1.3.1 part III

AVSBus frame and sub-fields

The figures below describe the AVSBus frame structure

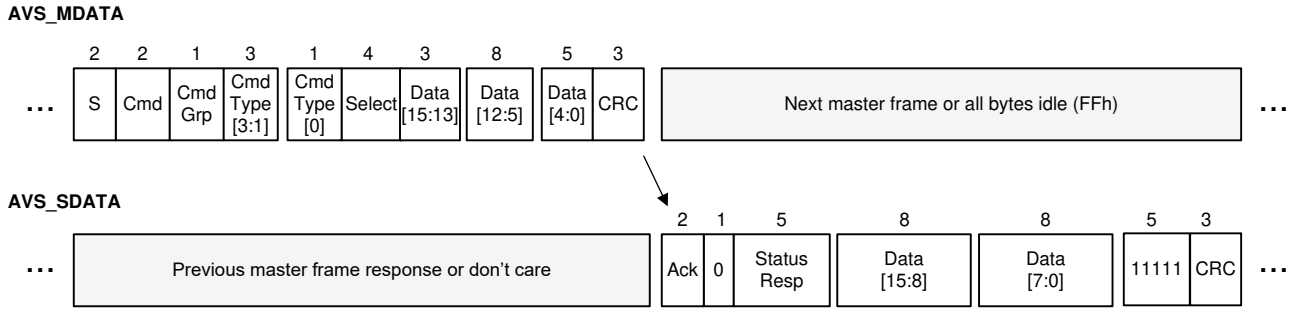

Figure 2-1. AVSBus frame structure

Table 2-1.

Frame index	Field	Length (bits)	Description
AVS_MDATA 31:30	S	2	Start condition 01b
AVS_MDATA 29:28	Cmd	2	Read / Write 11b: Read 01b: Write and Hold 00b: Write and Commit
AVS_MDATA 27	Cmd Group	1	0b: AVSBus standard commands 1b: MFR Specific commands (none supported by TPS53676)
AVS_MDATA 26:23	Cmd Type	4	0000b: Vout 0001b: Vout Transition Rate 0010b: Current Read 0011b: Temperature Read 0100b: Reset Vout 1110b: AVS Status 1111b: AVS Version
AVS_MDATA 22:19	Select	4	0000b: Channel A 0001b: Channel B 1111b: All channels (valid only for Status and Version commands)
AVS_MDATA 18:3	AVS_MDATA Data	16	Read Transactions: FFFFh Write Transactions: per command data format.
AVS_MDATA 2:0	AVS_MDATA CRC	3	CRC of AVS_MDATA frame. Polynomial $x^3 + x^1 + x^0$
AVS_SDATA 31:30	Ack	2	00b: Good CRC, valid data 01b: Good CRC, no action taken due to resource busy. 10b: Bad CRC, no action is taken 11b: Good CRC, but invalid selector, command, data...
AVS_SDATA 29	Reserved	1	Set to 0b always
AVS_SDATA 28:24	StatusResp	5	Bit 4: 1b if Vout is settled Bit 3: 1b if any status warning bits are set Bit 2: 1b is AVSBus has control of the output Bit 1: 1b if RESET# is LOW, 0b otherwise Bit 0: Set to 0b.
AVS_SDATA 23:8	AVS_SDATA Data	16	Writes: Don't care Reads: Per command format
AVS_SDATA 7:3	Reserved	5	Reserved and set to 11111b
AVS_SDATA 2:0	AVS_SDATA CRC	3:0	CRC of AVS_SDATA frame. Polynomial $x^3 + x^1 + x^0$

2.3 Example AVSBus Frames

A few example AVSBus frames frames are listed below:

Example: Set the target voltage for channel A to 0.80 V

The AVS_MDATA frame 40 00 19 07h corresponds to:

- Start = 01b (Valid start condition)
- Cmd = 00b (Write and commit)
- Cmd Group = 0b (AVSBus standard commands)
- Cmd Type = 0000b (Vout)
- Select = 0000b (Channel A)
- Data = 0000 0011 0010 0000b (800d = 800 mV)
- AVS_MDATA CRC = 111b (Valid CRC for the preceeding 29 bits)

The AVS_SDATA frame in response 04 FF FF FF FFh corresponds to:

- Ack = 00b (Good CRC, valid data)
- Reserved = 0b
- StatusResp = 00100b (AVSBus has control, No status bits, Vdone=0 due to new voltage command)
- Data = 1111 1111 1111 1111b (fill with 1's for write)
- AVS_SDATA CRC = 111b (Valid CRC for the preceeding 29 bits)

Example: Read the output current telemetry from channel A

The AVS_MDATA frame 71 07 FF F9h corresponds to:

- Start = 01b (Valid start condition)
- Cmd = 11b (Read)
- Cmd Group = 0b (AVSBus standard commands)
- Cmd Type = 0010b (Vout)
- Select = 0000b (Channel A)
- Data = 1111 1111 1111 1111b (fill with 1's for read)
- AVS_MDATA CRC = 001b (Valid CRC for the preceeding 29 bits)

The AVS_SDATA frame in response 14 10 86 F8h corresponds to:

- Ack = 00b (Good CRC, valid data)
- Reserved = 0b
- StatusResp = 10100b (Vdone=1, AVSBus has control, No status bits)
- Data = 0001 0000 1000 0110b (4230d = 42.3 A)
- AVS_SDATA CRC = 000b (Valid CRC for the preceeding 29 bits)

2.4 Example AVSBus number format conversions

All AVSBus transactions use the DIRECT number format.

Example: Encode or decode output voltage targets (unsigned, 1 mV / LSB)

Encode 1.000 V = 1.0 V × (1 LSB / 1 mV) = 1000d = 03E8h

Decode 0400h = 1024d × (1 mV / LSB) = 1.024 V

Example: Decode output current telemetry (unsigned, 10 mA / LSB)

Decode 1043h = 4163d × (10 mA / LSB) = 41.63 A

Example: Decode power stage temperature telemetry (signed, 0.1°C / LSB)

Decode 0358h = 856d × (0.1°C / LSB) = 85.6°C

Decode FF62h = -158d × (0.1°C / LSB) = -15.8°C

Example: Encode or decode slew rate settings (unsigned, 1 mV/µs / LSB)

The 16 bit data value for slew rate is divided into 8 bits for Rising and 8 bits for falling slew rate.

Encode Rising = Falling = (5 mV/µs × [1 LSB / 1 mV/µs]) = 05 05h

Decode 0A 02h:

- Rising = 0Ah = 10d × (1 mV/µs / LSB) = 10 mV/µs
- Falling = 02h = 2d × (1 mV/µs / LSB) = 2 mV/µs

2.5 AVSBus Command Descriptions

2.5.1 (0h) AVSBus Output Voltage

Cmd Type:	0000b
Access:	Read / Write
Data Format:	Direct, 16-bits, 1 mV per LSB (unsigned)
Select:	0h: Channel A 1h: Channel B Fh: Broadcast
Reset Value:	Initialized based on VOUT COMMAND from PMBus
Supported Values:	Values will be clamped to the values of VOUT_MIN and VOUT_MAX from PMBus
Description:	Get or set the current output voltage target. Reading this command returns the voltage *target*, and not the measured value.

2.5.2 (1h) AVSBus Transition Rate

Cmd Type:	0001b
Access:	Read / Write
Data Format:	Direct, 16 bits, 1 mV/µs per LSB (unsigned) 8 MSB bits for rising transition rate, 8 LSB bits for falling transition rate
Select:	0h: Channel A 1h: Channel B Fh: Broadcast
Reset Value:	Initialized based on VOUT_TRANSITION_RATE from PMBus
Supported Values:	1 mV/µs to 40 mV/µs
Description:	Get or set the current output slew rate. Rising and falling slew rates are independent. When commanded through AVSBus, the output voltage slew rate is slightly slower (nominally -5%) than when commanded through PMBus.

2.5.3 (2h) AVSBus Output Current

Cmd Type:	0010b
Access:	Read
Data Format:	Direct, 16 bits, 10 mA per LSB (unsigned)
Select:	0h: Channel A 1h: Channel B
Reset Value:	Current status
Supported Values:	0.0 to 327.67 A (MSB bit of AVSbus is always 0b).
Description:	Returns the measured output current value for the channel.

2.5.4 (3h) AVSBus Temperature

Cmd Type:	0011b
Access:	Read
Data Format:	Direct, 16 bits, 0.1 °C per LSB (signed)
Select:	0h: Channel A 1h: Channel B
Reset Value:	Current status
Supported Values:	-40.0 to 150.0 °C
Description:	Returns the measured power stage temperature for the channel.

2.5.5 (4h) AVSBus Reset Voltage

Cmd Type:	0100b
Access:	Write
Data Format:	Data-less. Send 0000h in data field for AVS_MDATA field.
Select:	0h: Channel A 1h: Channel B Fh: Broadcast
Reset Value:	N/A
Supported Values:	N/A
Description:	Resets the selected channel to their VBOOT voltages, whether determined by NVM or pinstrapping.

2.5.6 (5h) AVSBus Power Mode

Cmd Type:	0101b

Access:	Read / Write
Data Format:	Not supported.
Select:	0h: Channel A 1h: Channel B Fh: Broadcast
Reset Value:	0000h
Supported Values:	N/A
Description:	Command is accessible, but TPS53676 takes no action based on writes.

2.5.7 (Eh) AVSBus Status

Cmd Type:	1110b
Access:	Read / Write
Data Format:	Not supported.
Select:	0h: Channel A 1h: Channel B Fh: Broadcast
Reset Value:	0000h
Supported Values:	Write 1b to clear.
Description:	See *AVSBus fault and warning behavior*.

2.5.8 (Fh) AVSBus Version

Cmd Type:	1111b
Access:	Read
Data Format:	Direct, 16 bits, unsigned binary
Select:	Fh: Broadcast
Reset Value:	0000h (v1.3.1 part III)
Supported Values:	Write 1b to clear.
Description:	Returns the supported AVSBus Version

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265