UCD90320UEVM-032 32-Rail Sequencer Development Board

This user's guide describes the UCD90320U sequencer development board (UCD90320UEVM-032). The test setup and software setup are detailed and test procedures are outlined. Also included in this document are the schematics, and bill of materials (BOM).

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1 Introduction[1][2]

The UCD90320U device is a 32-rail PMBus power sequencer and system manager. It can sequence, monitor and margin 32 voltage rails; monitor and respond to user-defined faults such as OV, UV, OC, UC, temperature, time-out, and GPI-triggered faults; provide flexible configurations such as sequence-on and sequence-off dependencies, delay time, and Boolean logic; store fault logs into nonvolatile memory; and integrate value-added features such as watchdog, system reset, cascading and sync clock.

2 Description

The UCD90320UEVM-032 contains a UCD90320U device, two step-down power stages using the TPS54678 synchronous step-down switcher with integrated FET (SWIFT™), two TPS7A84 LDOs, a TPS73633 LDO, and a REF5030A voltage reference. Access to all of the I/O pins is provided via strip connectors for integration into complex systems using jumper wires. The UCD90320U EVM provides PMBus (power management bus) communication port. Microsoft® Windows ® based host computers can monitor, control, and configure the UCD90320U device using a USB interface adapter EVM (HPA172) and TI fusion digital power designer graphical user interface (GUI).

2.1 Typical Applications

This EVM is used in the following applications:

- Industrial ATE
- Telecom
- Networking equipment
- Servers
- Storage systems
- Any system requiring sequencing and monitoring of multiple power rails

2.2 Features

The EVM has the following features:

- Powered by single 5-V supply
- Status LEDs on all digital I/O pins
- Strip connector I/O access
- Headers with pull-up and pull-down configurations
- PMBus interface for configuration and monitoring

(1) SWIFT is a trademark of Texas Instruments.
(2) Microsoft, Windows are registered trademarks of Microsoft Corporation.

3 Electrical Performance Specifications

Table 1 lists the EVM electrical performance specifications.

Table 1. UCD90320UEVM-032 Electrical Performance Specifications

Parameter	Test Conditions	MIN	TYP	MAX	Units
Input power					
Input voltage range		4.5	5	5.5	V
Input current	All LEDs and power converters are on. No external load current on I/O pins or power converters.	166	167	169	mA
LDO and Step-down Converter for Margining Function Demonstration					
Output voltage	Normal operation, not in margin mode		1.2		V
Output current	Each LDO or step-down converter.			3	A
Analog Input					
Analog input voltage range	Use internal reference	0	-	3.3	V
Analog input voltage range	Use external reference	0	-	3	V
Digital inputs and outputs					
I/O high-level input voltage(1)		2.15	-	5.5	V
I/O low-level input voltage		0	-	1.15	V
I/O input hysteresis		0.2	-	-	V
I/O high-level output voltage	Load current (source) = –4 mA	2.4	-	-	V
I/O low-level output voltage	Load current (sink) = 4 mA	-	-	0.4	V

(1) Maximum input voltage for PMBUS_CNTRL, PMBALERT#, MAR19 and MAR20 pins are V33D + 0.3 V.

4 Schematic

Figure 1 illustrates the EVM board.

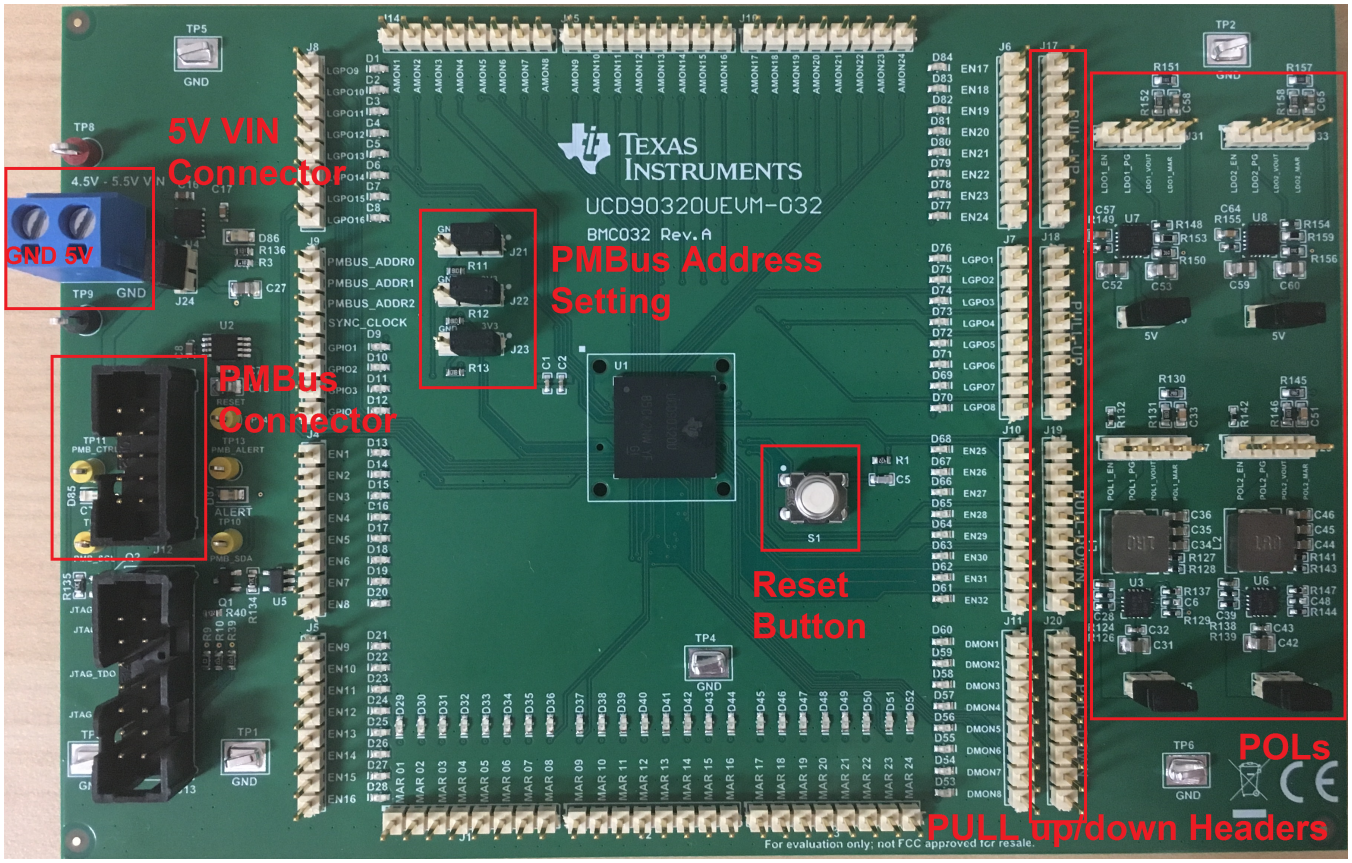


Figure 1. UCD90320UEVM-032

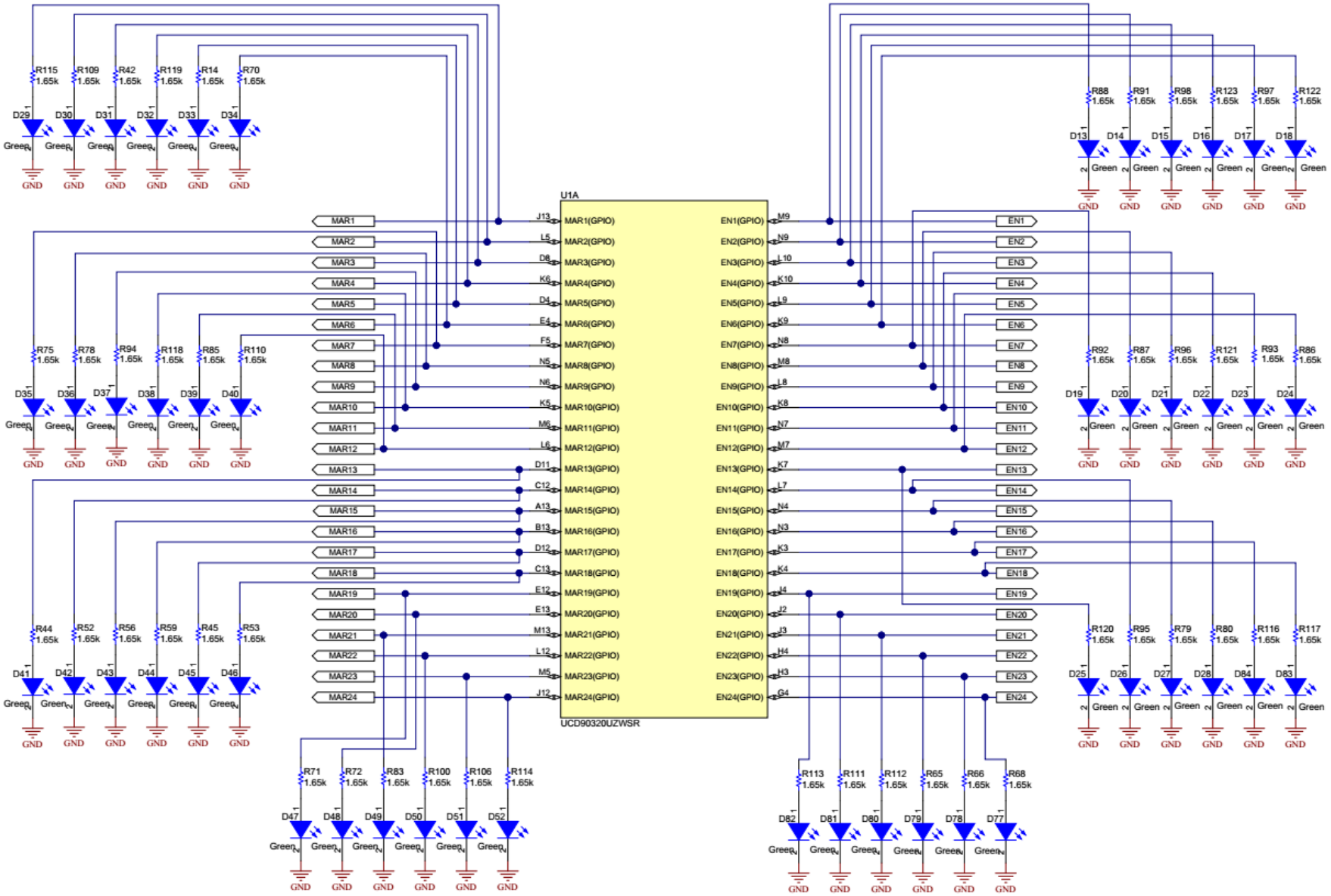


Figure 2. UCD90320UEVM-032 Schematic (1 of 6)

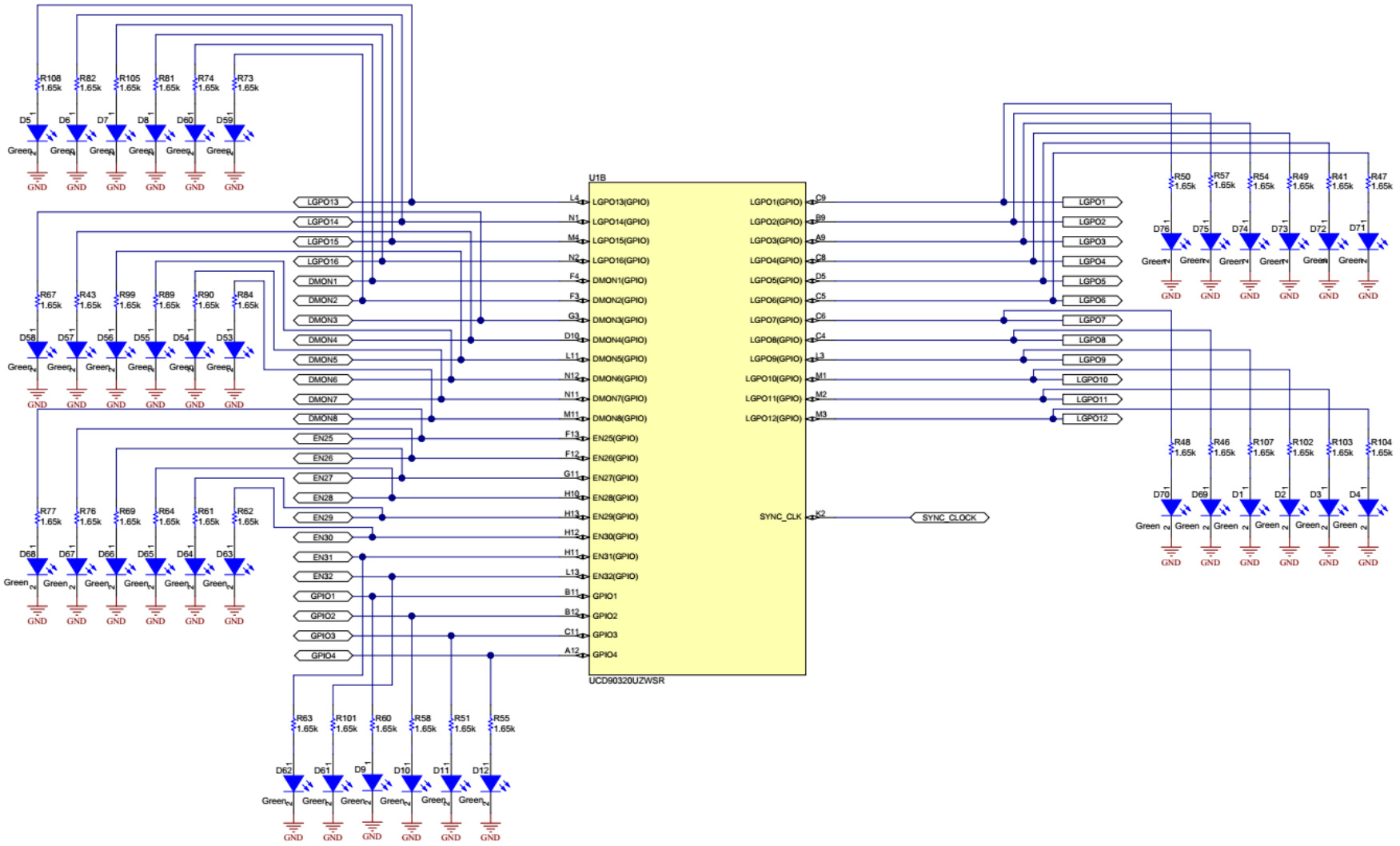


Figure 3. UCD90320UEVM-032 Schematic (2 of 6)

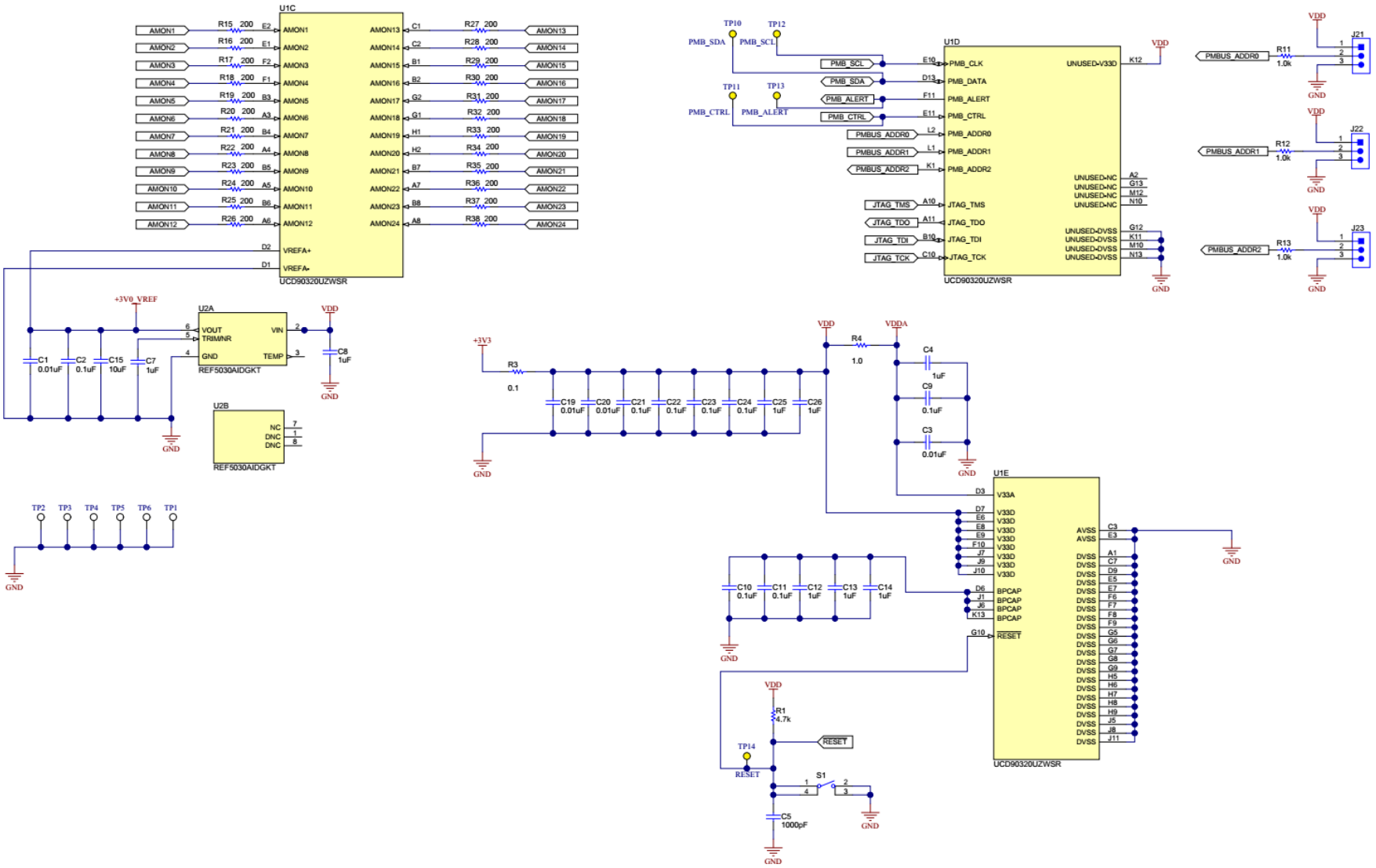


Figure 4. UCD90320UEVM-032 Schematic (3 of 6)

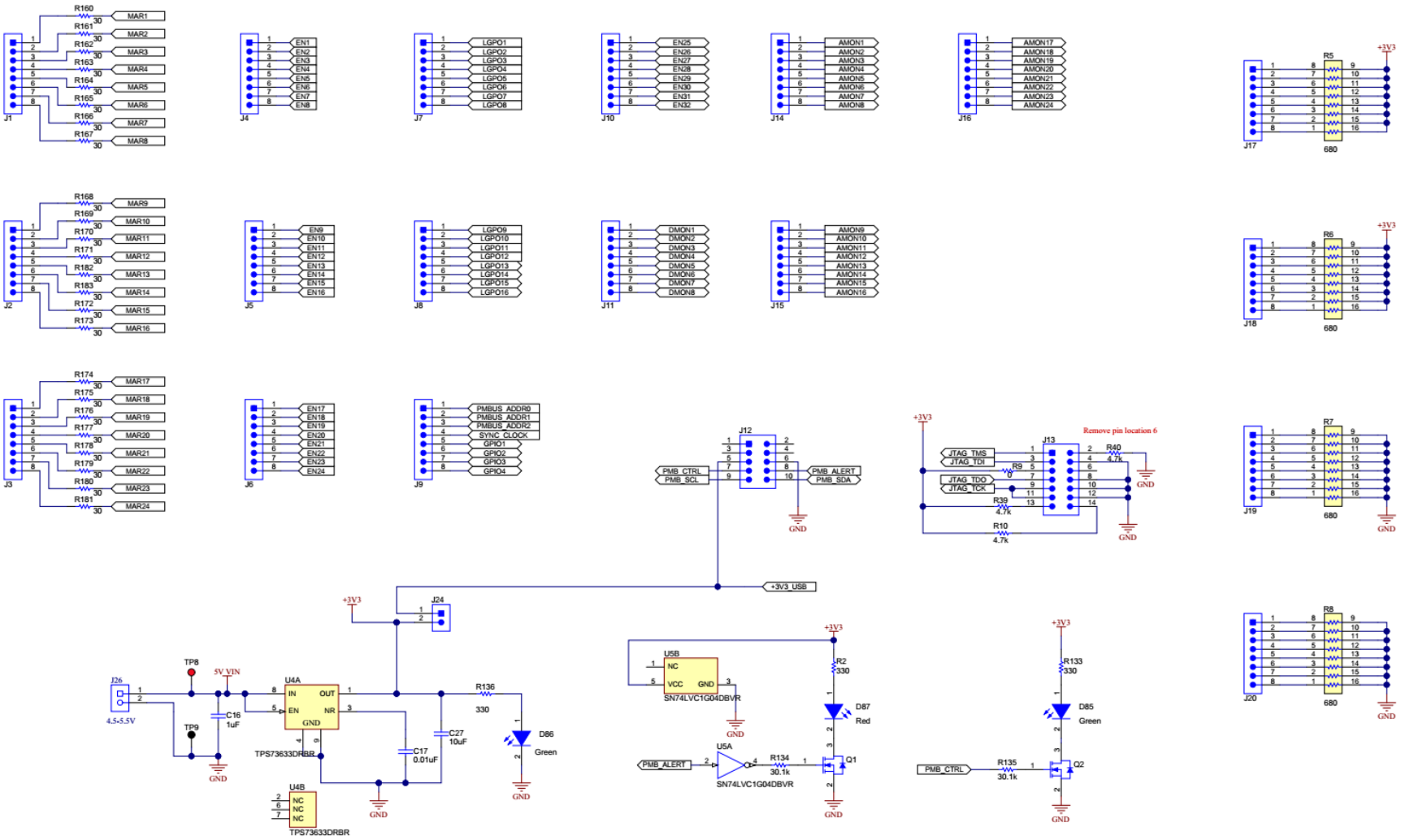


Figure 5. UCD90320UEVM-032 Schematic (4 of 6)

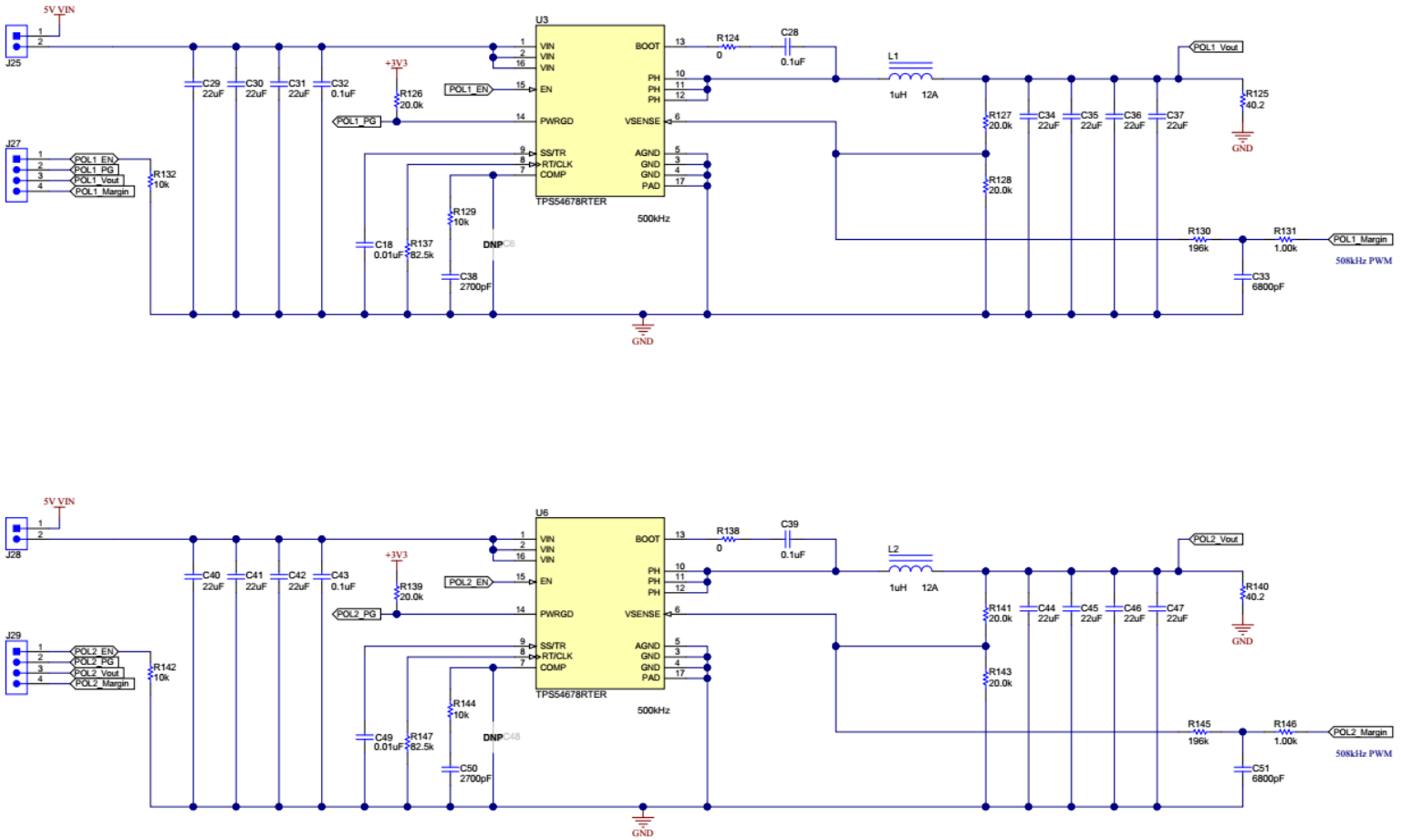


Figure 6. UCD90320UEVM-032 Schematic (5 of 6)

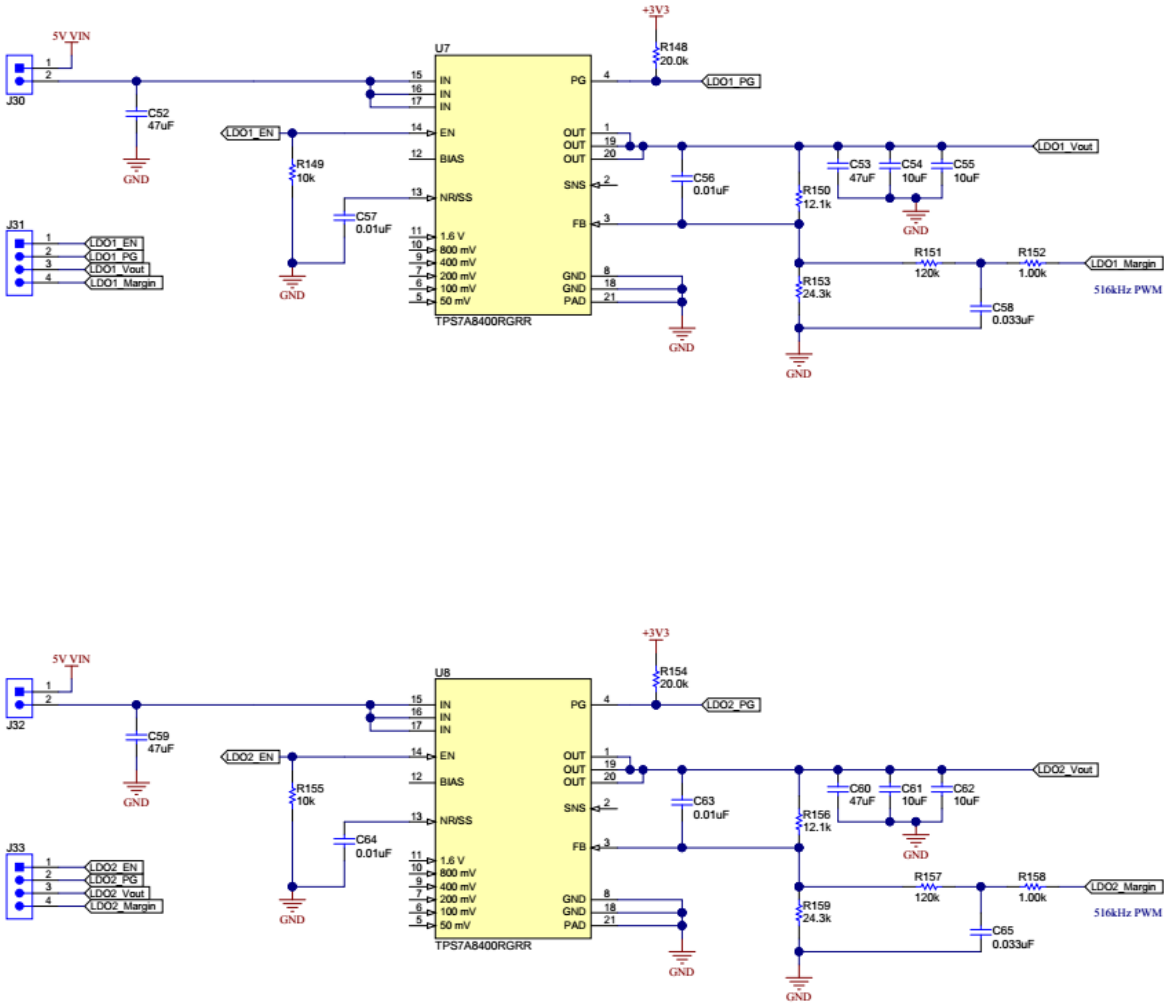


Figure 7. UCD90320UEVM-032 Schematic (6 of 6)

5 Test Setup

5.1 Test Equipment

The following test equipment is recommended when using the EVM:

Voltage Source: One 5-volt power supply with at least 0.5A sourcing capability.
Multimeters: One volt-meter
Output Load: None
Oscilloscope: Optional
Fan: None
Recommended Wire Gauge: AWG24 or thicker
Recommended PC platform: Windows 7 64-bit with 8GB RAM
USB Interface Adapter EVM (USB-to-GPIO): HPA172
The latest version Fusion Digital Power Designer software can be downloaded at the following link to the Texas Instruments website:
http://focus.ti.com/docs/toolsw/folders/print/fusion_digital_power_designer.html

5.2 Recommended Test Setup

Figure 8 illustrates the recommended test setup.

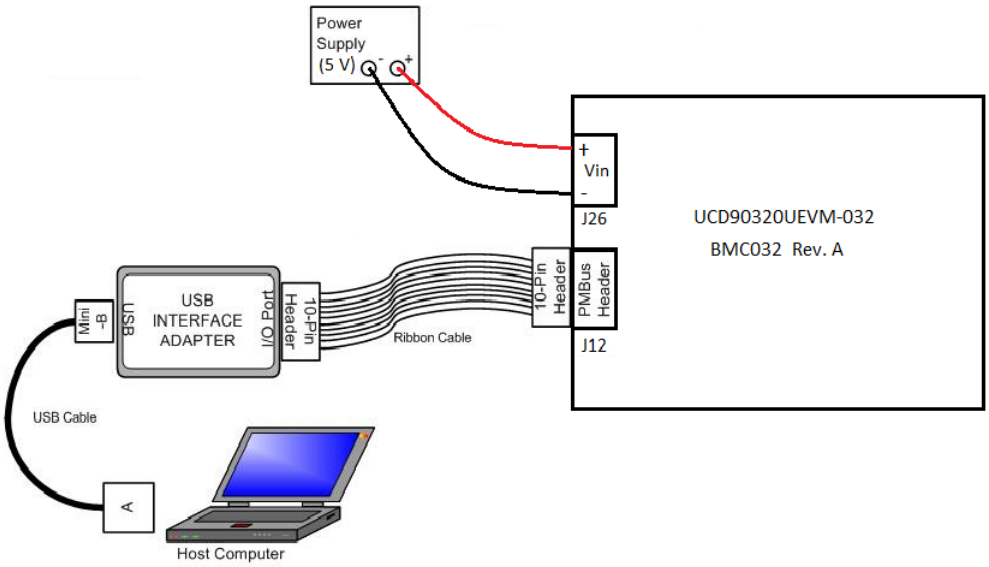


Figure 8. UCD90320UEVM-032 Recommended Test Setup

5.3 List of Connectors and Functions

Table 2 lists the connectors and their functions.

Table 2. Connector Definitions

Connectors	Pins	Name	Description
J1	1	MAR01	Margin PWM output or GPIO
	2	MAR02	Margin PWM output or GPIO
	3	MAR03	Margin PWM output or GPIO
	4	MAR04	Margin PWM output or GPIO
	5	MAR05	Margin PWM output or GPIO
	6	MAR06	Margin PWM output or GPIO
	7	MAR07	Margin PWM output or GPIO
	8	MAR08	Margin PWM output or GPIO
J2	1	MAR09	Margin PWM output or GPIO
	2	MAR10	Margin PWM output or GPIO
	3	MAR11	Margin PWM output or GPIO
	4	MAR12	Margin PWM output or GPIO
	5	MAR13	Margin PWM output or GPIO
	6	MAR14	Margin PWM output or GPIO
	7	MAR15	Margin PWM output or GPIO
	8	MAR16	Margin PWM output or GPIO
J3	1	MAR17	Margin PWM output or GPIO
	2	MAR18	Margin PWM output or GPIO
	3	MAR19	Margin PWM output or GPIO
	4	MAR20	Margin PWM output or GPIO
	5	MAR21	Margin PWM output or GPIO
	6	MAR22	Margin PWM output or GPIO
	7	MAR23	Margin PWM output or GPIO
	8	MAR24	Margin PWM output or GPIO
J4	1	EN1	Rail enable output or GPIO
	2	EN2	Rail enable output or GPIO
	3	EN3	Rail enable output or GPIO
	4	EN4	Rail enable output or GPIO
	5	EN5	Rail enable output or GPIO
	6	EN6	Rail enable output or GPIO
	7	EN7	Rail enable output or GPIO
	8	EN8	Rail enable output or GPIO
J5	1	EN9	Rail enable output or GPIO
	2	EN10	Rail enable output or GPIO
	3	EN11	Rail enable output or GPIO
	4	EN12	Rail enable output or GPIO
	5	EN13	Rail enable output or GPIO
	6	EN14	Rail enable output or GPIO
	7	EN15	Rail enable output or GPIO
	8	EN16	Rail enable output or GPIO
J6	1	EN17	Rail enable output or GPIO
	2	EN18	Rail enable output or GPIO
	3	EN19	Rail enable output or GPIO
	4	EN20	Rail enable output or GPIO
	5	EN21	Rail enable output or GPIO
	6	EN22	Rail enable output or GPIO
	7	EN23	Rail enable output or GPIO
	8	EN24	Rail enable output or GPIO

Table 2. Connector Definitions (continued)

Connectors	Pins	Name	Description
J7	1	LGPO1	Logic GPO output or GPIO
	2	LGPO2	Logic GPO output or GPIO
	3	LGPO3	Logic GPO output or GPIO
	4	LGPO4	Logic GPO output or GPIO
	5	LGPO5	Logic GPO output or GPIO
	6	LGPO6	Logic GPO output or GPIO
	7	LGPO7	Logic GPO output or GPIO
	8	LGPO8	Logic GPO output or GPIO
J8	1	LGPO9	Logic GPO output or GPIO
	2	LGPO10	Logic GPO output or GPIO
	3	LGPO11	Logic GPO output or GPIO
	4	LGPO12	Logic GPO output or GPIO
	5	LGPO13	Logic GPO output or GPIO
	6	LGPO14	Logic GPO output or GPIO
	7	LGPO15	Logic GPO output or GPIO
	8	LGPO16	Logic GPO output or GPIO
J9	1	PMBUS_ADDR0	PMBus address pin
	2	PMBUS_ADDR1	PMBus address pin
	3	PMBUS_ADDR2	PMBus address pin
	4	SYNC_CLOCK	Sync Clock pin
	5	GPIO1	General Purpose I/O
	6	GPIO2	General Purpose I/O
	7	GPIO3	General Purpose I/O
	8	GPIO4	General Purpose I/O
J10	1	EN25	Rail enable output or GPIO
	2	EN26	Rail enable output or GPIO
	3	EN27	Rail enable output or GPIO
	4	EN28	Rail enable output or GPIO
	5	EN29	Rail enable output or GPIO
	6	EN30	Rail enable output or GPIO
	7	EN31	Rail enable output or GPIO
	8	EN32	Rail enable output or GPIO
J11	1	DMON1	Digital monitor input or GPIO
	2	DMON2	Digital monitor input or GPIO
	3	DMON3	Digital monitor input or GPIO
	4	DMON4	Digital monitor input or GPIO
	5	DMON5	Digital monitor input or GPIO
	6	DMON6	Digital monitor input or GPIO
	7	DMON7	Digital monitor input or GPIO
	8	DMON8	Digital monitor input or GPIO
J12	1		No connection
	2		No connection
	3		No connection
	4		No connection
	5	+3V3_USB	3.3-V power provided by USB interface adapter EVM
	6	GND	PMBus GND
	7	PMB_CTRL	PMBus CONTROL line
	8	PMB_ALERT	PMBus ALERT# line
	9	PMB_SCL	PMBus Clock
	10	PMB_SDA	PMBus Data
J13	1	JTAG_TMS	JTAG TMS

Table 2. Connector Definitions (continued)

Connectors	Pins	Name	Description
	2		JTAG nTRST (unused)
	3	JTAG_TDI	JTAG TDI
	4		JTAG TDIS (unused)
	5		JTAG VTRef (unused)
	6		JTAG KEY
	7	JTAG_TDO	JTAG TDO
	8	GND	JTAG GND
	9		JTAG RTCK (unused)
	10	GND	JTAG GND
	11	JTAG_TCK	JTAG TCK
	12	GND	JTAG GND
	13		JTAG EMU0 (unused)
	14		JTAG EMU1 (unused)
J14	1	AMON1	Analog monitor input
	2	AMON2	Analog monitor input
	3	AMON3	Analog monitor input
	4	AMON4	Analog monitor input
	5	AMON5	Analog monitor input
	6	AMON6	Analog monitor input
	7	AMON7	Analog monitor input
	8	AMON8	Analog monitor input
J15	1	AMON9	Analog monitor input
	2	AMON10	Analog monitor input
	3	AMON11	Analog monitor input
	4	AMON12	Analog monitor input
	5	AMON13	Analog monitor input
	6	AMON14	Analog monitor input
	7	AMON15	Analog monitor input
	8	AMON16	Analog monitor input
J16	1	AMON17	Analog monitor input
	2	AMON18	Analog monitor input
	3	AMON19	Analog monitor input
	4	AMON20	Analog monitor input
	5	AMON21	Analog monitor input
	6	AMON22	Analog monitor input
	7	AMON23	Analog monitor input
	8	AMON24	Analog monitor input
J17	1		Pull-up signal (can be used as GPI input)
	2		Pull-up signal (can be used as GPI input)
	3		Pull-up signal (can be used as GPI input)
	4		Pull-up signal (can be used as GPI input)
	5		Pull-up signal (can be used as GPI input)
	6		Pull-up signal (can be used as GPI input)
	7		Pull-up signal (can be used as GPI input)
	8		Pull-up signal (can be used as GPI input)
J18	1		Pull-up signal (can be used as GPI input)
	2		Pull-up signal (can be used as GPI input)
	3		Pull-up signal (can be used as GPI input)
	4		Pull-up signal (can be used as GPI input)
	5		Pull-up signal (can be used as GPI input)
	6		Pull-up signal (can be used as GPI input)

Table 2. Connector Definitions (continued)

Connectors	Pins	Name	Description
	7		Pull-up signal (can be used as GPI input)
	8		Pull-up signal (can be used as GPI input)
J19	1		Pull-down signal (can be used as GPI input)
	2		Pull-down signal (can be used as GPI input)
	3		Pull-down signal (can be used as GPI input)
	4		Pull-down signal (can be used as GPI input)
	5		Pull-down signal (can be used as GPI input)
	6		Pull-down signal (can be used as GPI input)
	7		Pull-down signal (can be used as GPI input)
	8		Pull-down signal (can be used as GPI input)
J20	1		Pull-down signal (can be used as GPI input)
	2		Pull-down signal (can be used as GPI input)
	3		Pull-down signal (can be used as GPI input)
	4		Pull-down signal (can be used as GPI input)
	5		Pull-down signal (can be used as GPI input)
	6		Pull-down signal (can be used as GPI input)
	7		Pull-down signal (can be used as GPI input)
	8		Pull-down signal (can be used as GPI input)
J21	1	VDD	VDD (connect to pin 2 to pullup)
	2		Floating pin connected to PMBUS_ADDR0 through 1-kΩ resistor
	3	GND	GND (connect to pin 2 to pulldown)
J22	1	VDD	VDD (connect to pin 2 to pullup)
	2		Floating pin connected to PMBUS_ADDR1 through 1-kΩ resistor
	3	GND	GND (connect to pin 2 to pulldown)
J23	1	VDD	VDD (connect to pin 2 to pullup)
	2		Floating pin connected to PMBUS_ADDR2 through 1-kΩ resistor
	3	GND	GND (connect to pin 2 to pulldown)
J24	1	+3V3_USB	3.3-V power provided by USB interface adapter EVM
	2	+3V3	3.3-V rail to power VDD. Install a shut jumper to this connector to supply VDD from USB interface adapter.
J25	1	5V	Connected to 5-V V_{IN}
	2		V_{IN} for POL. Connect to pin 1 to supply 5-V V_{IN} to POL.
J26	1	5V_VIN	5-V input power positive terminal
	2	GND	5-V input power negative terminal
J27	1	POL1_EN	Connect this pin to an EN pin to test enable function
	2	POL1_PG	Connect this pin to a DMON pin to test digital monitor function
	3	POL1_VOUT	Connect this pin to an AMON pin to test analog monitor function
	4	POL1_MAR	Connect this pin to a MAR pin to test margining function
J28	1	5V	Connected to 5-V V_{IN}
	2		V_{IN} for POL. Connect to pin 1 to supply 5-V V_{IN} to POL.
J29	1	POL2_EN	Connect this pin to an EN pin to test enable function
	2	POL2_PG	Connect this pin to a DMON pin to test digital monitor function
	3	POL2_VOUT	Connect this pin to an AMON pin to test analog monitor function
	4	POL2_MAR	Connect this pin to a MAR pin to test margining function
J30	1	5V	Connected to 5-V V_{IN}
	2		V_{IN} for POL. Connect to pin 1 to supply 5-V V_{IN} to POL.
J31	1	POL3_EN	Connect this pin to an EN pin to test enable function
	2	POL3_PG	Connect this pin to a DMON pin to test digital monitor function
	3	POL3_VOUT	Connect this pin to an AMON pin to test analog monitor function
	4	POL3_MAR	Connect this pin to a MAR pin to test margining function
J32	1	5V	Connected to 5-V V_{IN}
	2		V_{IN} for POL. Connect to pin 1 to supply 5-V V_{IN} to POL.

Table 2. Connector Definitions (continued)

Connectors	Pins	Name	Description
J33	1	POL4_EN	Connect this pin to an EN pin to test enable function
	2	POL4_PG	Connect this pin to a DMON pin to test digital monitor function
	3	POL4_VOUT	Connect this pin to an AMON pin to test analog monitor function
	4	POL4_MAR	Connect this pin to a MAR pin to test margining function

5.4 List of Test Points

Table 3 lists and describes the test points.

Table 3. Test Points Functions

Test Points	Name	Description
TP1	GND	Ground
TP2	GND	Ground
TP3	GND	Ground
TP4	GND	Ground
TP5	GND	Ground
TP6	GND	Ground
TP8	5V_VIN	5-V input power positive terminal
TP9	GND	Ground
TP10	PMB_SDA	PMBus Data
TP11	PMB_CTRL	PMBus CONTROL line
TP12	PMB_SCL	PMBus Clock
TP13	PMB_ALERT	PMBus ALERT# line
TP14	RESET	UCD90320U reset pin signal

6 Software Setup

Accessing the configuration of the UCD90320UEVM-032, control and monitoring capabilities with the Fusion Digital Power Designer software tool requires a one-time software setup per host system.

6.1 Fusion Digital Power Designer Software (Fusion GUI) Installation

Place the *Fusion Digital Power Designer Software* (Fusion GUI) installer executable file in a known location on the host computer to be used for EVM configuration and test.

Double click the TI-Fusion-Digital-Power-Designer-2.0.xxx.exe file and proceed through the installation by accepting the installer prompts and the license agreement. Use the Fusion GUI installer's suggested default installation locations to complete the install.

When the Fusion GUI installation reaches the finished window, **uncheck** the Launch application check box and close the window.

7 Test Procedure

The UCD90320UEVM-032_Default_Configuration.xml file is found on the TI website and is provided to allow the user to return the EVM to its originally-configured state. Open the Fusion GUI while the powered EVM is connected to the computer with the USB interface adapter. In the Fusion GUI interface, select **File → Import Project** and the *Project Open Wizard* window opens.

7.1 Voltage Monitoring Example

Connect the EVM as shown in Figure 8. Connect 5-V V_{IN} to J26. Open the *Fusion Digital Power Designer GUI* by navigating to the **Start → Texas Instruments Fusion Digital Power Designer → Fusion Digital Power Designer** (not the offline version which would have monitoring disabled).

All AMON and DMON pins are assigned to corresponding rails in the default configuration file. Connect a wire jumper from POL1_VOUT to the AMON1 pin. Connect a wire jumper from POL1_EN to a pull-up pin in J18. The output voltage of POL1 will be displayed as *Vout #1* voltage in the **Fusion GUI → Monitor** page. Note that floating AMON pins give non-zero readings, which is an expected behavior.

7.2 Rail Enable Example

In the default configuration file, all EN pins are assigned to corresponding rails, and all rails are controlled by the CONTROL pin. The pin assignments are shown in the **Fusion GUI → Configure page → Hardware Configuration** tab. The CONTROL pin status can be controlled in the **Fusion GUI → Monitor** page. Turn on the CONTROL Line in the *Monitor* page. Observe that all LEDs attached to EN pins are lit.

7.3 Fault Log Example (Including Blackbox Log)

In the *Status* page, click the **Clear Faults** button, the **Clear Logged Faults** button, and the **Clear Blackbox Log** button to clear all previous faults. In **Configure** page → **Global Configuration** tab → **Set/Sync Device Clock** window, click **Set Device Clock to Local PC Time** button to update device run time clock.

With the CONTROL line being asserted, disconnect the jumper wire from the POL1_EN pin, which disables the POL1 output. Since the CONTROL line is asserted, and Rail #1 is previously in *Power Good* condition, the unexpected POL1 output drop will cause a V_{OUT} UV fault. In the **Status page → Status Registers** tab, observe that the V_{OUT} UV Fault of Rail #1 is raised. In the *Logged Faults* tab, observe that the V_{OUT} UV Fault of Rail #1 is also raised. In the *Blackbox Info* tab, click the **Refresh Blackbox Log** button. Observe that all the fault information and status of all the GPI, GPO, and rails when the fault occurred were recorded in the *Blackbox Log*.

7.4 Command GPO Example

In the default configuration file, the GPIO3-4 pins are configured as command GPO. In the **Configure page → Hardware Configuration** tab, change the *Command GPO* states and then click the **Write to Hardware** button. Observe the LED of the corresponding GPIO pin changes state.

7.5 GPI and Logic GPO Example

In the default configuration file, the GPIO1 pin is configured as GPI pin with GPI fault enabled. Each of the 16 LGPO pins is configured to follow the GPI input with 960-ms time delay. The pin assignments are shown in **Configure page → Hardware Configuration** tab.

Connect a jumper wire from a pull-up pin in J17 or J18 to the GPI pin. Observe that the LEDs of the 16 LGPO pins are lit after 960 ms. Also observe that the corresponding GPI Fault is logged in the *Status* page. Then disconnect the logic input signal from the GPI pin. Observe that the LEDs of the LGPO pins are out after 960 ms.

7.6 Margin Example

In the default configuration file, all 24 analog rails are configured with the margining function. The pin assignments are shown in **Configure page → Hardware Configuration** tab. Connect POL1 output voltage (J27-POL1_VOUT) to AMON1 pin using a jumper wire. Then connect the margin input of POL1 (J27-POL1_MAR) to the MAR1 pin. Also, connect the enable pin of POL1 (J27-POL1_EN) to EN1.

In **Fusion GUI → Monitor page**, turn on the CONTROL line. Observe that the EN1 pin's LED is lit, and the on-board POL is enabled. The POL's output voltage is monitored in the Monitor page, which should be at 1.2 V. In **Fusion GUI → Monitor page**, click to change margin status to Low. Observe that the POL output voltage is regulated at Margin Low level defined in **Configure page → Vout Config** tab. Then click to change margin status to High. Observe that the POL output voltage is regulated at Margin High level.

7.7 Cascading Example

7.7.1 Sync Clock

Sync Clock can synchronize multiple UCD90320U devices such that they respond to the same GPI event synchronously, and the same GPI event has the same time stamp in all synchronized UCD90320U devices. The *Sync Clock I/O* pin is located in J9. Implementing the *Sync Clock* feature requires two or more UCD90320UEVM-032 boards.

In **Fusion GUI → Configure page → Global Configuration tab → Misc Config**, configure one EVM board as *Sync Clock* master, and all other boards as slaves. Connect the multiple EVM boards to the same ground. Connect all *Sync Clock* pins to the same node. Observe that the synchronized UCD90320U devices respond to the same GPI event synchronously.

When the *Sync Clock* pin is not used, configure the UCD90320U device as *Sync Clock* master.

7.7.2 Fault Pin

Multiple UCD90320U devices can be acknowledged of the same rail fault and react accordingly, even if the rail is monitored by only one UCD90320U device. This is achieved with the *Fault Pin* feature.

In each UCD90320U device, up to 4 GPI pins can be configured as *Fault Pins*. Each *Fault Pin* is connected to a *Fault Bus*. Each *Fault Bus* should be pulled up to 3.3 V by a 10-kΩ resistor. When there is no fault on a *Fault Bus*, the *Fault Pins* are GPI pins and listen to the *Fault Bus*. When a rail fault is detected by a UCD90320U device, the corresponding *Fault Pin* is turned into active driven low state, pulling down the *Fault Bus* and informing all other UCD90320U devices of the corresponding fault.

In the default configuration file, the GPIO2 pin is configured as a *Fault Pin*. Continuing the previous example, where CONTROL line is asserted, POL1_EN is connected to EN1, and POL1_VOUT is connected to AMON1. Connect GPIO2 (*Fault Pin*) to a pull-up pin in J17 or J18. Then, disconnect the POL1_VOUT pin from AMON1, observe that the LED of GPIO2 is out due to Rail #1 V_{OUT} UV fault. The *Fault Pin* configuration is in **Fusion GUI → Configure page → Global Configuration tab → Fault Pin Config**. Only the faults on selected rails (pages) will trigger the *Fault Pin* to pulldown.

Reconnect POL1_VOUT to AMON1 so that the *Fault Pin* is no longer held low by the UCD90320U device. Next, disconnect GPIO2 from the pull-up signal. This simulates the condition that the *Fault Bus* is pulled down by another UCD90320U device. Observe that a GPI2 fault is logged in **Fusion GUI → Status page → Logged Faults tab → Logged Faults Detail**. This GPI fault can be configured to trigger rail shut down. The fault response of each rail to GPI faults can be configured in the **Fusion GUI → Configure page → Rail Config tab → GPI Fault Responses** window.

The *Fault Pin* feature and the *Sync Clock* feature can work together to achieve better synchronized fault response performance.

8 EVM Assembly Drawing and PCB Layout

The EVM assembly drawing and PCB layout images are shown in Figure 9 through Figure 22.

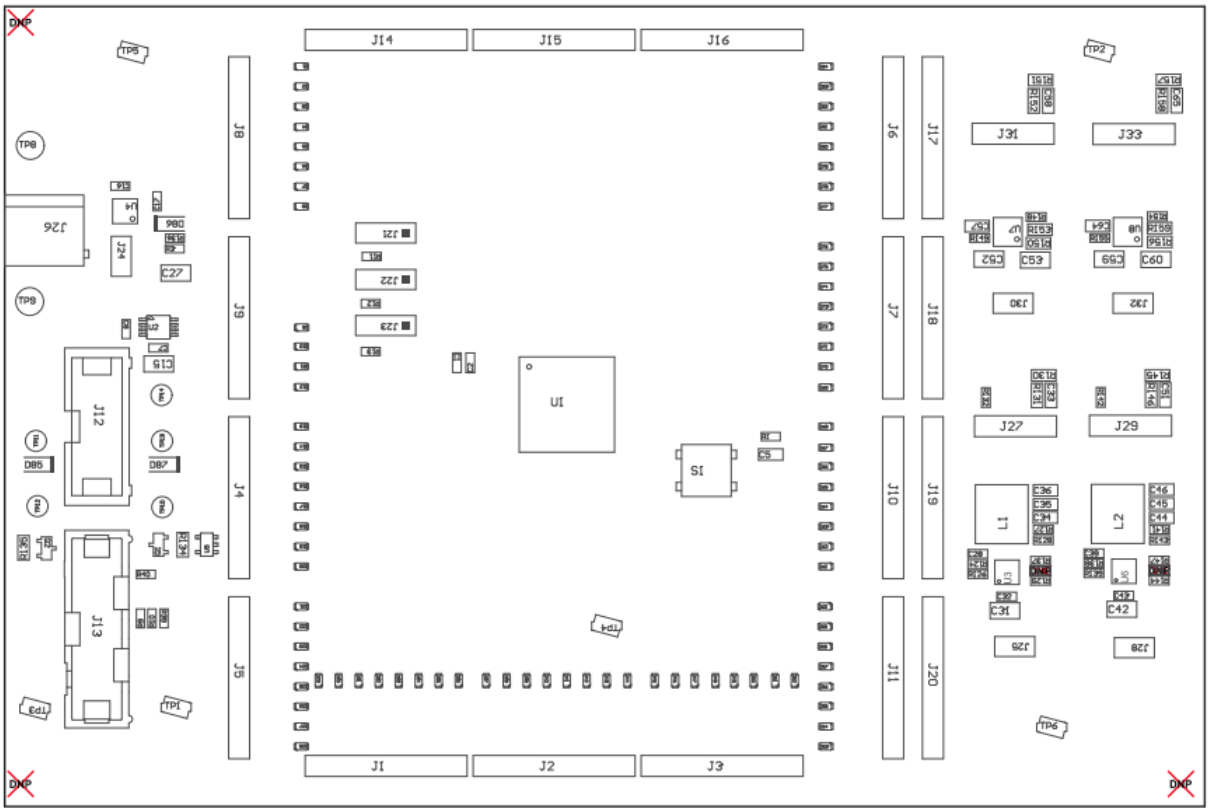


Figure 9. Top Assembly Drawing

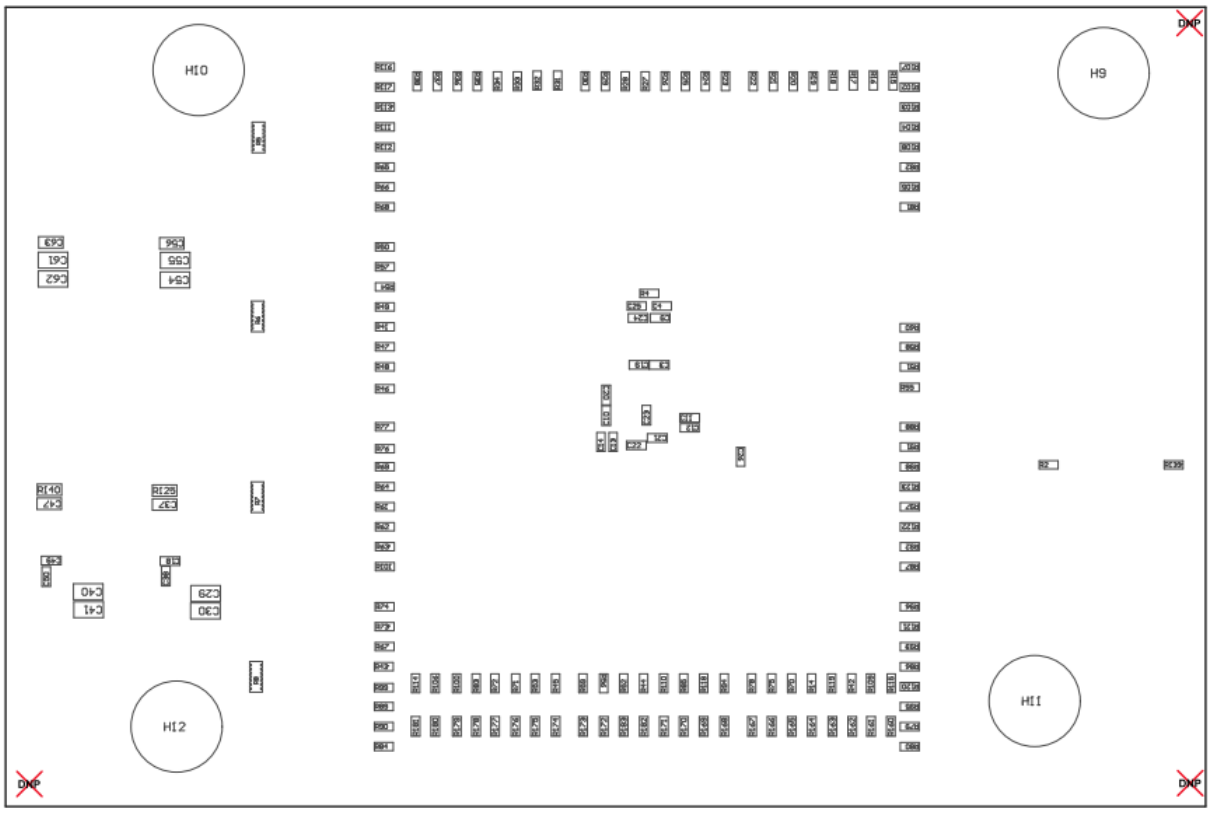


Figure 10. Bottom Assembly Drawing

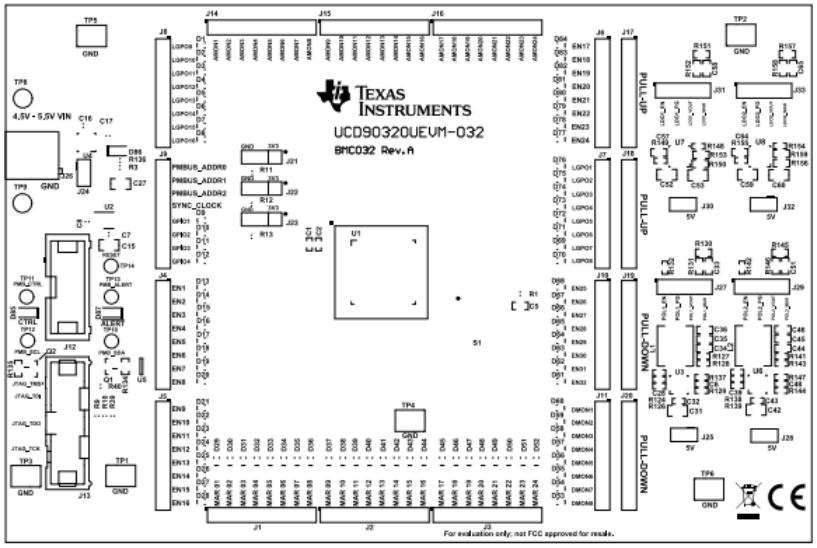


Figure 11. Top Overlay

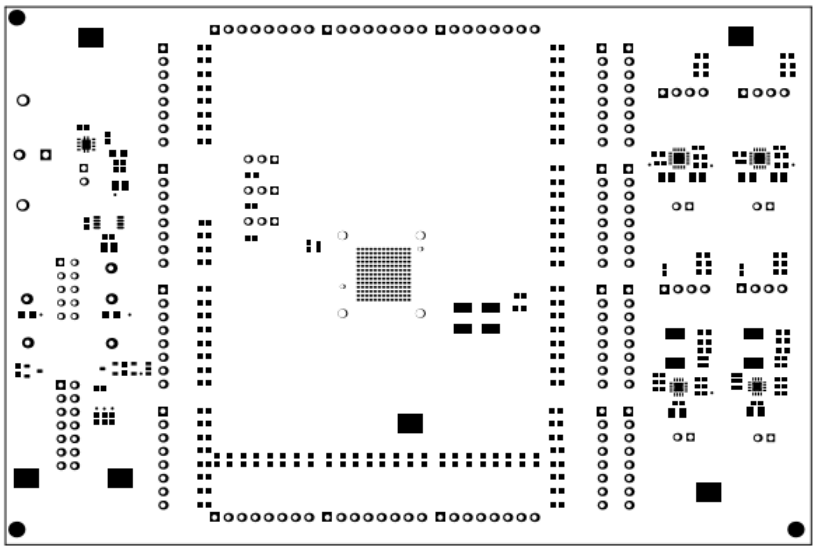


Figure 12. Top Solder Mask

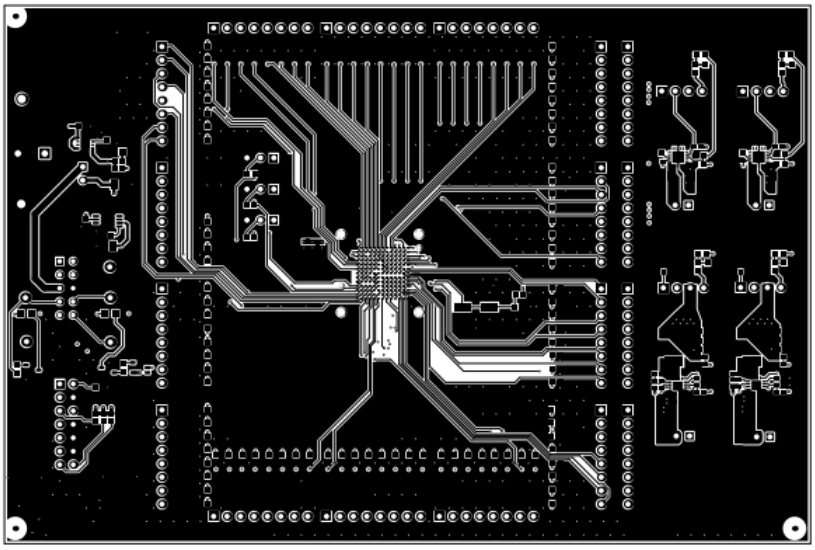


Figure 13. Top Layer

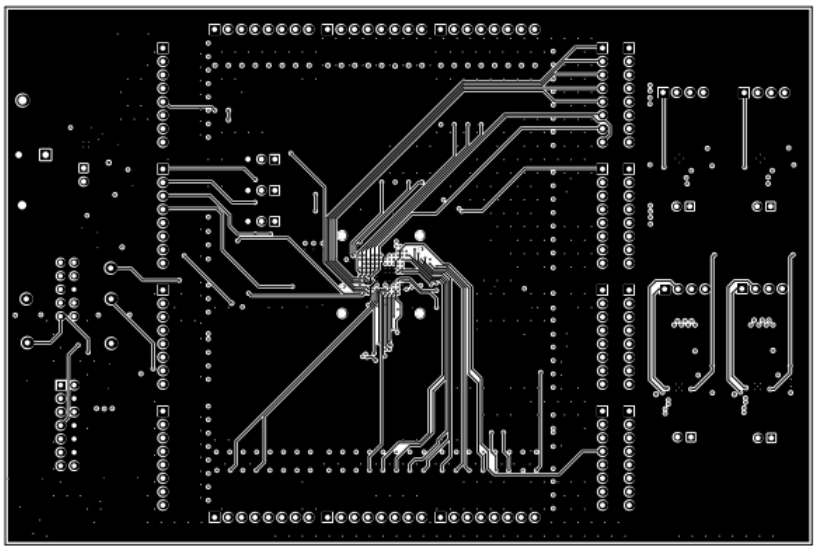


Figure 14. Mid Layer 1

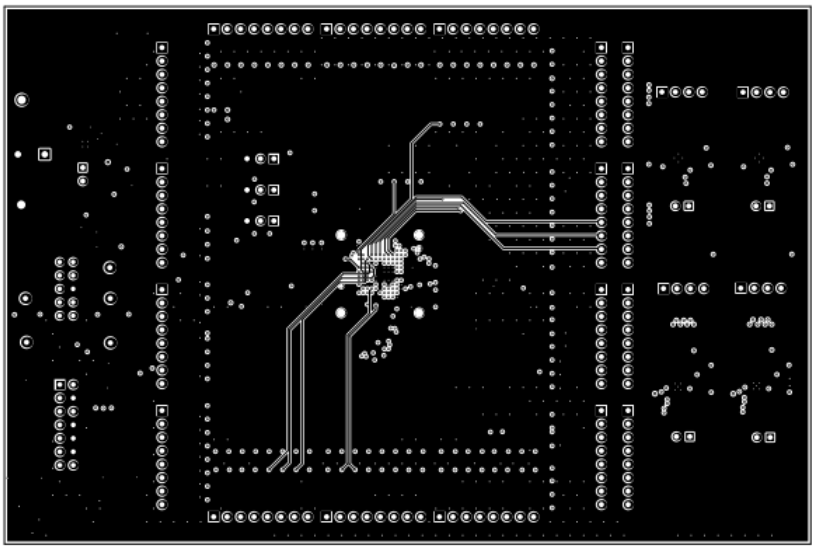


Figure 15. Mid Layer 2

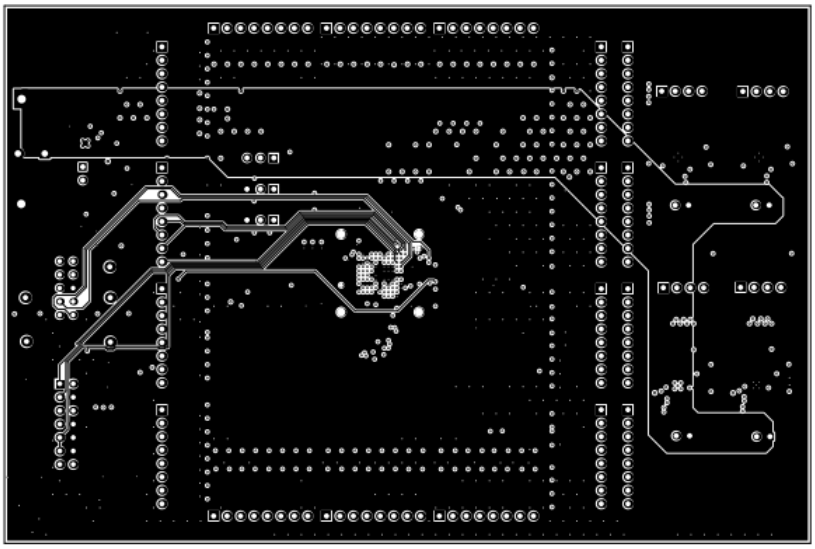


Figure 16. Mid Layer 3

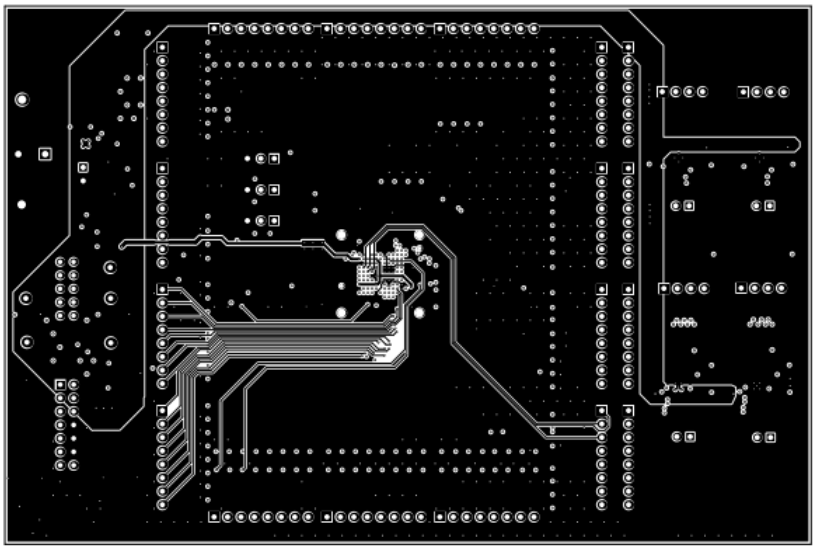


Figure 17. Mid Layer 4

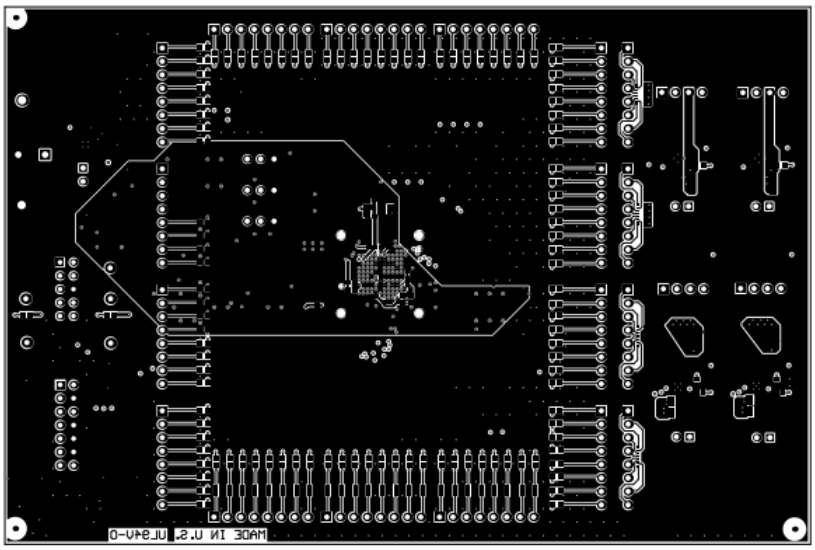


Figure 18. Bottom Layer

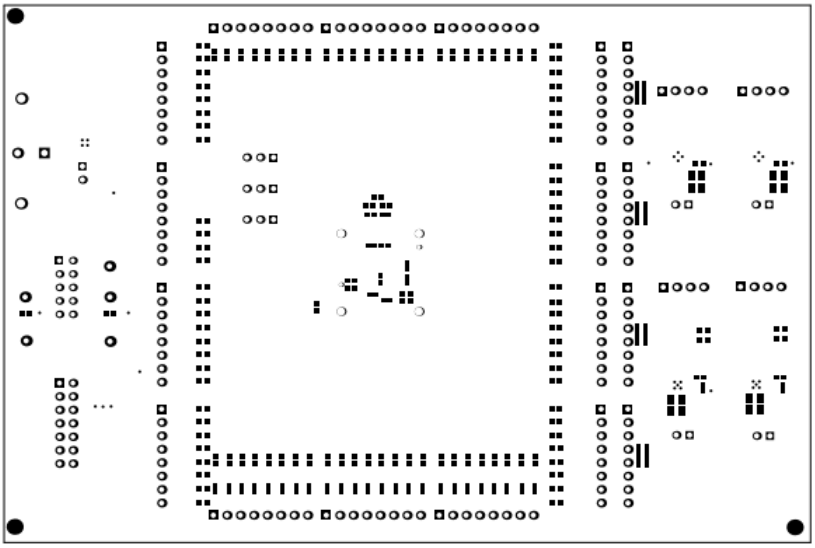


Figure 19. Bottom Solder Mask

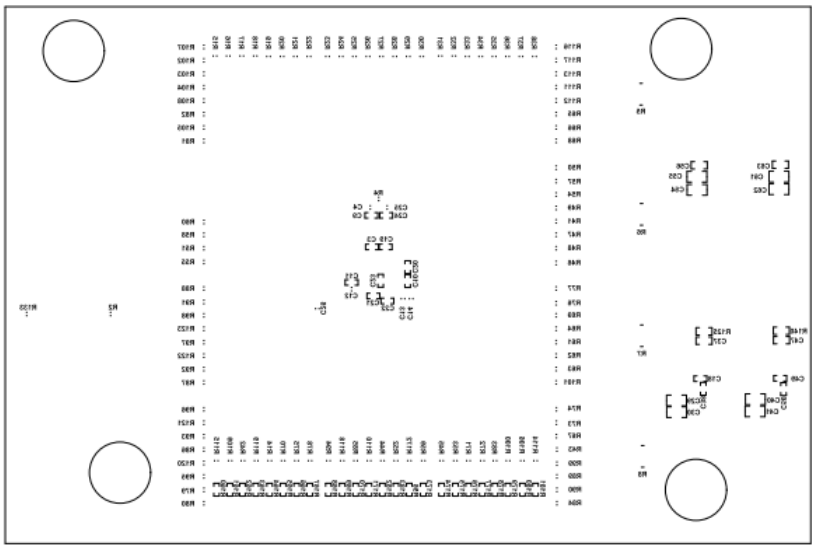
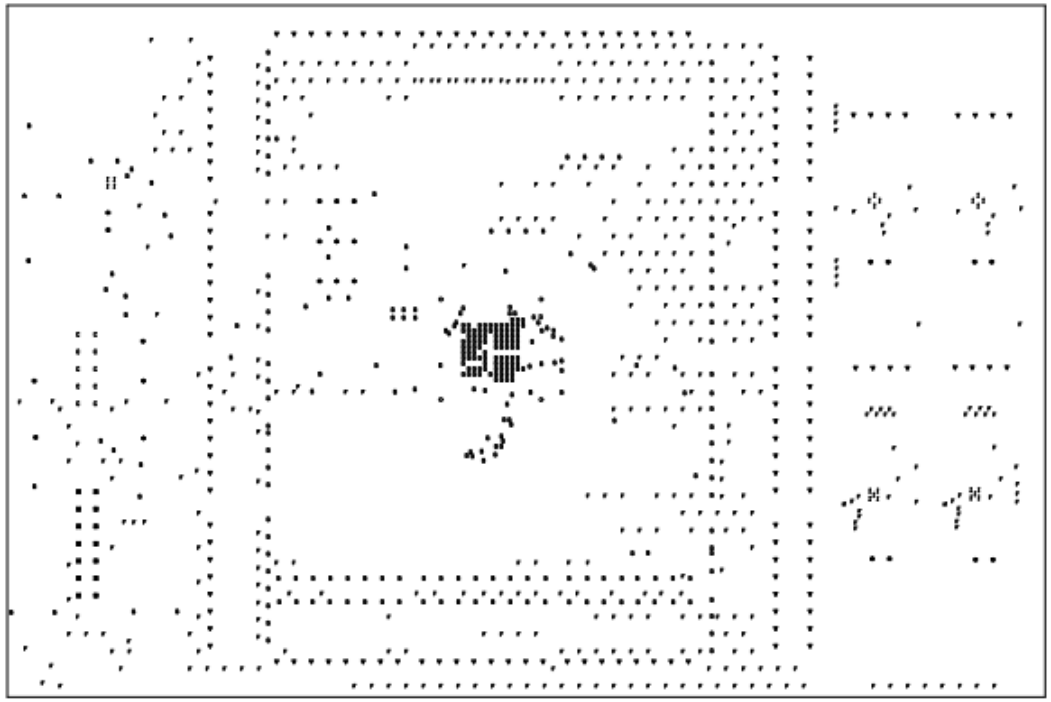


Figure 20. Bottom Overlay



Symbol	Hit Count	Finished Hole Size	Plated	Hole Type
H	2	12.00mil (0.305mm)	PTH	Round
D	2	31.10mil (0.790mm)	NPTH	Round
A	2	49.21mil (1.250mm)	PTH	Round
B	2	63.00mil (1.600mm)	PTH	Round
O	4	62.60mil (1.590mm)	NPTH	Round
C	10	35.43mil (0.900mm)	PTH	Round
⊠	14	37.00mil (0.940mm)	PTH	Round
I	22	7.87mil (0.200mm)	PTH	Round
✡	24	40.00mil (1.016mm)	PTH	Round
▽	160	39.37mil (1.000mm)	PTH	Round
G	307	8.00mil (0.203mm)	PTH	Round
F	480	10.00mil (0.254mm)	PTH	Round
	1029 Total			

Figure 21. Drill Drawing

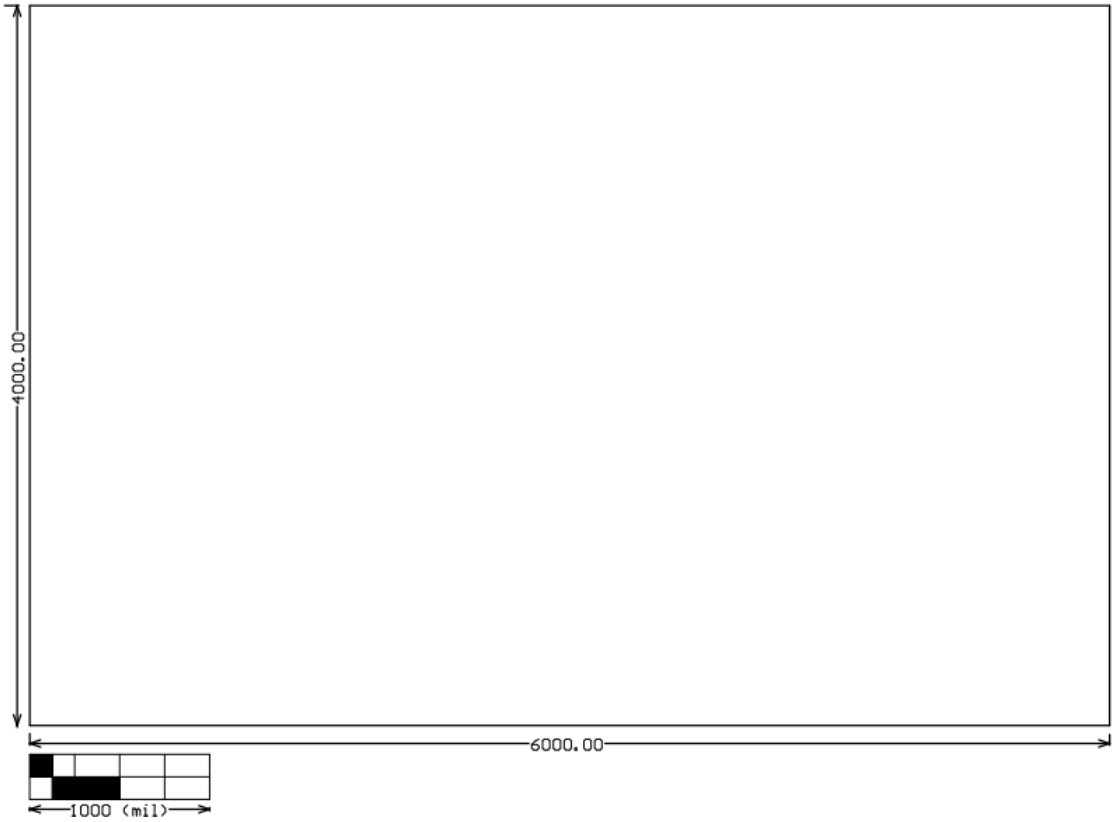


Figure 22. Board Dimensions

9 Bill of Materials

Table 4 lists the EVM bill of materials.

Table 4. UCD90320UEVM-032 BOM

Designator	Qty	Value	Description	Package Reference	Part Number	Man µF acturer	Alternate Part Number	Alternate Man µF acturer
C1, C3, C18, C19, C20, C49	6	0.01 µF	CAP, CERM, 0.01 µF, 16 V, +/- 10%, X7R, 0402	0402	C1005X7R1C103K050BA	TDK		
C2, C9, C10, C11, C21, C22, C23, C24	8	0.1 µF	CAP, CERM, 0.1 µF, 6.3 V, +/- 10%, X5R, 0402	0402	C1005X5R0J104K050BA	TDK		
C4, C7, C8, C12, C13, C14, C16, C25, C26	9	1 µF	CAP, CERM, 1 µF, 25 V, +/- 10%, X5R, 0603	0603	C1608X5R1E105K080AC	TDK		
C5	1	1000pF	CAP, CERM, 1000pF, 50V, +/-5%, X7R, 0603	0603	C0603C102J5RACTU	Kemet	-	-
C15, C27	2	10 µF	CAP, CERM, 10 µF, 6.3 V, +/- 10%, X6S, 0805	0805	GRM219C80J106KE39D	Murata		
C17	1	0.01 µF	CAP, CERM, 0.01 µF, 50 V, +/- 5%, X7R, 0603	0603	C0603C103J5RACTU	Kemet		
C28, C32, C39, C43	4	0.1 µF	CAP, CERM, 0.1 µF, 16 V, +/- 10%, X5R, 0402	0402	GRM155R61C104KA88D	Murata		
C29, C30, C31, C40, C41, C42	6	22 µF	CAP, CERM, 22 µF, 6.3 V, +/- 20%, X5R, 0805	0805	GRM21BR60J226ME39L	Murata		
C33, C51	2	6800 pF	CAP, CERM, 6800 pF, 100 V, +/- 10%, X7R, 0603	0603	06031C682KAT2A	AVX		
C34, C35, C36, C37, C44, C45, C46, C47	8	22 µF	CAP, CERM, 22 µF, 6.3 V, +/- 20%, X5R, 0603	0603	C1608X5R0J226M080AC	TDK		
C38, C50	2	2700pF	CAP, CERM, 2700 pF, 50 V, +/- 10%, X7R, 0402	0402	GRM155R71H272KA01D	Murata		
C52, C53, C59, C60	4	47 µF	CAP, CERM, 47 µF, 4 V, +/- 20%, X5R, 0805	0805	GRM219R60G476ME44D	Murata		
C54, C55, C61, C62	4	10 µF	CAP, CERM, 10 µF, 16 V, +/- 10%, X5R, 0805	0805	GRM21BR61C106KE15L	Murata		
C56, C57, C63, C64	4	0.01 µF	CAP, CERM, 0.01 µF, 50 V, +/- 10%, X7R, 0603	0603	GRM188R71H103KA01D	Murata		
C58, C65	2	0.033 µF	CAP, CERM, 0.033 µF, 50 V, +/- 5%, X7R, 0603	0603	06035C333JAT2A	AVX		
D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15, D16, D17, D18, D19, D20, D21, D22, D23, D24, D25, D26, D27, D28, D29, D30, D31, D32, D33, D34, D35, D36, D37, D38, D39, D40, D41, D42, D43, D44, D45, D46, D47, D48, D49, D50, D51, D52, D53, D54, D55, D56, D57, D58, D59, D60, D61, D62, D63, D64, D65, D66, D67, D68, D69, D70, D71, D72, D73, D74, D75, D76, D77, D78, D79, D80, D81, D82, D83, D84	84	Green	LED, Green, SMD	1.7x0.65x0.8mm	LG L29K-G2J1-24-Z	OSRAM		
D85, D86	2	Green	LED, Green, SMD	LED_0805	LTST-C171GKT	Lite-On		
D87	1	Red	LED, Red, SMD	LED_0805	LTST-C170KRKT	Lite-On		
H9, H10, H11, H12	4		Bumpon, Hemisphere, 0.44 X 0.20, Clear	Transparent Bumpon	SJ-5303 (CLEAR)	3M		
J1, J2, J3, J4, J5, J6, J7, J8, J9, J10, J11, J14, J15, J16, J17, J18, J19, J20	18		Header, 100mil, 8x1, Tin, TH	Header, 8x1, 100mil, TH	PEC08SAAN	Sullins Connector Solutions		
J12	1		Header (shrouded), 100mil, 5x2, Gold, TH	TH, 10-Leads, Body 8.5x20mm, Pitch 2.54mm	XG4C-1031	Omron Electronic Components		
J13	1		Header (shrouded), 100mil, 7x2, Gold, TH	7x2 Header	N2514-6002-RB	3M		

Table 4. UCD90320UEVM-032 BOM (continued)

Designator	Qty	Value	Description	Package Reference	Part Number	Man µF acturer	Alternate Part Number	Alternate Man µF acturer
J21, J22, J23	3		Header, 100mil, 3x1, Tin, TH	Header, 3 PIN, 100mil, Tin	PEC03SAAN	Sullins Connector Solutions		
J24, J25, J28, J30, J32	5		Header, 100mil, 2x1, Tin, TH	Header, 2 PIN, 100mil, Tin	PEC02SAAN	Sullins Connector Solutions		
J26	1		TERMINAL BLOCK 5.08MM VERT 2POS, TH	TERM_BLK, 2pos, 5.08mm	ED120/2DS	On-Shore Technology		
J27, J29, J31, J33	4		Header, 100mil, 4x1, Tin, TH	Header, 4x1, 100mil, TH	PEC04SAAN	Sullins Connector Solutions		
L1, L2	2	1 µH	Inductor, Shielded, Ferrite, 1 µH, 12 A, 0.0072 ohm, SMD	Inductor, 7.2x4x6.5mm	SRP6540-1R0M	Bourns		
Q1, Q2	2	60 V	MOSFET, N-CH, 60 V, 0.17 A, SOT-23	SOT-23	2N7002-7-F	Diodes Inc.		None
R1, R10, R39, R40	4	4.7 kΩ	RES, 4.7 k, 5%, 0.1 W, 0603	0603	CRCW06034K70JNEA	Vishay-Dale		
R2, R133, R136	3	330 Ω	RES, 330, 5%, 0.1 W, 0603	0603	CRCW0603330RJNEA	Vishay-Dale		
R3	1	0.1 Ω	RES, 0.1, 1%, 0.1 W, 0603	0603	ERJ-3RSFR10V	Panasonic		
R4	1	1.0 Ω	RES, 1.0, 5%, 0.1 W, 0603	0603	CRCW06031R00JNEA	Vishay-Dale		
R5, R6, R7, R8	4	680 Ω	RES, 680, 5%, 0.0625 W, Resistor Array - 8x1	Resistor Array - 8x1	EXB-2HV681JV	Panasonic		
R9	1	0	RES, 0, 5%, 0.1 W, 0603	0603	ERJ-3GEY0R00V	Panasonic		
R11, R12, R13	3	1.0 kΩ	RES, 1.0 k, 5%, 0.1 W, 0603	0603	RC0603JR-071KL	Yageo America		
R14, R41, R42, R43, R44, R45, R46, R47, R48, R49, R50, R51, R52, R53, R54, R55, R56, R57, R58, R59, R60, R61, R62, R63, R64, R65, R66, R67, R68, R69, R70, R71, R72, R73, R74, R75, R76, R77, R78, R79, R80, R81, R82, R83, R84, R85, R86, R87, R88, R89, R90, R91, R92, R93, R94, R95, R96, R97, R98, R99, R100, R101, R102, R103, R104, R105, R106, R107, R108, R109, R110, R111, R112, R113, R114, R115, R116, R117, R118, R119, R120, R121, R122, R123	84	1.65 kΩ	RES, 1.65 k, 1%, 0.1 W, 0603	0603	RC0603FR-071K65L	Yageo America		
R15, R16, R17, R18, R19, R20, R21, R22, R23, R24, R25, R26, R27, R28, R29, R30, R31, R32, R33, R34, R35, R36, R37, R38	24	200 Ω	RES, 200, 0.1%, 0.1 W, 0603	0603	RG1608P-201-B-T5	Susumu Co Ltd		
R124, R138	2	0	RES, 0, 5%, 0.063 W, 0402	0402	CRCW04020000Z0ED	Vishay-Dale		
R125, R140	2	40.2 Ω	RES, 40.2, 1%, 0.1 W, 0603	0603	RC0603FR-0740R2L	Yageo America		
R126, R127, R128, R139, R141, R143, R148, R154	8	20.0 kΩ	RES, 20.0 k, 1%, 0.063 W, 0402	0402	CRCW040220K0FKED	Vishay-Dale		
R129, R132, R142, R144, R149, R155	6	10 kΩ	RES, 10 k, 5%, 0.063 W, 0402	0402	CRCW040210K0JNED	Vishay-Dale		
R130, R145	2	196 kΩ	RES, 196 k, 1%, 0.1 W, 0603	0603	CRCW0603196KFKEA	Vishay-Dale		
R131, R146, R152, R158	4	1.00 kΩ	RES, 1.00 k, 1%, 0.1 W, 0603	0603	CRCW06031K00FKEA	Vishay-Dale		
R134, R135	2	30.1 kΩ	RES, 30.1 k, 1%, 0.1 W, 0603	0603	RC0603FR-0730K1L	Yageo America		

Table 4. UCD90320UEVM-032 BOM (continued)

Designator	Qty	Value	Description	Package Reference	Part Number	Man µF acturer	Alternate Part Number	Alternate Man µF acturer
R137, R147	2	82.5 kΩ	RES, 82.5 k, 1%, 0.063 W, 0402	0402	CRCW040282K5FKED	Vishay-Dale		
R150, R156	2	12.1 kΩ	RES, 12.1 k, 1%, 0.1 W, 0603	0603	CRCW060312K1FKEA	Vishay-Dale		
R151, R157	2	120 kΩ	RES, 120 k, 5%, 0.1 W, 0603	0603	CRCW0603120KJNEA	Vishay-Dale		
R153, R159	2	24.3 kΩ	RES, 24.3 k, 1%, 0.1 W, 0603	0603	CRCW060324K3FKEA	Vishay-Dale		
R160, R161, R162, R163, R164, R165, R166, R167, R168, R169, R170, R171, R172, R173, R174, R175, R176, R177, R178, R179, R180, R181, R182, R183	24	30	RES, 30, 5%, 0.063 W, 0402	0402	CRCW040230R0JNED	Vishay-Dale		
S1	1		Switch, Tactile, SPST-NO, 1VA, 32V, SMT	Switch, 6.3x5.36x6.6 mm, SMT	KT11P2JM34LFS	C&K Components		
SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6, SH-J7, SH-J8	8	1x2	Shunt, 100mil, Gold plated, Black	Shunt	969102-0000-DA	3M	SNT-100-BK-G	Samtec
TP1, TP2, TP3, TP4, TP5, TP6	6	SMT	Test Point, Compact, SMT	Testpoint_Keystone_Compact	5016	Keystone		
TP8	1	Red	Test Point, Multipurpose, Red, TH	Red Multipurpose Testpoint	5010	Keystone		
TP9	1	Black	Test Point, Multipurpose, Black, TH	Black Multipurpose Testpoint	5011	Keystone		
TP10, TP11, TP12, TP13, TP14	5	Yellow	Test Point, Miniature, Yellow, TH	Yellow Miniature Testpoint	5004	Keystone		
U1	1		32-Rail PMBus Power Sequencer and System Manager, ZWS0169A	ZWS0169A	UCD90320UZWSR	Texas Instruments	UCD90320UZWST	Texas Instruments
U2	1		Low Noise, Very Low Drift, Precision Voltage Reference, -40 to 125 degC, 8-pin MSOP (DGK), Green (RoHS & no Sb/Br)	DGK0008A	REF5030AIDGKT	Texas Instruments	Equivalent	None
U3, U6	2		2.95 V to 6 V INPUT, 6 A OUTPUT, 2 MHz, SYNCHRONOUS STEP DOWN SWITCHER WITH INTEGRATED FET (SWIFT™), RTE0016F	RTE0016F	TPS54678RTER	Texas Instruments	TPS54678RTET	Texas Instruments
U4	1		Single Output Low Noise LDO, 400 mA, Fixed 3.3 V Output, 1.7 to 5.5 V Input, with Reverse Current Protection, 8-pin SON (DRB), -40 to 85 degC, Green (RoHS & no Sb/Br)	DRB0008A	TPS73633DRBR	Texas Instruments	Equivalent	None
U5	1		Single Inverter Gate, DBV0005A	DBV0005A	SN74LVC1G04DBVR	Texas Instruments	SN74LVC1G04DBVT	Texas Instruments
U7, U8	2		2-A, 6-µVRMS, RF, LDO Voltage Regulator, RGR0020A	RGR0020A	TPS7A8400RGRR	Texas Instruments	TPS7A8400RGRT	Texas Instruments
C6, C48	0	DNP	CAP, CERM, 22 pF, 50 V, +/- 5%, C0G/NP0, 0402	0402	GRM1555C1H220JA01D	Murata		
FID1, FID2, FID3, FID4, FID5, FID6	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A		
Notes:			Unless otherwise noted in the Alternate Part Number and/or Alternate Man µF acturer columns, all parts may be substituted with equivalents.					

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