TPS53681 Technical Reference Manual

Technical Reference Manual

Literature Number: SLUUBO4
May 2017

Contents

List of Figures

List of Tables

Read This First

About This Manual

This Technical Reference Manual (TRM) details the integration, the environment, the functional description, and the programming models for each peripheral and subsystem in the device.

The TRM should not be considered a substitute for the data manual, rather a companion guide that should be used alongside the device-specific data manual to understand the details to program the device. The primary purpose of the TRM is to abstract the programming details of the device from the data manual. This allows the data manual to outline the high-level features of the device without unnecessary information about register descriptions or programming models.

Related Documentation From Texas Instruments

For product information, visit the Texas Instruments website at http://www.ti.com.

Introduction

Topic Page

1.1 Overview

1.2 Environment/External Connections

1.2.1 PMBus Connections

These devices can support either 100-kHz class, 400-kHz class or 1-MHz class operation. Connection for the PMBus interface should follow the DC specifications given in *Section 4.3 of the System Management Bus (SMBus) Specification V3.0* . The complete SMBus specification is available from the SMBus website, smbus.org.

1.2.2 PMBus Address Selection

The PMBus slave address is selected with a resistor divider from VREF to ADDR. The lower resistor, R_{ADDRL}, should be fixed to either 10.0 kΩ or 20.0 kΩ and the PMBus slave address is set by the voltage on the ADDR pin. Refer to Table 1-1. With the desired PMBus address, and R_{ADDRL} selected, R_{ADDRH} may be calculated using Equation 1

.

Note that the PMBus interface uses 7 bit addressing, per the SMBus specification. Users communicating to the device using generic I^2C drivers should be aware that these 7 bits occupy the most significant bits of the first byte in each transaction, with the least significant bit being the data direction bit (0 for write operations, 1 for read operations). That is, for read transactions, the address byte is $A_6A_5A_4A_3A_2A_1A_0$1 and for write operations the address byte is $A_6A_5A_4A_3A_2A_1A_0$0. Refer to the SMBus specification, and Section 2.1.2 for more information.

The general procedure for selecting these resistors is as follows:

1. Determine the desired PMBus slave addresses, per system requirements.
2. Select 10.0 kΩ for the R_{ADDRL} resistor.
3. Using the desired PMBus address, refer to Table 1-1 for the desired ADDR pin voltage.
4. Use Equation 1 to calculate R_{ADDRH}

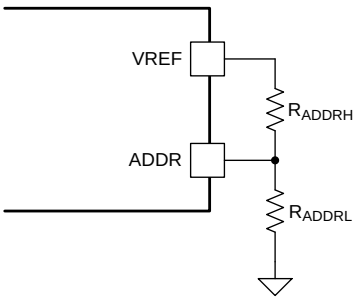

Figure 1-1. PMBus Address Selection

$$R_{ADDRH} = R_{ADDRL}\left(\frac{V_{REF}}{V_{ADDR}} - 1\right) \quad (1)$$

Table 1-1. PMBus Slave Address Selection

V_{ADDR} (V)	PMBus Address (7 bit binary) $A_6A_5A_4A_3A_2A_1A_0$	PMBus Address (7-bit decimal)	I^2C Address Byte (Write Operation)	I^2C Address Byte (Read Operation)
≤ 0.039 V	1011000b	88d	B0h	B1h
0.073 V ± 15 mV	1011001b	89d	B2h	B3h
0.122 V ± 15 mV	1011010b	90d	B4h	B5h

Table 1-1. PMBus Slave Address Selection (continued)

V_{ADDR} (V)	PMBus Address (7 bit binary) $A_6A_5A_4A_3A_2A_1A_0$	PMBus Address (7-bit decimal)	I^2C Address Byte (Write Operation)	I^2C Address Byte (Read Operation)
0.171 V ± 15 mV	1011011b	91d	B6h	B7h
0.219 V ± 15 mV	1011100b	92d	B8h	B9h
0.268 V ± 15 mV	1011101b	93d	BAh	BBh
0.317 V ± 15 mV	1011110b	94d	BCh	BDh
0.366 V ± 15 mV	1011111b	95d	BEh	BFh
0.415 V ± 15 mV	1100000b	96d	C0h	C1h
0.464 V ± 15 mV	1100001b	97d	C2h	C3h
0.513 V ± 15 mV	1100010b	98d	C4h	C5h
0.562 V ± 15 mV	1100011b	99d	C6h	C7h
0.610 V ± 15 mV	1100100b	100d	C8h	C9h
0.660 V ± 15 mV	1100101b	101d	CAh	CBh
0.708 V ± 15 mV	1100110b	102d	CCh	CDh
0.757 V ± 15 mV	1100111b	103d	CEh	CFh
0.806 V ± 15 mV	1101000b	104d	D0h	D1h
0.854 V ± 15 mV	1101001b	105d	D2h	D3h
0.903 V ± 15 mV	1101010b	106d	D4h	D5h
0.952 V ± 15 mV	1101011b	107d	D6h	D7h
1.000 V ± 15 mV	1101100b	108d	D8h	D9h
1.050 V ± 15 mV	1101101b	109d	DAh	DBh
1.098 V ± 15 mV	1101110b	110d	DCh	DDh
1.147 V ± 15 mV	1101111b	111d	DEh	DFh
1.196 V ± 15 mV	1110000b	112d	E0h	E1h
1.245 V ± 15 mV	1110001b	113d	E2h	E3h
1.294 V ± 15 mV	1110010b	114d	E4h	E5h
1.343 V ± 15 mV	1110011b	115d	E6h	E7h
1.392 V ± 15 mV	1110100b	116d	E8h	E9h
1.440 V ± 15 mV	1110101b	117d	EAh	EBh
1.489 V ± 15 mV	1110110b	118d	ECh	EDh
1.540 V ± 15 mV	1110111b	119d	EEh	EFh

PMBus Interface

Topic **Page**

2.1 Overview

2.1.1 Supported PMBus Data Formats

These devices support both linear and VID data formats. The linear data format is used for all telemetry reporting data, and VID formatting for certain other commands. (see for more details on which command supports which data type). Examples of commands that support VID formatting include VOUT_MODE (Read-only Byte) and VOUT_COMMAND (Read/Write Word). An example of each can be seen below in Figure 2-1 and Figure 2-2.

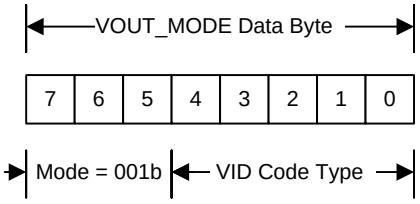

Figure 2-1. VOUT_MODE Data Byte for VID Mode

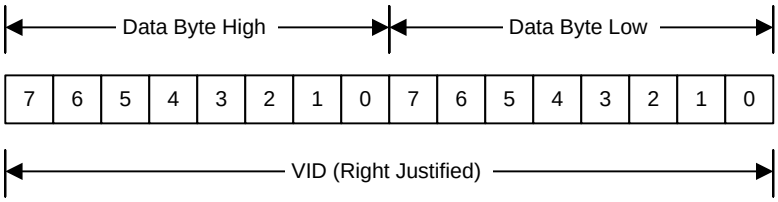

Figure 2-2. VOUT_COMMAND Data Bytes for VID Mode

The Linear Data Format is a two byte value with:

- An 11-bit, two's complement mantissa, and
- A 5-bit, two's complement exponent (scaling factor).

The format of the two bytes is shown in Figure 2-3.

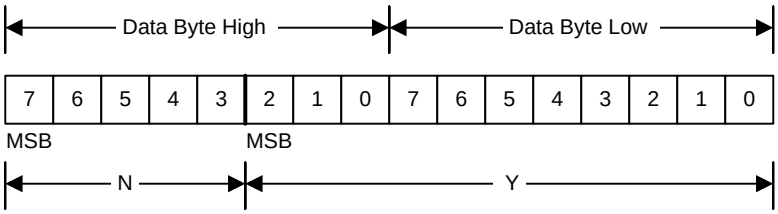

Figure 2-3. Linear Data Format Data Bytes

The relation between Y, N, and the *real world* value is as shown in Equation 2.

$$X = Y \times 2^{N} \quad (2)$$

where

- X is the *real world* value
- Y is an 11-bit, two's complement integer
- N is a 5-bit, two's complement integer

Note that devices that use the Linear format must accept and be able to process any value of N.

2.1.2 PMBus Command Format

These devices are PMBus-compliant. Figure 2-4 through Figure 2-15 show the major communication protocols used. For full details on the PMBus communication protocols, please visit http://pmbus.org.

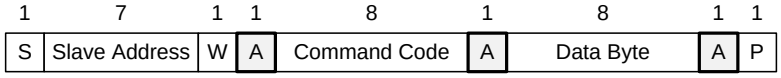

Figure 2-4. Write Byte Protocol

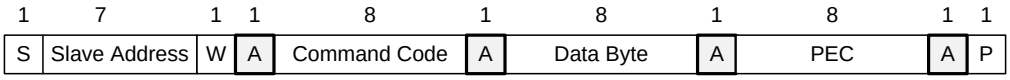

Figure 2-5. Write Byte Protocol with PEC

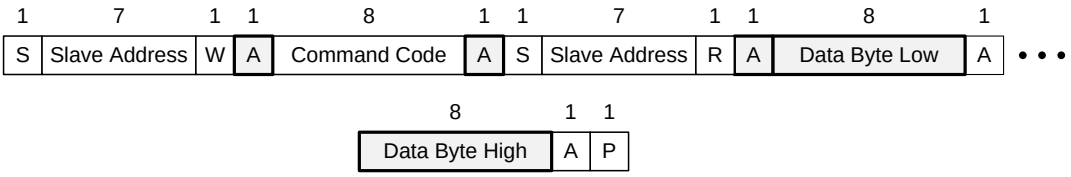

Figure 2-6. Write Word Protocol

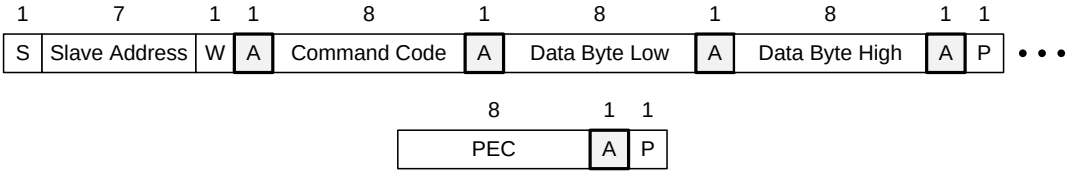

Figure 2-7. Write Word Protocol with PEC

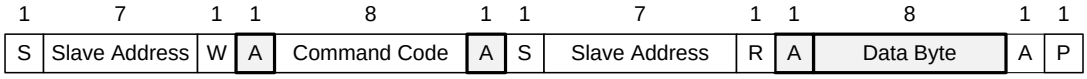

Figure 2-8. Read Byte Protocol

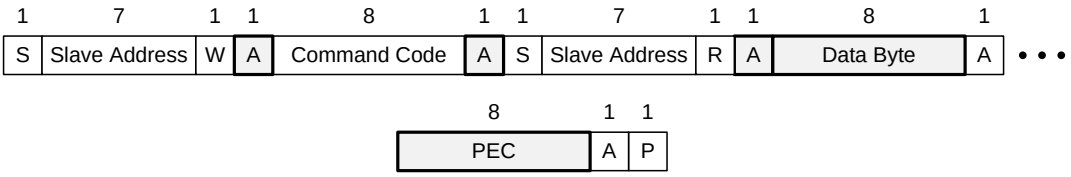

Figure 2-9. Read Byte Protocol with PEC

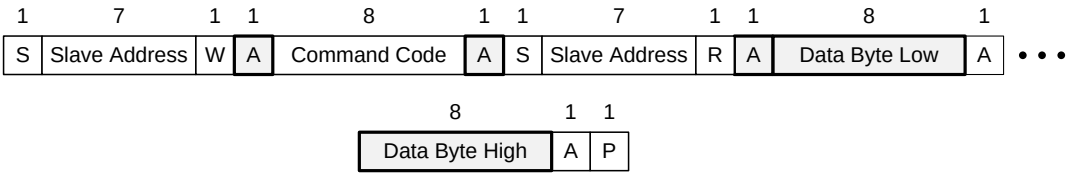

Figure 2-10. Read Word Protocol

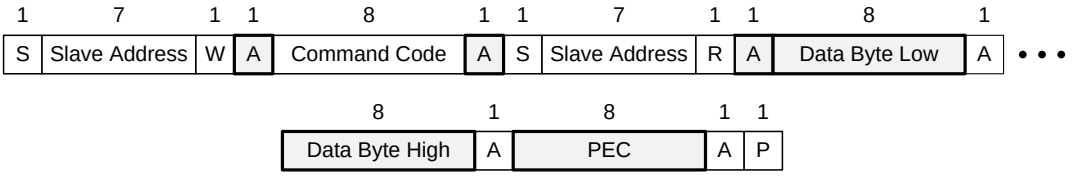

Figure 2-11. Read Word Protocol with PEC

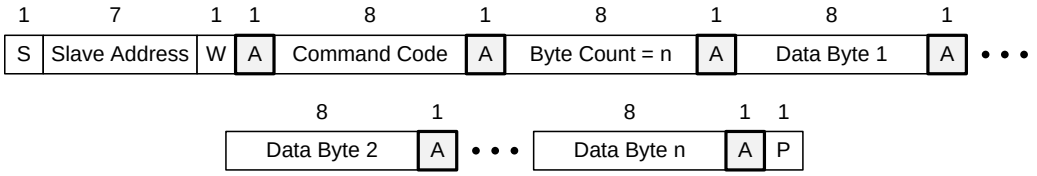

Figure 2-12. Block Write Protocol

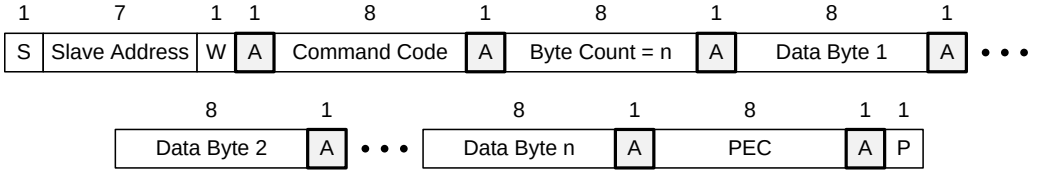

Figure 2-13. Block Write Protocol with PEC

Figure 2-14. Block Read Protocol

Figure 2-15. Block Read Protocol with PEC

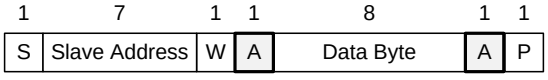

Figure 2-16. Send Byte Protocol

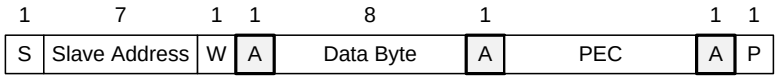

Figure 2-17. Send Byte Protocol with PEC

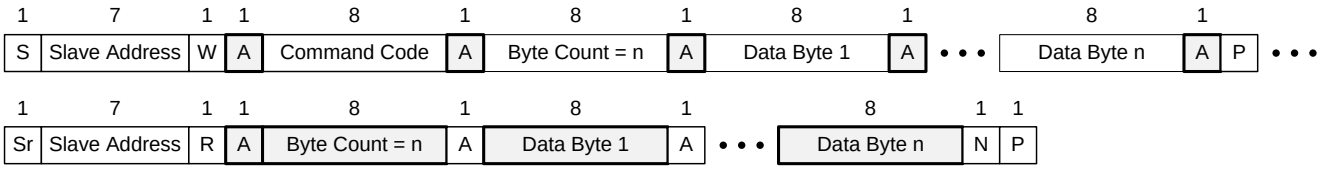

Figure 2-18. Block Write-Block Read Process Call

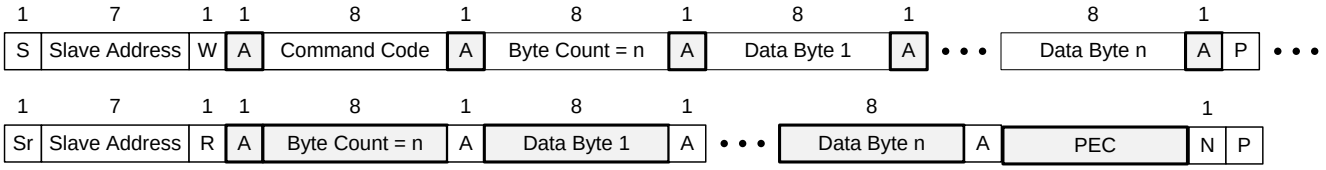

Figure 2-19. Block Write-Block Read Process Call with PEC

2.1.3 Bit Indexes for Block Commands

As specified in Section 2.1.2, individual bytes in block commands are transmitted in ascending order, however, per the SMBus specification, the bits within each byte are in descending order. Therefore, the user must take note of the bit ordering to update block commands successfully.

Example: Reading and Updating USER_DATA commands

For example, if the user reads USER_DATA_00 = 0123456789ABh, the individual byte values and bit indices are shown in Table 2-1:

Table 2-1. Example: USER_DATA_00 = 0123456789ABh bit indexing

Byte Number	USER_DATA_00 Bit Indices	Example Hex Value
0	7:0	01h
1	15:8	23h
2	23:16	45h
3	31:24	67h
4	39:32	89h
5	47:40	ABh

Referring to Table 2-1, for example, to set USER_DATA_00[47:43] to 1111b, the user must issue a block write command, to USER_DATA_00 with the data value of 0123456789FBh.

2.2 VID Table

These devices make extensive use of the VID format. The VR_MODE bits in the MFR_SPECIFIC_13 command select between the 5-mV step, and 10-mV DAC modes. The table below describes the VID table used by these devices.

Table 2-2. VID Table

VID Hex VALUE	DAC STEP (5 mV)	DAC STEP (10 mV)
00	0	0
01	0.25	0.50
02	0.255	0.51
03	0.26	0.52
04	0.265	0.53
05	0.27	0.54
06	0.275	0.55
07	0.28	0.56
08	0.285	0.57
09	0.29	0.58
0A	0.295	0.59
0B	0.30	0.60
0C	0.305	0.61
0D	0.31	0.62
0E	0.315	0.63
0F	0.32	0.64
10	0.325	0.65
11	0.33	0.66
12	0.335	0.67
13	0.34	0.68
14	0.345	0.69
15	0.35	0.70
16	0.355	0.71
17	0.36	0.72
18	0.365	0.73
19	0.37	0.74
1A	0.375	0.75
1B	0.38	0.76
1C	0.385	0.77
1D	0.39	0.78
1E	0.395	0.79
1F	0.40	0.80
20	0.405	0.81
21	0.41	0.82
22	0.415	0.83
23	0.42	0.84
24	0.425	0.85
25	0.43	0.86
26	0.435	0.87
27	0.44	0.88
28	0.445	0.89
29	0.45	0.90
2A	0.455	0.91
2B	0.46	0.92
2C	0.465	0.93
2D	0.47	0.94
2E	0.475	0.95
2F	0.48	0.96
30	0.485	0.97
31	0.49	0.98
32	0.495	0.99
33	0.50	1.00
34	0.505	1.01
35	0.51	1.02
36	0.515	1.03
37	0.52	1.04
38	0.525	1.05
39	0.53	1.06
3A	0.535	1.07
3B	0.54	1.08
3C	0.545	1.09
3D	0.55	1.10
3E	0.555	1.11
3F	0.56	1.12
40	0.565	1.13
41	0.57	1.14
42	0.575	1.15
43	0.58	1.16
44	0.585	1.17
45	0.59	1.18
46	0.595	1.19
47	0.60	1.20
48	0.605	1.21
49	0.61	1.22
4A	0.615	1.23
4B	0.62	1.24
4C	0.625	1.25
4D	0.63	1.26
4E	0.635	1.27
4F	0.64	1.28
50	0.645	1.29
51	0.65	1.30
52	0.655	1.31
53	0.66	1.32
54	0.665	1.33
55	0.67	1.34
56	0.675	1.35

Table 2-2. VID Table (continued)

VID Hex VALUE	DAC STEP (5 mV)	DAC STEP (10 mV)
57	0.68	1.36
58	0.685	1.37
59	0.69	1.38
5A	0.695	1.39
5B	0.70	1.40
5C	0.705	1.41
5D	0.71	1.42
5E	0.715	1.43
5F	0.72	1.44
60	0.725	1.45
61	0.73	1.46
62	0.735	1.47
63	0.74	1.48
64	0.745	1.49
65	0.75	1.50
66	0.755	1.51
67	0.76	1.52
68	0.765	1.53
69	0.77	1.54
6A	0.775	1.55
6B	0.78	1.56
6C	0.785	1.57
6D	0.79	1.58
6E	0.795	1.59
6F	0.80	1.60
70	0.805	1.61
71	0.81	1.62
72	0.815	1.63
73	0.82	1.64
74	0.825	1.65
75	0.83	1.66
76	0.835	1.67
77	0.84	1.68
78	0.845	1.69
79	0.85	1.70
7A	0.855	1.71
7B	0.86	1.72
7C	0.865	1.73
7D	0.87	1.74
7E	0.875	1.75
7F	0.88	1.76
80	0.885	1.77
81	0.89	1.78
82	0.895	1.79
83	0.90	1.80
84	0.905	1.81
85	0.91	1.82
86	0.915	1.83
87	0.92	1.84
88	0.925	1.85
89	0.93	1.86
8A	0.935	1.87
8B	0.94	1.88
8C	0.945	1.89
8D	0.95	1.90
8E	0.955	1.91
8F	0.96	1.92
90	0.965	1.93
91	0.97	1.94
92	0.975	1.95
93	0.98	1.96
94	0.985	1.97
95	0.99	1.98
96	0.995	1.99
97	1.00	2.00
98	1.005	2.01
99	1.01	2.02
9A	1.015	2.03
9B	1.02	2.04
9C	1.025	2.05
9D	1.03	2.06
9E	1.035	2.07
9F	1.04	2.08
A0	1.045	2.09
A1	1.05	2.10
A2	1.055	2.11
A3	1.06	2.12
A4	1.065	2.13
A5	1.07	2.14
A6	1.075	2.15
A7	1.08	2.16
A8	1.085	2.17
A9	1.09	2.18
AA	1.095	2.19
AB	1.10	2.20
AC	1.105	2.21
AD	1.11	2.22
AE	1.115	2.23
AF	1.12	2.24
B0	1.125	2.25
B1	1.13	2.26
B2	1.135	2.27
B3	1.14	2.28
B4	1.145	2.29
B5	1.15	2.30

Table 2-2. VID Table (continued)

VID Hex VALUE	DAC STEP (5 mV)	DAC STEP (10 mV)
B6	1.155	2.31
B7	1.16	2.32
B8	1.165	2.33
B9	1.17	2.34
BA	1.175	2.35
BB	1.18	2.36
BC	1.185	2.37
BD	1.19	2.38
BE	1.195	2.39
BF	1.20	2.40
C0	1.205	2.41
C1	1.21	2.42
C2	1.215	2.43
C3	1.22	2.44
C4	1.225	2.45
C5	1.23	2.46
C6	1.235	2.47
C7	1.24	2.48
C8	1.245	2.49
C9	1.25	2.50
CA	1.255	n/a
CB	1.26	n/a
CC	1.265	n/a
CD	1.27	n/a
CE	1.275	n/a
CF	1.28	n/a
D0	1.285	n/a
D1	1.29	n/a
D2	1.295	n/a
D3	1.30	n/a
D4	1.305	n/a
D5	1.31	n/a
D6	1.315	n/a
D7	1.32	n/a
D8	1.325	n/a
D9	1.33	n/a
DA	1.335	n/a
DB	1.34	n/a
DC	1.345	n/a
DD	1.35	n/a
DE	1.355	n/a
DF	1.36	n/a
E0	1.365	n/a
E1	1.37	n/a
E2	1.375	n/a
E3	1.38	n/a
E4	1.385	n/a
E5	1.39	n/a
E6	1.395	n/a
E7	1.40	n/a
E8	1.405	n/a
E9	1.41	n/a
EA	1.415	n/a
EB	1.42	n/a
EC	1.425	n/a
ED	1.43	n/a
EE	1.435	n/a
EF	1.44	n/a
F0	1.445	n/a
F1	1.45	n/a
F2	1.455	n/a
F3	1.46	n/a
F4	1.465	n/a
F5	1.47	n/a
F6	1.475	n/a
F7	1.48	n/a
F8	1.485	n/a
F9	1.49	n/a
FA	1.495	n/a
FB	1.50	n/a
FC	1.505	n/a
FD	1.51	n/a
FE	1.515	n/a
FF	1.52	n/a

2.3 PMBus Command Summary

CMD	Command Name	Description
00h	PAGE	Selects which channel subsequent PMBus commands address
01h	OPERATION	Enable or disable each channel, enter or exit margin
02h	ON_OFF_CONFIG	Configure the combination of OPERATION, and enable pin required to enable power conversion for each channel.
03h	CLEAR_FAULT	Clears all fault status registers to 00h and releases PMB_ALERT
04h	PHASE	Selects which phase of the active channel subsequent PMBus commands address
10h	WRITE_PROTECT	Used to control writing to the volatile operating memory (PMBus and restore from NVM).
11h	STORE_DEFAULT_ALL	Stores all current storable register settings into NVM as new defaults.
12h	RESTORE_DEFAULT_ALL	Restores all storable register settings from NVM.
19h	CAPABILITY	Provides a way for a host system to determine key PMBus capabilities of the device.
1Bh	SMBALERT_MASK	Selects which fault sources are allowed to assert PMB_ALERT
20h	VOUT_MODE	Read-only output mode indicator
21h	VOUT_COMMAND	Output voltage target.
24h	VOUT_MAX	Sets the maximum output voltage
25h	VOUT_MARGIN_HIGH	Load the unit with the voltage to which the output is to be changed when OPERATION command is set to “Margin High”.
26h	VOUT_MARGIN_LOW	Load the unit with the voltage to which the output is to be changed when OPERATION command is set to “Margin Low”.
27h	VOUT_TRANSITION_RATE	Used to set slew rate settings for output voltage updates
28h	VOUT_DROOP	The VOUT_DROOP sets the rate, in mV/A (mΩ) at which the output voltage decreases (or increases) with increasing (or decreasing) output current for use with Adaptive Voltage Positioning
29h	VOUT_SCALE_LOOP	Used for scaling the VID code
2Ah	VOUT_SCALE_MONITOR	Used for scaling output voltage telemetry
2Bh	VOUT_MIN	Sets the minimum output voltage
33h	FREQUENCY_SWITCH	Sets the switching frequency
35h	VIN_ON	Sets value of input voltage at which the device should start power conversion.
38h	IOUT_CAL_GAIN	Sets the ratio of voltage at the current sense pins to the sensed current.
39h	IOUT_CAL_OFFSET	Used to null offsets in the output current sensing circuit
40h	VOUT_OV_FAULT_LIMIT	Sets the value of the sensed output voltage which triggers an output overvoltage fault
41h	VOUT_OV_FAULT_RESPONSE	Sets the converter response to an output overvoltage event
44h	VOUT_UV_FAULT_LIMIT	Sets the value of the sensed output voltage which triggers an output undervoltage fault
45h	VOUT_UV_FAULT_RESPONSE	Sets the converter response to an output undervoltage event
46h	IOUT_OC_FAULT_LIMIT	Sets the output Over Current fault limit
47h	IOUT_OC_FAULT_RESPONSE	Define the over-current fault response.
4Ah	IOUT_OC_WARN_LIMIT	Sets the value of the output current that causes the over current detector to indicate an over current warning.
4Fh	OT_FAULT_LIMIT	Sets the temperature, in degrees Celsius, of the unit at which it should indicate an Over temperature Fault.
50h	OT_FAULT_RESPONSE	Sets the converter response to an over temperature fault.
51h	OT_WARN_LIMIT	Sets the temperature, in degrees Celsius, of the unit at which it should indicate an Over temperature warning.

CMD	Command Name	Description
55h	VIN_OV_FAULT_LIMIT	Set the voltage, in volts, of the unit at which it should indicate a Vin Over-voltage Fault.
56h	VIN_OV_FAULT_RESPONSE	VIN_OV_FAULT_RESPONSE command instructs the device on what action to take in response to an input overvoltage fault.
59h	VIN_UV_FAULT_LIMIT	VIN_UV_FAULT_LIMIT command sets the value of the input voltage that causes an Input Under voltage Fault
5Ah	VIN_UV_FAULT_RESPONSE	Sets the converter response to an input undervoltage event
5Bh	IIN_OC_FAULT_LIMIT	Sets the value in amperes that causes the over current fault condition of the input current
5Ch	IIN_OC_FAULT_RESPONSE	Sets the converter response to input overcurrent events
5Dh	IIN_OC_WARN_LIMIT	Sets the value in amperes that causes the over current warning condition of the input current
60h	TON_DELAY	Sets the time, in milliseconds, from when a start condition is received (as programmed by the ON_OFF_CONFIG command) until the output voltage starts to rise.
6Bh	PIN_OP_WARN_LIMIT	The PIN_OP_WARN_LIMIT command sets the value of the input power, in watts, that causes a warning that the input power is high
78h	STATUS_BYTE	PMBus read-only status and flag bits.
79h	STATUS_WORD	PMBus read-only status and flag bits.
7Ah	STATUS_VOUT	PMBus read-only status and flag bits.
7Bh	STATUS_IOUT	PMBus read-only status and flag bits.
7Ch	STATUS_INPUT	PMBus read-only status and flag bits.
7Dh	STATUS_TEMPERATURE	PMBus read-only status and flag bits.
7Eh	STATUS_CML	PMBus read-only status and flag bits.
80h	STATUS_MFR_SPECIFIC	PMBus read-only status and flag bits.
88h	READ_VIN	Returns the input voltage in volts
89h	READ_IIN	Returns the input current in amperes
8Bh	READ_VOUT	Returns the output voltage in VID format
8Ch	READ_IOUT	Returns the output current in amperes
8Dh	READ_TEMPERATURE_1	Returns the highest power stage temperature in °C
96h	READ_POUT	Returns the output power in Watts
97h	READ_PIN	Returns the input power in Watts
98h	PMBUS_REVISION	Returns the version of the PMBus specification to which this device complies
99h	MFR_ID	Loads the unit with bits that contain the manufacturer's ID
9Ah	MFR_MODEL	Loads the unit with bits that contain the manufacturer's model number
9Bh	MFR_REVISION	Loads the unit with bits that contain the manufacturer's model revision
9Dh	MFR_DATE	Loads the unit with bits that contain the manufacture date
9Eh	MFR_SERIAL	NVM Checksum
ADh	IC_DEVICE_ID	Returns a number indicating the part number of the device
AEh	IC_DEVICE_REV	Returns a number indicating the device revision
B0h	USER_DATA_00	Used for batch NVM programming.
B1h	USER_DATA_01	Used for batch NVM programming.
B2h	USER_DATA_02	Used for batch NVM programming.
B3h	USER_DATA_03	Used for batch NVM programming.
B4h	USER_DATA_04	Used for batch NVM programming.
B5h	USER_DATA_05	Used for batch NVM programming.
B6h	USER_DATA_06	Used for batch NVM programming.
B7h	USER_DATA_07	Used for batch NVM programming.
B8h	USER_DATA_08	Used for batch NVM programming.

CMD	Command Name	Description
B9h	USER_DATA_09	Used for batch NVM programming.
BAh	USER_DATA_10	Used for batch NVM programming.
BBh	USER_DATA_11	Used for batch NVM programming.
BCh	USER_DATA_12	Used for batch NVM programming.
D0h	MFR_SPECIFIC_00	Configures per-phase overcurrent levels, current share thresholds, and other miscellaneous settings.
D3h	MFR_SPECIFIC_03	Returns information regarding current imbalance warnings for each phase
D4h	MFR_SPECIFIC_04	Returns the output voltage for the active channel, in linear format
D5h	MFR_SPECIFIC_05	Used to trim the output voltage of the active channel, by applying an offset to the currently selected VID code.
D6h	MFR_SPECIFIC_06	Configures dynamic load line options for both channels, and selects Auto-DCM operation.
D7h	MFR_SPECIFIC_07	Configures the internal loop compensation for both channels.
D8h	MFR_SPECIFIC_08	Used to identify catastrophic faults which occur first, and store this information to NVM
D9h	MFR_SPECIFIC_09	Used to configure non-linear transient performance enhancements such as undershoot reduction (USR) and overshoot reduction (OSR)
DAh	MFR_SPECIFIC_10	Used to configure input current sensing, and set the maximum output current
DBh	MFR_SPECIFIC_11	Used to configure the boot-up voltage for each channel
DCh	MFR_SPECIFIC_12	Used to configure input current sensing, OSR, and other miscellaneous settings
DDh	MFR_SPECIFIC_13	Used to configure output voltage slew rates, VR Mode, and other miscellaneous settings.
DEh	MFR_SPECIFIC_14	Used to configure dynamic phase shedding, and compensation ramp amplitude, and dynamic ramp amplitude during USR, and different power states
DFh	MFR_SPECIFIC_15	Used to configure dynamic phase shedding.
E4h	MFR_SPECIFIC_20	Used to set the maximum operational phase number, on-the-fly.
F0h	MFR_SPECIFIC_32	Used to set the input over-power warning
FAh	MFR_SPECIFIC_42	NVM Security

2.4 PMBus Register Maps

2.4.1 (00h) PAGE

The PAGE command provides the ability to configure, control, and monitor through only one physical address both channels (outputs).

The PAGE command must be accessed through Read Byte/Write Byte transactions as shown in Section 2.1.2

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
PAGE							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

PAGE

Table 2-3. PAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PAGE	RW	00h	00h: All commands address PAGE 0 (channel A) 01h: All commands address PAGE 1 (Channel B) FFh: All write transactions address PAGE 0 and PAGE 1. All read transactions will address PAGE 0.

Attempts to write any value other than those specified above will be treated as invalid data - invalid data will be ignored, the appropriate flags in STATUS_CML and STATUS_WORD will be set, and the PMB_ALERT will be asserted to notify the system host of an invalid transaction.

2.4.2 (01h) OPERATION

The OPERATION command is used to enable or disable power conversion, in conjunction with the input from the AVR_EN pin for channel A, and BEN pin for channel B, according to the configuration of the ON_OFF_CONFIG command. It is also used to set the output voltage to the upper or lower MARGIN levels.

OPERATION is a paged register. In order to access OPERATION command for channel A, PAGE must be set to 00h. In order to access OPERATION register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh.

The OPERATION command must be accessed through Read Byte/Write Byte transactions as shown in Section 2.1.2

7	6	5	4	3	2	1	0
RW	R	RW	RW	RW	RW	R	R
ON	0	MARGIN				0	0

LEGEND: R/W = Read/Write; R = Read only

OPERATION

Table 2-4. OPERATION Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ON	RW	0b	Enable/disable power conversion for the currently selected channel, when the ON_OFF_CONFIG command is configured to require input from the ON bit for output control. Note that there may be several other requirements that must be satisfied before the power conversion can begin (e.g. input voltages above UVLO thresholds, AVR_EN/BEN pins high if required by ON_OFF_CONFIG, etc...) 0b: Disable power conversion 1b: Enable power conversion
5:2	MARGIN	RW	0000b	Set the output voltage to either the value selected by the VOUT_MARGIN_HIGH or VOUT_MARGIN_LOW commands, for the currently selected PAGE. 0000b: Margin Off. Output voltage is set to the value of VOUT_COMMAND 0101b: Margin Low (Ignore Fault). Output voltage is set to the value of VOUT_MARGIN_LOW. 0110b: Margin Low (Act on Fault). Output voltage is set to the value of VOUT_MARGIN_LOW. 1001b: Margin High (Ignore Fault). Output voltage is set to the value of VOUT_MARGIN_HIGH 1010b: Margin High (Act on Fault). Output voltage is set to the value of VOUT_MARGIN_HIGH.

Note that the VOUT_MAX_WARN bit in STATUS_VOUT can be caused by a margin operation, if "Act on Fault" is selected, and the VOUT_MARGIN_HIGH/VOUT_MARGIN_LOW value loaded by the margin operation exceeds the value of VOUT_MAX.

2.4.3 (02h) ON_OFF_CONFIG

The ON_OFF_CONFIG command configures the combination of enable pin input and serial bus commands needed to enable/disable power conversion. This includes how the unit responds when power is applied.

ON_OFF_CONFIG is a paged register. In order to access ON_OFF_CONFIG command for channel A, PAGE must be set to 00h. In order to access the ON_OFF_CONFIG register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh.

The ON_OFF_CONFIG command must be accessed through Read Byte/Write Byte transactions as shown in Section 2.1.2

7	6	5	4	3	2	1	0
R	R	R	R	RW	RW	R	R
0	0	0	PU	CMD	CP	PL	SP

LEGEND: R/W = Read/Write; R = Read only

ON_OFF_CONFIG

Table 2-5. ON_OFF_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
4	PU	R	1b	Unsupported and always set to 1. Per the PMBus specification, this bit indicates that the active channel will always require OPERATION and/or the AVR_EN/BEN pin, according to the settings of CMD and CP, in order to begin power conversion.
3	CMD	RW	NVM	The CMD bit controls how the device responds to the ON bit in OPERATION. 0b: Device ignores the ON bit. Power conversion is controlled only by the AVR_EN/BEN pins. 1b: (Default) Device responds to the ON bit.
2	CP	RW	NVM	The CP bit controls how the device responds to the AVR_EN/BEN pins 0b: Device ignores the AVR_EN/BEN pins, and ON/OFF is controlled only by the OPERATION command 1b: Device responds to the AVR_EN/BEN pins.
1	PL	R	1b	Unsupported and always set to 1. Per the PMBus specification, this bit indicates that the AVR_EN and BEN pins operate with active high (high = on) logic.
0	SP	R	1b	Unsupported and always set to 1. Per the PMBus specification, this bit indicates that power conversion will shutdown immediately when commanded to do so, without first waiting for a turn-off delay, or actively ramping down the output voltage.

2.4.4 (03h) CLEAR_FAULT

The CLEAR_FAULTS command is used to clear any fault bits that have been set. This command simultaneously clears all bits in all status registers in the selected PAGE. The faults which are common for both Channel A and Channel B will be cleared together irrespective of PAGE register setting. At the same time, the device negates (clears, releases) its PMB_ALERT signal output if the device is asserting the PMB_ALERT signal.

CLEAR_FAULT is a paged register. In order to access the CLEAR_FAULT command for channel A, PAGE must be set to 00h. In order to access the CLEAR_FAULT command for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh.

The CLEAR_FAULT command must be accessed through the Send Byte transaction as shown in Section 2.1.2. CLEAR_FAULT is a dataless, write-only command and cannot be read.

The CLEAR_FAULTS command does not cause a unit that has latched off for a fault condition to restart. If the fault is still present when the bit is cleared, the fault bit shall immediately be set again and the host notified by the re-assertion of the PMB_ALERT signal. If the device responds to an Alert Response Address (ARA) from the host, it will clear PMB_ALERT; but, not clear the offending status bit(s) (as it has successfully notified the host and then expects the host to handle the interrupt, appropriately). The original fault – as well as any, due to other sources, that occur between the initial assertion of PMB_ALERT and the device's successful response to the ARA - must be cleared (via CLEAR_FAULTS, OFF-ON toggle, or power reset) before any of these sources will be allowed to re-trigger PMB_ALERT. However, fault sources which only become active post-ARA can/will trigger PMB_ALERT.

2.4.5 (04h) PHASE

The PHASE command provides the ability to configure, control, and monitor multiple phases on one PMBus unit. The phase selected by the PHASE command will be used for all subsequent phase dependent commands.

The PHASE command must be accessed through Read Byte/Write Byte transactions as shown in Section 2.1.2.

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
PHASE							

LEGEND: R/W = Read/Write; R = Read only

PHASE

Table 2-6. PHASE Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PHASE	RW	FFh	00h: All commands address the first phase in the selected PAGE 01h: All commands address the second phase in the selected PAGE 02h: All commands address the third phase in the selected PAGE 03h: All commands address the fourth phase in the selected PAGE 04h: All commands address the fifth phase in the selected PAGE 05h: All commands address the sixth phase in the selected PAGE 80h: Used for reading/calibrating the total phase current for the selected PAGE (IOUT_CAL_GAIN, IOUT_CAL_OFFSET, READ_IOUT only). See the product datasheet for more information FFh: Commands access all phases in the selected PAGE

Attempts to write any value other than those specified above will be treated as invalid data - invalid data will be ignored, the appropriate flags in STATUS_CML and STATUS_WORD will be set, and the PMB_ALERT will be asserted to notify the system host of an invalid transaction.

2.4.6 (10h) WRITE_PROTECT

The WRITE_PROTECT command is used to control writing to the PMBus device. The intent of this command is to provide protection against accidental changes. This command is not intended to provide protection against deliberate or malicious changes to a device's configuration or operation. All supported commands may have their parameters read, regardless of the WRITE_PROTECT settings.

The WRITE_PROTECT command must be accessed through Read Byte/Write Byte transactions as shown in Section 2.1.2.

The WRITE_PROTECT command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
WRITE_PROTECT							

LEGEND: R/W = Read/Write; R = Read only

WRITE_PROTECT

Table 2-7. WRITE_PROTECT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	WRITE_PROTECT	RW	00h	80h: Disables all WRITES except to the WRITE_PROTECT command. 40h: Disables all WRITES except to the WRITE_PROTECT, OPERATION and PAGE commands 20h: Disables all WRITES except to the WRITE_PROTECT, OPERATION, PAGE, ON_OFF_CONFIG, and VOUT_COMMAND commands. 00h: Enable writes to all commands

Commands which are write-protected according to the settings listed above will also be protected (e.g. not overwritten) from NVM restore operations via RESTORE_DEFAULT_ALL.

Attempts to write any value other than those specified above will be treated as invalid data - invalid data will be ignored, the appropriate flags in STATUS_CML and STATUS_WORD will be set, and the PMB_ALERT will be asserted to notify the system host of an invalid transaction.

2.4.7 (11h) STORE_DEFAULT_ALL

Store all of the current storable register settings in the EEPROM memory as the new defaults on power up. It is permitted to use the STORE_USER_ALL command while the device is operating. However, the device may be unresponsive during the write operation with unpredictable memory storage results. TI recommends to disabling power conversion for both channels before issuing this command.

The STORE_DEFAULT_ALL command must be accessed through the Send Byte transaction as shown in Section 2.1.2. STORE_DEFAULT_ALL is a dataless, write-only command and cannot be read.

The STORE_DEFAULT_ALL command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

2.4.8 (12h) RESTORE_DEFAULT_ALL

Write EEPROM data to those registers which: (1) have EEPROM support, and; (2) are unprotected according to current setting of the WRITE_PROTECT command. It is permitted to use the RESTORE_USER_ALL command while the device is operating. However, the device may be unresponsive during the copy operation with unpredictable, undesirable or even catastrophic results. TI recommends disabling power conversion for both channels before issuing this command.

The RESTORE_DEFAULT_ALL command must be accessed through the Send Byte transaction as shown in Section 2.1.2. RESTORE_DEFAULT_ALL is a dataless, write-only command and cannot be read.

The RESTORE_DEFAULT_ALL command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

2.4.9 (19h) CAPABILITY

The CAPABILITY command provides a way for the host to determine the capabilities of this PMBus device.

The CAPABILITY command must be accessed through Read Byte transactions as shown in Section 2.1.2.

The CAPABILITY command is shared between Channel A and Channel B. All transactions to this command apply to both channels regardless of the PAGE command.

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
PEC	SPD		PMBALRT	0	0	0	0

LEGEND: R/W = Read/Write; R = Read only

CAPABILITY

Table 2-8. CAPABILITY Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PEC	R	1b	1b: Packet Error Checking is supported.
6:5	SPD	R	10b	10b: Maximum supported bus speed is 1 MHz
4	PMBALRT	R	1b	1b: The device does have a PMB_ALERT pin and does support the SMBus Alert Response protocol.

2.4.10 (1Bh) SMBALERT_MASK

SMBALERT_MASK command may be used to prevent a warning or fault condition from asserting the PMB_ALERT pin.

The SMBALERT_MASK commands must be accessed through the Write Word protocol for write transactions, with the data byte equal to 1Bh (SMBALERT_MASK command address), and the low-order byte equal to the command address for the status register being masked. For example, to write the mask byte for STATUS_VOUT (7Ah) to 80h, use a Write Word transaction with the data byte equal to 1Bh, the low-order byte equal to 7Ah, and the and the high-order byte equal to the mask byte, 80h. Reading of mask bytes is accomplished using the Block Write/Block Read Process Call transaction as shown in Section 2.1.2.

SMBALERT_MASK is a paged register. In order to access SMBALERT_MASK commands for channel A, PAGE must be set to 00h. In order to access the SMBALERT_MASK commands for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh.

The bits in the mask byte align with the bits in the corresponding status register. For example, if the STATUS_VOUT command were sent with the mask byte 10000000b, then a VOUT_OV_FAULT condition would be blocked from asserting SMBALERT. Please refer to the PMBus v1.3 specification and the SMBus specification Block Write/Block Read protocol for further details.

Not all status bits are supported. Unsupported status bits do not trigger PMB_ALERT. Reads to the mask bits for unsupported status bits will return 0b always. Writes to unsupported mask bits will be ignored.

The mask byte for STATUS_VOUT is shown below:

7	6	5	4	3	2	1	0
RW	R	R	RW	RW	R	R	R
mVOUT_OVF	0	0	mVOUT_UVF	mVOUT_MAX_MIN	0	0	0

LEGEND: R/W = Read/Write; R = Read only

SMBALERT_MASK (STATUS_VOUT Mask Byte)

Table 2-9. SMBALERT_MASK (STATUS_VOUT Mask Byte) Register Field Descriptions

Bit	Field	Type	Reset	Description
7	mVOUT_OVF	RW	NVM	0b: VOUT overvoltage fault events on the active PAGE will assert PMB_ALERT 1b: VOUT overvoltage fault events on the active PAGE will NOT assert PMB_ALERT
4	mVOUT_UVF	RW	NVM	0b: VOUT undervoltage fault events on the active PAGE will assert PMB_ALERT 1b: VOUT undervoltage fault events on the active PAGE will NOT assert PMB_ALERT
3	mVOUT_MAX_MIN	RW	NVM	0b: VOUT_MAX_MIN warn events on the active PAGE will assert PMB_ALERT 1b: VOUT_MAX_MIN warn events on the active PAGE will NOT assert PMB_ALERT

The mask byte for STATUS_IOUT is shown below:

7	6	5	4	3	2	1	0
RW	R	RW	R	RW	R	R	R
mIOUT_OCF	0	mIOUT_OCW	0	mCUR_SHARF	0	0	0

LEGEND: R/W = Read/Write; R = Read only

SMBALERT_MASK (STATUS_IOUT Mask Byte)

Table 2-10. SMBALERT_MASK (STATUS_IOUT Mask Byte) Register Field Descriptions

Bit	Field	Type	Reset	Description
7	mIOUT_OCF	RW	NVM	0b: IOUT overcurrent fault events on the active PAGE will assert PMB_ALERT 1b: IOUT overcurrent fault events on the active PAGE will NOT assert PMB_ALERT
5	mIOUT_OCW	RW	NVM	0b: IOUT overcurrent warning events on the active PAGE will assert PMB_ALERT 1b: IOUT overcurrent warning events on the active PAGE will NOT assert PMB_ALERT
3	mCUR_SHARF	RW	NVM	0b: Current sharing fault events on the active PAGE will assert PMB_ALERT 1b: Current sharing fault events on the active PAGE will NOT assert PMB_ALERT

The mask byte for STATUS_INPUT is shown below. Note that STATUS_INPUT is not a paged register (shared by Channel A and Channel B).

7	6	5	4	3	2	1	0
RW	R	R	RW	RW	RW	RW	RW
mVIN_OVF	0	0	mVIN_UVF	mLOW_VIN	mIIN_OCF	mIIN_OCW	mPIN_OPW

LEGEND: R/W = Read/Write; R = Read only

SMBALERT_MASK (STATUS_INPUT Mask Byte)

Table 2-11. SMBALERT_MASK (STATUS_INPUT Mask Byte) Register Field Descriptions

Bit	Field	Type	Reset	Description
7	mVIN_OVF	RW	NVM	0b: VIN overvoltage fault events will assert PMB_ALERT 1b: VIN overvoltage fault events will NOT assert PMB_ALERT
4	mVIN_UVF	RW	NVM	0b: VIN undervoltage fault events will assert PMB_ALERT 1b: VIN undervoltage fault events will NOT assert PMB_ALERT
3	mLOW_VIN	RW	NVM	0b: Unit off due to insufficient input voltage will assert PMB_ALERT 1b: Unit off due to insufficient input voltage will NOT assert PMB_ALERT
2	mIIN_OCF	RW	NVM	0b: IIN overcurrent fault events will assert PMB_ALERT 1b: IIN overcurrent fault events will NOT assert PMB_ALERT
1	mIIN_OCW	RW	NVM	0b: IIN overcurrent warning events will assert PMB_ALERT 1b: IIN overcurrent warning events will NOT assert PMB_ALERT
0	mPIN_OPW	RW	NVM	0b: PIN over-power warning events will assert PMB_ALERT 1b: PIN over-power warning events will NOT assert PMB_ALERT

The mask byte for STATUS_TEMPERATURE is shown below:

7	6	5	4	3	2	1	0
RW	RW	R	R	R	R	R	R
mOTF	mOTW	0	0	0	0	0	0

LEGEND: R/W = Read/Write; R = Read only

SMBALERT_MASK (STATUS_TEMPERATURE Mask Byte)

Table 2-12. SMBALERT_MASK (STATUS_TEMPERATURE Mask Byte) Register Field Descriptions

Bit	Field	Type	Reset	Description
7	mOTF	RW	NVM	0b: Overtemperature fault events on the active PAGE will assert PMB_ALERT 1b: Overtemperature fault events on the active PAGE will NOT assert PMB_ALERT
6	mOTW	RW	NVM	0b: Overtemperature warning events on the active PAGE will assert PMB_ALERT 1b: Overtemperature warning events on the active PAGE will NOT assert PMB_ALERT

The mask byte for STATUS_CML is shown below. Note that STATUS_CML is not a paged register (shared by channel A and channel B).

7	6	5	4	3	2	1	0
RW	RW	R	R	R	R	R	R
mIVC	mIVD	mPECF	mMEMF	0	0	mCOMF	0

LEGEND: R/W = Read/Write; R = Read only

SMBALERT_MASK (STATUS_CML Mask Byte)

Table 2-13. SMBALERT_MASK (STATUS_CML Mask Byte) Register Field Descriptions

Bit	Field	Type	Reset	Description
7	mIVC	RW	NVM	0b: Invalid command fault events will assert PMB_ALERT 1b: Invalid command fault events will NOT assert PMB_ALERT
6	mIVD	RW	NVM	0b: Invalid data fault events will assert PMB_ALERT 1b: Invalid data fault events will NOT assert PMB_ALERT
5	mPECF	RW	NVM	0b: Invalid PEC byte events will assert PMB_ALERT 1b: Invalid PEC byte events PAGE will NOT assert PMB_ALERT
4	mMEMF	RW	NVM	0b: Memory fault events will assert PMB_ALERT 1b: Memory fault events will NOT assert PMB_ALERT
1	mCOMF	RW	NVM	0b: Communication fault events will assert PMB_ALERT 1b: Communication fault events will NOT assert PMB_ALERT

The mask byte for STATUS_MFR_SPECIFIC is shown below:

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	R	R	RW
mFLT_PS	mVSNS_OPEN	mMAX_PHASE	mTSNS_LOW	mRST_VID	0	0	mPHFLT

LEGEND: R/W = Read/Write; R = Read only

SMBALERT_MASK (STATUS_MFR_SPECIFIC Mask Byte)

Table 2-14. SMBALERT_MASK (STATUS_MFR_SPECIFIC Mask Byte) Register Field Descriptions

Bit	Field	Type	Reset	Description
7	mFLT_PS	RW	NVM	0b: Power stage fault events on the active PAGE will assert PMB_ALERT 1b: Power stage fault events on the active PAGE will NOT assert PMB_ALERT
6	mVSNS_OPEN	RW	NVM	0b: VSNS open on the active PAGE will assert PMB_ALERT 1b: VSNS open on the active PAGE will NOT assert PMB_ALERT

Table 2-14. SMBALERT_MASK (STATUS_MFR_SPECIFIC Mask Byte) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	mMAX_PHASE	RW	NVM	0b: MAX_PHASE events on the active PAGE will assert PMB_ALERT 1b: MAX_PHASE events on the active PAGE will NOT assert PMB_ALERT
4	mTSNS_LOW	RW	NVM	0b: TSNS open on the active PAGE will assert PMB_ALERT 1b: TSNS open on the active PAGE will NOT assert PMB_ALERT
3	mRST_VID	RW	NVM	0b: RST_VID events on the active PAGE will assert PMB_ALERT 1b: RST_VID events on the active PAGE will NOT assert PMB_ALERT
0	mPHFLT	RW	NVM	0b: Phase current share fault events on the active PAGE will assert PMB_ALERT 1b: Phase current share fault events on the active PAGE will NOT assert PMB_ALERT

2.4.11 (20h) VOUT_MODE

The VOUT_MODE command indicates that the output voltage related commands for TPS53681 are in the VID format.

The VOUT_MODE command must be accessed through Read Byte transactions as shown in Section 2.1.2.

The VOUT_MODE command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
MODE			VID_TYPE				

LEGEND: R/W = Read/Write; R = Read only

VOUT_MODE

Table 2-15. VOUT_MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	MODE	R	001b	VID Format.
4:0	VID_TYPE	R	See Product Datasheet.	00100b: 10-mV DAC Mode 00111b: 5-mV DAC Mode Note that VOUT_MODE is read-only, however the VID_TYPE field will be updated when the VID Table is changed via the VR_MODE bits in MFR_SPECIFIC_13.

2.4.12 (21h) VOUT_COMMAND

VOUT_COMMAND is used to set the output voltage of the active PAGE.

VOUT_COMMAND is a VID format command, as described in Section 2.1.1.

VOUT_COMMAND command must be accessed through Read Word/Write Word transactions as shown in Section 2.1.2.

VOUT_COMMAND is a paged register. In order to access VOUT_COMMAND for channel A, PAGE must be set to 00h. In order to access the VOUT_COMMAND register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh.

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VOUT_CMD_VID							

LEGEND: R/W = Read/Write; R = Read only

VOUT_COMMAND

Table 2-16. VOUT_COMMAND Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VOUT_CMD_VID	RW	NVM	Used to set the commanded VOUT. Cannot be set to a level above the value set by VOUT_MAX.

2.4.13 (24h) VOUT_MAX

The VOUT_MAX command sets an upper limit on the output voltage that the unit may be commanded to, regardless of an other commands or combinations. The intent of this command is to provide a safeguard against a user accidentally setting the output voltage to a possibly destructive level.

The device detects that an attempt has been made to program the output to a voltage greater than the value set by the VOUT_MAX command. Attempts to program the output voltage greater than VOUT_MAX can include VOUT_COMMAND attempts, and margin events while the VOUT_MARGIN_HIGH/VOUT_MARGIN_LOW values exceed the value of VOUT_MAX. These events will be treated warning conditions and not as fault conditions. If an attempt is made to program the output voltage higher than the limit set by the VOUT_MAX command, the device will respond as follows:

- The commanded output voltage will be clamped to VOUT_MAX,
- The OTHER bit will be set in the STATUS_BYTE,
- The VOUT bit will be set in the STATUS_WORD,
- The VOUT_MAX warning bit will be set in the STATUS_VOUT register, and
- The device notifies the host (asserts PMB_ALERT, if the corresponding mask bit in SMBALERT_MASK is not set).

VOUT_MAX is a VID format command, as described in Section 2.1.1.

The VOUT_MAX command must be accessed through Read Word/Write Word transactions as shown in Section 2.1.2.

VOUT_MAX is a paged register. In order to access VOUT_MAX for channel A, PAGE must be set to 00h. In order to access the VOUT_COMMAND register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh.

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VOUT_MAX_VID							

LEGEND: R/W = Read/Write; R = Read only

VOUT_MAX

Table 2-17. VOUT_MAX Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VOUT_MAX_VID	RW	NVM	Used to set the maximum VOUT of the device in VID format.

2.4.14 (25h) VOUT_MARGIN_HIGH

The VOUT_MARGIN_HIGH command loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to “Margin High”.

VOUT_MARGIN_HIGH is a VID format command, as described in Section 2.1.1.

The VOUT_MARGIN_HIGH command must be accessed through Read Word/Write Word transactions as shown in Section 2.1.2.

VOUT_MARGIN_HIGH is a paged register. In order to access VOUT_MARGIN_HIGH for channel A, PAGE must be set to 00h. In order to access the VOUT_MARGIN_HIGH register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh.

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VOUT_MARGH_VID							

LEGEND: R/W = Read/Write; R = Read only

VOUT_MARGIN_HIGH

Table 2-18. VOUT_MARGIN_HIGH Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VOUT_MARGH_VID	RW	00h	Used to set the output voltage to be loaded when the active PAGE is set to Margin High in VID format.

2.4.15 (26h) VOUT_MARGIN_LOW

The VOUT_MARGIN_LOW command loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to “Margin Low”.

VOUT_MARGIN_LOW is a VID format command, as described in Section 2.1.1.

The VOUT_MARGIN_LOW command must be accessed through Read Word/Write Word transactions as shown in Section 2.1.2.

VOUT_MARGIN_LOW is a paged register. In order to access VOUT_MARGIN_LOW for channel A, PAGE must be set to 00h. In order to access the VOUT_MARGIN_LOW register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh.

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VOUT_MARGL_VID							

LEGEND: R/W = Read/Write; R = Read only

VOUT_MARGIN_LOW

Table 2-19. VOUT_MARGIN_LOW Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VOUT_MARGL_VID	RW	00h	Used to set the output voltage to be loaded when the active PAGE is set to Margin Low, in VID format.

2.4.16 (27h) VOUT_TRANSITION_RATE

When the TPS53681 receives either a VOUT_COMMAND or OPERATION (Margin High, Margin Low, Margin Off) that causes the output voltage to change, this command sets the rate in mV/µs at which the output should change voltage. This commanded rate of change does not apply when the unit is commanded to turn on or to turn off (e.g. soft-start, or shutdown).

VOUT_TRANSITION_RATE is a linear format command, as described in Section 2.1.1.

The VOUT_TRANSITION_RATE command must be accessed through Read Word/Write Word transactions as shown in Section 2.1.2.

VOUT_TRANSITION_RATE is a paged register. In order to access VOUT_TRANSITION_RATE for channel A, PAGE must be set to 00h. In order to access the VOUT_TRANSITION_RATE register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh.

15	14	13	12	11	10	9	8
R	R	R	R	R	RW	RW	RW
VOTR_EXP					VOTR_MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VOTR_MAN							

LEGEND: R/W = Read/Write; R = Read only

VOUT_TRANSITION_RATE

Table 2-20. VOUT_TRANSITION_RATE Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	VOTR_EXP	R	11100b	Linear two's complement fixed exponent, –4. LSB = 0.0625 mV/µs
10:0	VOTR_MAN	RW	NVM	Linear two's complement mantissa. See table of acceptable values below.

Attempts to write any value other than those specified below will be treated as invalid data - invalid data will be ignored, the appropriate flags in STATUS_CML and STATUS_WORD will be set, and the PMB_ALERT will be asserted to notify the system host of an invalid transaction.

Table 2-21. Acceptable VOUT_TRANSITION_RATE Values

VOUT_TRANSITION_RATE (hex)	Slew Rate (mV/µs)
E005h	0.3125
E00Ah	0.625
E00Fh	0.9375
E014h	1.25
E019h	1.5625
E01Eh	1.875
E023h	2.1875
E028h	2.5
E050h	5
E0A0h	10
E0F0h	15
E140h	20
E190h	25
E1E0h	30
E230h	35
E280h	40

2.4.17 (28h) VOUT_DROOP

The VOUT_DROOP command sets the rate, in mV/A (mΩ) at which the output voltage decreases (or increases) with increasing (or decreasing) output current for use with adaptive voltage positioning. This is also referred to as the DC Load Line (DCLL).

VOUT_DROOP is a linear format command, as described in Section 2.1.1.

The VOUT_DROOP command must be accessed through Read Word/Write Word transactions as shown in Section 2.1.2.

VOUT_DROOP is a paged register. In order to access VOUT_DROOP for channel A, PAGE must be set to 00h. In order to access the VOUT_DROOP register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh.

15	14	13	12	11	10	9	8
R	R	R	R	R	RW	RW	RW
VDROOP_EXP					VDROOP_MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VDROOP_MAN							

LEGEND: R/W = Read/Write; R = Read only

VOUT_DROOP

Table 2-22. VOUT_DROOP Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	VDROOP_EXP	R	11010b	Linear two's complement fixed exponent, –6. LSB = 0.015625 mΩ
10:0	VDROOP_MAN	RW	NVM	Linear two's complement mantissa. See table of acceptable values below, note that Channel A and Channel B support different acceptable values of VOUT_DROOP.

The table below summarizes the acceptable values of VOUT_DROOP for channel A and channel B. Attempts to write any value other than those specified below will be treated as invalid data - invalid data will be ignored, the appropriate flags in STATUS_CML and STATUS_WORD will be set, and the PMB_ALERT will be asserted to notify the system host of an invalid transaction.

Table 2-23. Acceptable VOUT_DROOP Values

Bin	VOUT_DROOP (hex)	Supported by Channel A	Supported by Channel B	DC Load Line (mΩ)
0	D000h	Yes	Yes	0
1	D008h	Yes	Yes	0.125
2	D010h	Yes	Yes	0.25
3	D014h	Yes	Yes	0.3125
4	D018h	Yes	Yes	0.375
5	D01Ch	Yes	Yes	0.4375
6	D020h	Yes	Yes	0.5
7	D024h	Yes	Yes	0.5625
8	D028h	Yes	Yes	0.625
9	D030h	Yes	Yes	0.703125
10	D033h	Yes	Yes	0.7969
11	D034h	Yes	Yes	0.8125
12	D035h	Yes	Yes	0.8281
13	D036h	Yes	Yes	0.8438
14	D037h	Yes	Yes	0.8594

Table 2-23. Acceptable VOUT_DROOP Values (continued)

Bin	VOUT_DROOP (hex)	Supported by Channel A	Supported by Channel B	DC Load Line (mΩ)
15	D038h	Yes	Yes	0.875
16	D039h	Yes	No	0.8906
17	D03Ah	Yes	No	0.9063
18	D03Bh	Yes	No	0.9219
19	D03Ch	Yes	No	0.9375
20	D03Dh	Yes	No	0.9531
21	D03Eh	Yes	No	0.9688
22	D03Fh	Yes	No	0.9844
23	D040h	Yes	No	1
24	D041h	Yes	No	1.0156
25	D042h	Yes	No	1.0313
26	D043h	Yes	No	1.0469
27	D044h	Yes	No	1.0625
28	D048h	Yes	No	1.125
29	D050h	Yes	No	1.25
30	D058h	Yes	No	1.375
31	D060h	Yes	No	1.5
32	D068h	Yes	No	1.625
33	D070h	Yes	No	1.75
34	D078h	Yes	No	1.875
35	D07Ch	Yes	No	1.9375
36	D080h	Yes	No	2
37	D084h	Yes	No	2.0625
38	D088h	Yes	No	2.125
39	D08Ch	Yes	No	2.1875
40	D090h	Yes	No	2.25
41	D098h	Yes	No	2.375
42	D09Bh	Yes	No	2.4218
43	D09Ch	Yes	No	2.4375
44	D09Dh	Yes	No	2.4531
45	D09Eh	Yes	No	2.4687
46	D09Fh	Yes	No	2.4843
47	D0A0h	Yes	No	2.5
48	D0A1h	Yes	No	2.5156
49	D0A2h	Yes	No	2.5312
50	D0A3h	Yes	No	2.5468
51	D0A4h	Yes	No	2.5625
52	D0A5h	Yes	No	2.5781
53	D0A6h	Yes	No	2.5937
54	D0A7h	Yes	No	2.609
55	D0A8h	Yes	No	2.625
56	D0A9h	Yes	No	2.6406
57	D0AAh	Yes	No	2.6562
58	D0ABh	Yes	No	2.6718
59	D0ACh	Yes	No	2.6875
60	D0B0h	Yes	No	2.75
61	D0B8h	Yes	No	2.875

Table 2-23. Acceptable VOUT_DROOP Values (continued)

Bin	VOUT_DROOP (hex)	Supported by Channel A	Supported by Channel B	DC Load Line (mΩ)
62	D0C0h	Yes	No	3
63	D0C8h	Yes	No	3.125

2.4.18 (29h) VOUT_SCALE_LOOP

VOUT_SCALE_LOOP is used to scale output voltage related commands. VOUT_SCALE_LOOP will affect the behavior of the following commands:

- VOUT_COMMAND
- VOUT_MARGIN_HIGH
- VOUT_MARGIN_LOW
- VOUT_OV_FAULT_LIMIT
- VOUT_UV_FAULT_LIMIT
- VOUT_MAX
- VOUT_MIN

For example: VOUT = LOOKUP(VOUT_CMD_VID)× VOUT_SCALE_LOOP

VOUT_SCALE_LOOP is a linear format command, as described in Section 2.1.1.

The VOUT_SCALE_LOOP command must be accessed through Read Word/Write Word transactions as shown in Section 2.1.2.

VOUT_SCALE_LOOP is a paged register. In order to access VOUT_SCALE_LOOP for channel A, PAGE must be set to 00h. In order to access the VOUT_SCALE_LOOP register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh.

NOTE: Writes to the VOUT_SCALE_LOOP command will also update the VOUT_SCALE_MONITOR command.

15	14	13	12	11	10	9	8
R	R	R	R	R	RW	RW	RW
VOSL_EXP					VOSL_MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VOSL_MAN							

LEGEND: R/W = Read/Write; R = Read only

VOUT_SCALE_LOOP

Table 2-24. VOUT_SCALE_LOOP Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	VOSL_EXP	R	11101b	Linear two's complement fixed exponent, –3. LSB = 0.125
10:0	VOSL_MAN	RW	NVM	08h: VOUT_SCALE_LOOP = 1 09h: VOUT_SCALE_LOOP = 1.125

Attempts to write any value other than those specified above will be treated as invalid data - invalid data will be ignored, the appropriate flags in STATUS_CML and STATUS_WORD will be set, and the PMB_ALERT will be asserted to notify the system host of an invalid transaction.

2.4.19 (2Ah) VOUT_SCALE_MONITOR

VOUT_SCALE_MONITOR is used to scale the output voltage readings appropriately into the VID format, for the READ_VOUT command.

VOUT_SCALE_MONITOR is a linear format command, as described in Section 2.1.1.

The VOUT_SCALE_MONITOR command must be accessed through Read Word/Write Word transactions as shown in Section 2.1.2.

VOUT_SCALE_MONITOR is a paged register. In order to access VOUT_SCALE_MONITOR for channel A, PAGE must be set to 00h. In order to access the VOUT_SCALE_MONITOR register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh.

NOTE: Writes to the VOUT_SCALE_LOOP command will also update the VOUT_SCALE_MONITOR command.

15	14	13	12	11	10	9	8
R	R	R	R	R	RW	RW	RW
VOSM_EXP					VOSM_MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VOSM_MAN							

LEGEND: R/W = Read/Write; R = Read only

VOUT_SCALE_MONITOR

Table 2-25. VOUT_SCALE_MONITOR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	VOSL_EXP	R	11101b	Linear two's complement fixed exponent, –3. LSB = 0.125
10:0	VOSL_MAN	RW	NVM	08h: VOUT_SCALE_MONITOR = 1 09h: VOUT_SCALE_MONITOR = 1.125

Attempts to write any value other than those specified above will be treated as invalid data - invalid data will be ignored, the appropriate flags in STATUS_CML and STATUS_WORD will be set, and the PMB_ALERT will be asserted to notify the system host of an invalid transaction.

2.4.20 (2Bh) VOUT_MIN

The VOUT_MIN command sets a lower bound on the output voltage to which the unit can be commanded, regardless of any other commands or combinations. The intent of this command is to provide a safeguard against a user accidentally setting the output voltage to a possibly destructive level rather than to be the primary output under voltage protection.

If an attempt is made to program the output voltage lower than the limit set by this command, the device will respond as follows:

- The commanded output voltage will be clamped to VOUT_MIN
- The OTHER bit will be set in the STATUS_BYTE
- The VOUT bit will be set in the STATUS_WORD
- The VOUT_MAX_MIN Warning bit will be set in the STATUS_VOUT register
- The device notifies the host (asserts PMB_ALERT, if the corresponding mask bit in SMBALERT_MASK is not set).

VOUT_MIN is a VID format command, as described in Section 2.1.1.

The VOUT_MIN command must be accessed through Read Word/Write Word transactions as shown in Section 2.1.2.

VOUT_MIN is a paged register. In order to access VOUT_MIN for channel A, PAGE must be set to 00h. In order to access the VOUT_MIN register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh.

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VOUT_MIN_VID							

LEGEND: R/W = Read/Write; R = Read only

VOUT_MIN

Table 2-26. VOUT_MIN Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VOUT_MIN_VID	RW	NVM	Used to set a lower bound for output voltage programming for the active PAGE, is set to in VID format.

2.4.21 (33h) FREQUENCY_SWITCH

The FREQUENCY_SWITCH command sets the per-phase switching frequency in kHz for the active PAGE.

FREQUENCY_SWITCH is a linear format command, as described in Section 2.1.1.

The FREQUENCY_SWITCH command must be accessed through Read Word/Write Word transactions as shown in Section 2.1.2.

FREQUENCY_SWITCH is a paged register. In order to access FREQUENCY_SWITCH for channel A, PAGE must be set to 00h. In order to access the FREQUENCY_SWITCH register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh.

15	14	13	12	11	10	9	8
R	R	R	R	R	RW	RW	RW
FSW_EXP					FSW_MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
FSW_MAN							

LEGEND: R/W = Read/Write; R = Read only

FREQUENCY_SWITCH

Table 2-27. FREQUENCY_SWITCH Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	FSW_EXP	R	00000b	Linear two's complement exponent, 0. LSB = 1 kHz
10:0	FSW_MAN	RW	NVM	Linear two's complement mantissa. See the table of acceptable values below.

Table 2-28. Acceptable values for FREQUENCY_SWITCH

FREQUENCY_SWITCH (hex)	Switching Frequency (kHz)
012Ch	300
015Eh	350
0190h	400
01C2h	450
01F4h	500
0226h	550
0258h	600
028Ah	650
02BCh	700
02EEh	750
0320h	800
0352h	850
0384h	900
03B6h	950
03E8h	1000

Attempts to write any value other than those specified above will be treated as invalid data - invalid data will be ignored, the appropriate flags in STATUS_CML and STATUS_WORD will be set, and the PMB_ALERT will be asserted to notify the system host of an invalid transaction.

2.4.22 (35h) VIN_ON

The VIN_ON command sets the value of the input voltage, in Volts, at which the unit should start power conversion. This command has two data bytes encoded in linear data format. The supported range for VIN_ON is from 4.0 V volts to 11.25 Volts

VIN_ON is a linear format command, as described in Section 2.1.1.

The VIN_ON command must be accessed through Read Word/Write Word transactions as shown in Section 2.1.2.

The VIN_ON command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

15	14	13	12	11	10	9	8
R	R	R	R	R	RW	RW	RW
VINON_EXP					VINON_MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VINON_MAN							

LEGEND: R/W = Read/Write; R = Read only

VIN_ON

Table 2-29. VIN_ON Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	VINON_EXP	R	11110b	Linear two's complement exponent, –2. LSB = 0.25 V
10:0	VINON_MAN	RW	NVM	Linear two's complement mantissa. See the table of acceptable values below.

Table 2-30. Acceptable Values of VIN_ON

VIN_ON (hex)	Turn-On Voltage (V)
F010h	4.0
F015h	5.25
F019h	6.25
F01Dh	7.25
F021h	8.25
F025h	9.25
F029h	10.25
F02Dh	11.25

Attempts to write any value other than those specified above will be treated as invalid data - invalid data will be ignored, the appropriate flags in STATUS_CML and STATUS_WORD will be set, and the PMB_ALERT will be asserted to notify the system host of an invalid transaction.

2.4.23 (38h) IOUT_CAL_GAIN

The IOUT_CAL_GAIN command is used to set the ratio of the voltage at the current sense pins to the sensed current, in mΩ.

IOUT_CAL_GAIN is a linear format command, as described in Section 2.1.1.

The IOUT_CAL_GAIN command must be accessed through Read Word/Write Word transactions as shown in Section 2.1.2.

IOUT_CAL_GAIN is a paged register. In order to access IOUT_CAL_GAIN for channel A, PAGE must be set to 00h. In order to access the IOUT_CAL_GAIN register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh. PHASE must also be set to 80h to apply IOUT_CAL_GAIN to the total phase current measurement, as described in the product datasheet. Having different values of IOUT_CAL_GAIN for each phase is not supported.

15	14	13	12	11	10	9	8
R	R	R	R	R	RW	RW	RW
IOCG_EXP					IOCG_MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
IOCG_MAN							

LEGEND: R/W = Read/Write; R = Read only

IOUT_CAL_GAIN

Table 2-31. IOUT_CAL_GAIN Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	IOCG_EXP	R	11010b	Linear two's complement exponent, –6. LSB = 0.015625 mΩ
10:0	IOCG_MAN	RW	NVM	Linear two's complement mantissa. See the table of acceptable values below.

Table 2-32. Acceptable Values of IOUT_CAL_GAIN

IOUT_CAL_GAIN (hex)	Current Sense Gain (mΩ)
D131h	4.765625
D132h	4.78125
D133h	4.796875
D134h	4.8125
D135h	4.828125
D136h	4.84375
D137h	4.859375
D138h	4.875
D139h	4.890625
D13Ah	4.90625
D13Bh	4.921875
D13Ch	4.9375
D13Dh	4.953125
D13Eh	4.96875
D13Fh	4.984375
D140h	5
D141h	5.015625
D142h	5.03125
D143h	5.046875
D144h	5.0625

Table 2-32. Acceptable Values of IOUT_CAL_GAIN (continued)

IOUT_CAL_GAIN (hex)	Current Sense Gain (mΩ)
D145h	5.078125
D146h	5.09375
D147h	5.109375
D148h	5.125
D149h	5.140625
D14Ah	5.15625
D14Bh	5.171875
D14Ch	5.1875
D14Dh	5.203125
D14Eh	5.21875
D14Fh	5.234375
D150h	5.25

Attempts to write any value other than those specified above will be treated as invalid data - invalid data will be ignored, the appropriate flags in STATUS_CML and STATUS_WORD will be set, and the PMB_ALERT will be asserted to notify the system host of an invalid transaction.

2.4.24 (39h) IOUT_CAL_OFFSET

The IOUT_CAL_OFFSET command is used to compensate for offset errors in the READ_IOUT telemetry, in Amperes.

IOUT_CAL_OFFSET is a linear format command, as described in Section 2.1.1.

The IOUT_CAL_OFFSET command must be accessed through Read Word/Write Word transactions as shown in Section 2.1.2.

IOUT_CAL_OFFSET is a paged register. In order to access IOUT_CAL_OFFSET for channel A, PAGE must be set to 00h. In order to access the IOUT_CAL_OFFSET register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh. IOUT_CAL_OFFSET is also a phased register. Depending on the configuration of the design, for channel A, PHASE must be set to 00h to access Phase 1, 01h to access Phase 2, etc... PHASE must be set to FFh to access all phases simultaneously. PHASE may also be set to 80h to apply IOUT_CAL_OFFSET to the total phase current (sum of all active phases for the current channel) measurement, as described in . Unlike IOUT_CAL_GAIN, phases may have individual IOUT_CAL_OFFSET values.

15	14	13	12	11	10	9	8
R	R	R	R	R	RW	RW	RW
IOCOS_EXP					IOCOS_MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
IOCOS_MAN							

LEGEND: R/W = Read/Write; R = Read only

IOUT_CAL_OFFSET

Table 2-33. IOUT_CAL_OFFSET Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	IOCOS_EXP	R	11101b	Linear two's complement exponent, –3. LSB = 0.125 A
10:0	IOCOS_MAN	RW	NVM	Linear two's complement mantissa. See the table of acceptable values below. Note that there is a different set of acceptable values for individual phases (e.g. PHASE = 00h - 05h, and FFh) vs. the total current telemetry function (e.g. PHASE = 80h). See for more information.

Table 2-34. Acceptable Values of IOUT_CAL_OFFSET (Individual Phases, PHASE ≠ 80h)

IOUT_CAL_OFFSET (hex)	Current Sense Offset (A)
E800h	0.00
E801h	0.125
E802h	0.25
E803h	0.375
E804h	0.5
E805h	0.625
E806h	0.75
E807h	0.875
E808h	1.0
EFF9h	-0.875
EFFAh	-0.75
EFFBh	-0.625
EFFCh	-0.5
EFFDh	-0.375
EFFEh	-0.25

Table 2-34. Acceptable Values of IOUT_CAL_OFFSET (Individual Phases, PHASE ≠ 80h) (continued)

IOUT_CAL_OFFSET (hex)	Current Sense Offset (A)
EFFFh	-0.125

Table 2-35. Acceptable Values of IOUT_CAL_OFFSET (Total Current, PHASE = 80h)

IOUT_CAL_OFFSET (hex)	Current Sense Offset (A)
E800h	0.00
E802h	0.25
E804h	0.5
E806h	0.75
E808h	1.0
E80Ah	1.25
E80Ch	1.5
E80Eh	1.75
E810h	2.0
E812h	2.25
E814h	2.5
E816h	2.75
E818h	3.0
E81Ah	3.25
E81Ch	3.5
E81Eh	3.75
E820h	4.0
EFE2h	-3.75
EFE4h	-3.5
EFE6h	-3.25
EFE8h	-3.0
EFEAh	-2.75
EFECh	-2.5
EFEEh	-2.25
EFF0h	-2.0
EFF2h	-1.75
EFF4h	-1.5
EFF6h	-1.25
EFF8h	-1.0
EFFAh	-0.75
EFFCh	-0.5
EFFEh	-0.25

Attempts to write any value other than those specified above will be treated as invalid data - invalid data will be ignored, the appropriate flags in STATUS_CML and STATUS_WORD will be set, and the PMB_ALERT will be asserted to notify the system host of an invalid transaction.

2.4.25 (40h) VOUT_OV_FAULT_LIMIT

The VOUT_OV_FAULT_LIMIT is used to read back the value of the output voltage measured at the sense or output pins that causes an output overvoltage fault.

VOUT_OV_FAULT_LIMIT is a VID format command, as described in Section 2.1.1.

The VOUT_OV_FAULT_LIMIT command must be accessed through Read Word/Write Word transactions as shown in Section 2.1.2.

VOUT_OV_FAULT_LIMIT is a paged register. In order to access VOUT_OV_FAULT_LIMIT for channel A, PAGE must be set to 00h. In order to access the VOUT_OV_FAULT_LIMIT register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh.

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
VO_OVF_VID							

LEGEND: R/W = Read/Write; R = Read only

VOUT_OV_FAULT_LIMIT

Table 2-36. VOUT_OV_FAULT_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VO_OVF_VID	R	Refer to product datasheet.	Read-only overvoltage fault limit, in VID format.

Attempts to write to this command will be treated as invalid transactions - any data will be ignored, the appropriate flags in STATUS_CML and STATUS_WORD will be set, and the PMB_ALERT will be asserted to notify the system host of an invalid transaction.

2.4.26 (41h) VOUT_OV_FAULT_RESPONSE

The VOUT_OV_FAULT_RESPONSE instructs the device on what action to take in response to an output overvoltage fault.

Upon triggering the over-voltage fault, the controller is latched off, and the following actions are taken:

- Set the VOUT_OV_FAULT bit in the STATUS_BYTE
- Set the VOUT bit in the STATUS_WORD
- Set the VOUT_OV_FAULT bit in the STATUS_VOUT register
- The device notifies the host (asserts PMB_ALERT, if the corresponding mask bit in SMBALERT_MASK is not set)

The VOUT_OV_FAULT_RESPONSE command must be accessed through Read Byte transactions as shown in Section 2.1.2.

The VOUT_OV_FAULT_RESPONSE command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
VO_OV_RESP							

LEGEND: R/W = Read/Write; R = Read only

VOUT_OV_FAULT_RESPONSE

Table 2-37. VOUT_OV_FAULT_RESPONSE Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VO_OV_RESP	R	80h	80h: Latch-off and do not restart. To clear a shutdown event due to a fault event, the user must toggle the AVR_EN/BEN pin and/or the ON bit in OPERATION, per the settings in ON_OFF_CONFIG, or power cycle the bias power to the V3P3 pin of the controller device.

Attempts to write to this command will be treated as invalid transactions - any data will be ignored, the appropriate flags in STATUS_CML and STATUS_WORD will be set, and the PMB_ALERT will be asserted to notify the system host of an invalid transaction.

2.4.27 (44h) VOUT_UV_FAULT_LIMIT

The VOUT_UV_FAULT_LIMIT is used to read back the value of the output voltage measured at the sense or output pins that causes an output undervoltage fault in VID format.

VOUT_UV_FAULT_LIMIT is a VID format command, as described in Section 2.1.1.

The VOUT_UV_FAULT_LIMIT command must be accessed through Read Word transactions as shown in Section 2.1.2.

VOUT_UV_FAULT_LIMIT is a paged register. In order to access VOUT_UV_FAULT_LIMIT for channel A, PAGE must be set to 00h. In order to access the VOUT_UV_FAULT_LIMIT register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh.

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
VO_UVF_VID							

LEGEND: R/W = Read/Write; R = Read only

VOUT_UV_FAULT_LIMIT

Table 2-38. VOUT_UV_FAULT_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VO_UVF_VID	R	Refer to product datasheet.	Read-only undervoltage fault limit, in VID format.

Attempts to write to this command will be treated as invalid transactions - any data will be ignored, the appropriate flags in STATUS_CML and STATUS_WORD will be set, and the PMB_ALERT will be asserted to notify the system host of an invalid transaction.

2.4.28 (45h) VOUT_UV_FAULT_RESPONSE

The VOUT_UV_FAULT_RESPONSE instructs the device on what action to take in response to an output undervoltage fault.

Upon triggering the undervoltage fault, the following actions are taken:

- Set the OTHER bit in the STATUS_BYTE
- Set the VOUT bit in the STATUS_WORD
- Set the VOUT_UV_FAULT bit in the STATUS_VOUT register
- The device notifies the host (asserts PMB_ALERT, if the corresponding mask bit in SMBALERT_MASK is not set)

The VOUT_UV_FAULT_RESPONSE command must be accessed through Read Byte/Write Byte transactions as shown in Section 2.1.2.

The VOUT_UV_FAULT_RESPONSE command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VO_UV_RESP							

LEGEND: R/W = Read/Write; R = Read only

VOUT_UV_FAULT_RESPONSE

Table 2-39. VOUT_UV_FAULT_RESPONSE Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VO_UV_RESP	RW	NVM	00h: Ignore. The controller will set the appropriate status bits, and alert the host, but continue converting power. BAh: Shutdown and restart. The controller will shutdown the channel on which the fault occurred, and attempt to restart 20ms later. This will occur continuously until the condition causing the fault has disappeared, or the controller has been disabled. 80h: Latch-off and do not restart. To clear a shutdown event due to a fault event, the user must toggle the AVR_EN/BEN pin and/or the ON bit in OPERATION, per the settings in ON_OFF_CONFIG, or power cycle the bias power to the V3P3 pin of the controller device.

Attempts to write any value other than those specified above will be treated as invalid data - invalid data will be ignored, the appropriate flags in STATUS_CML and STATUS_WORD will be set, and the PMB_ALERT will be asserted to notify the system host of an invalid transaction.

2.4.29 (46h) IOUT_OC_FAULT_LIMIT

The IOUT_OC_FAULT_LIMIT command sets the value of the total output current, in amperes, that causes the over-current detector to indicate an over-current fault condition. The command has two data bytes and the data format is Linear as shown in the table below. The units are amperes.

IOUT_OC_FAULT_LIMIT is a linear format command, as described in Section 2.1.1.

The IOUT_OC_FAULT_LIMIT command must be accessed through Read Word/Write Word transactions as shown in Section 2.1.2.

IOUT_OC_FAULT_LIMIT is a paged register. In order to access IOUT_OC_FAULT_LIMIT command for channel A, PAGE must be set to 00h. In order to access IOUT_OC_FAULT_LIMIT register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh.

15	14	13	12	11	10	9	8
R	R	R	R	R	RW	RW	RW
IOOCF_EXP					IOOCF_MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
IOOCF_MAN							

LEGEND: R/W = Read/Write; R = Read only

IOUT_OC_FAULT_LIMIT

Table 2-40. IOUT_OC_FAULT_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	IOOCF_EXP	R	00000b	Linear two's complement exponent, 0. LSB = 1.0 A
10:0	IOOCF_MAN	RW	See below.	Linear two's complement mantissa

At power-on, or after a RESTORE_DEFAULT_ALL operation, the IOUT_OC_FAULT_LIMIT command will be loaded with the value of IOUTMAX × 1.25. The IOUTMAX bits for each channel are stored in MFR_SPECIFIC_10 (PAGE 0 for channel A, PAGE 1 for channel B). IOUT_OC_FAULT_LIMIT may be changed during operation, but will return to this value on reset.

Attempts to write any value other than 00000b to the exponent bits will be treated as invalid data - invalid data will be ignored, the appropriate flags in STATUS_CML and STATUS_WORD will be set, and the PMB_ALERT will be asserted to notify the system host of an invalid transaction.

2.4.30 (47h) IOUT_OC_FAULT_RESPONSE

The IOUT_OC_FAULT_RESPONSE instructs the device on what action to take in response to an output over-current fault. Upon triggering the over-current fault, the controller is latched off, and the following actions are taken:

- Set the IOUT_OC_FAULT bit in the STATUS_BYTE
- Set the IOUT bit in the STATUS_WORD
- Set the IOUT_OC_FAULT bit in the STATUS_IOUT register
- The device notifies the host (asserts PMB_ALERT, if the corresponding mask bit in SMBALERT_MASK is not set)

The IOUT_OC_FAULT_RESPONSE command must be accessed through Read Byte/Write Byte transactions as shown in Section 2.1.2.

The IOUT_OC_FAULT_RESPONSE command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
IO_OC_RESP							

LEGEND: R/W = Read/Write; R = Read only

IOUT_OC_FAULT_RESPONSE

Table 2-41. IOUT_OC_FAULT_RESPONSE Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	IO_OC_RESP	RW	NVM	C0h: Latch-off and do not restart. To clear a shutdown event due to a fault event, the user must toggle the AVR_EN/BEN pin and/or the ON bit in OPERATION, per the settings in ON_OFF_CONFIG, or power cycle the bias power to the V3P3 pin of the controller device. FAh: Shutdown and restart. The controller will shutdown the channel on which the fault occurred, and attempt to restart 20ms later. This will occur continuously until the condition causing the fault has disappeared, or the controller has been disabled.

Attempts to write any value other than those specified above will be treated as invalid data - invalid data will be ignored, the appropriate flags in STATUS_CML and STATUS_WORD will be set, and the PMB_ALERT will be asserted to notify the system host of an invalid transaction.

2.4.31 (4Ah) IOUT_OC_WARN_LIMIT

The IOUT_OC_WARN_LIMIT command sets the value of the output current, in amperes, that causes the over-current detector to indicate an over-current warning condition. Upon triggering the overcurrent warning, the following actions are taken:

- Set the OTHER bit in the STATUS_BYTE
- Set the IOUT bit in the STATUS_WORD
- Set the IOUT Over current Warning bit in the STATUS_IOUT register
- The device notifies the host (asserts PMB_ALERT, if the corresponding mask bit in SMBALERT_MASK is not set)

IOUT_OC_WARN_LIMIT is a linear format command, as described in Section 2.1.1.

The IOUT_OC_WARN_LIMIT command must be accessed through Read Word/Write Word transactions as shown in Section 2.1.2.

IOUT_OC_WARN_LIMIT is a paged register. In order to access IOUT_OC_WARN_LIMIT command for channel A, PAGE must be set to 00h. In order to access IOUT_OC_WARN_LIMIT register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh.

15	14	13	12	11	10	9	8
R	R	R	R	R	RW	RW	RW
IOOCW_EXP					IOOCW_MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
IOOCW_MAN							

LEGEND: R/W = Read/Write; R = Read only

IOUT_OC_WARN_LIMIT

Table 2-42. IOUT_OC_WARN_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	IOOCW_EXP	R	00000b	Linear two's complement exponent, 0. LSB = 1.0 A
10:0	IOOCW_MAN	RW	See below.	Linear two's complement mantissa.

At power-on, or after a RESTORE_DEFAULT_ALL operation, the IOUT_OC_WARN_LIMIT command will be loaded with the value of IOUTMAX. The IOUTMAX bits for each channel are stored in MFR_SPECIFIC_10 (PAGE 0 for channel A, PAGE 1 for channel B). IOUT_OC_WARN_LIMIT may be changed during operation, but will return to this value on reset.

Attempts to write any value other than 00000b to the exponent bits will be treated as invalid data - invalid data will be ignored, the appropriate flags in STATUS_CML and STATUS_WORD will be set, and the PMB_ALERT will be asserted to notify the system host of an invalid transaction.

2.4.32 (4Fh) OT_FAULT_LIMIT

The OT_FAULT_LIMIT command sets the value of the temperature limit, in degrees Celsius, that causes an overtemperature fault condition when the sensed temperature from the external sensor exceeds this limit. The default value is selected in MFR_SPECIFIC_13, using the OTF_DFLT bit.

OT_FAULT_LIMIT is a linear format command, as described in Section 2.1.1.

The OT_FAULT_LIMIT command must be accessed through Read Word/Write Word transactions as shown in Section 2.1.2.

OT_FAULT_LIMIT is a paged register. In order to access OT_FAULT_LIMIT command for channel A, PAGE must be set to 00h. In order to access OT_FAULT_LIMIT register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh.

15	14	13	12	11	10	9	8
R	R	R	R	R	RW	RW	RW
OTF_EXP					OTF_MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
OTF_MAN							

LEGEND: R/W = Read/Write; R = Read only

OT_FAULT_LIMIT

Table 2-43. OT_FAULT_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	OTF_EXP	R	00000b	Linear two's complement exponent, 0. LSB = 1 ºC
10:0	OTF_MAN	RW	NVM	Linear two's complement mantissa. The default OT_FAULT_LIMIT is set by the OTF_DFLT bit in MFR_SPECIFIC_13.

Attempts to write any value other than 00000b to the exponent bits will be treated as invalid data - invalid data will be ignored, the appropriate flags in STATUS_CML and STATUS_WORD will be set, and the PMB_ALERT will be asserted to notify the system host of an invalid transaction.

2.4.33 (50h) OT_FAULT_RESPONSE

The OT_FAULT_RESPONSE instructs the device on what action to take in response to an output over-temperature fault. Upon triggering the over-temperature fault, the controller is latched off, and the following actions are taken:

- Set the TEMPERATURE bit in the STATUS_BYTE
- Set the OT_FAULT bit in the STATUS_TEMPERATURE register
- The device notifies the host (asserts PMB_ALERT, if the corresponding mask bit in SMBALERT_MASK is not set).

The OT_FAULT_RESPONSE command must be accessed through Read Byte/Write Byte transactions as shown in Section 2.1.2.

The OT_FAULT_RESPONSE command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
OTF_RESP							

LEGEND: R/W = Read/Write; R = Read only

OT_FAULT_RESPONSE

Table 2-44. OT_FAULT_RESPONSE Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OTF_RESP	RW	NVM	80h: Latch-off and do not restart. To clear a shutdown event due to a fault event, the user must toggle the AVR_EN/BEN pin and/or the ON bit in OPERATION, per the settings in ON_OFF_CONFIG, or power cycle the bias power to the V3P3 pin of the controller device. C0h: Shutdown and restart when the fault condition is no longer present

Attempts to write any value other than those specified above will be treated as invalid data - invalid data will be ignored, the appropriate flags in STATUS_CML and STATUS_WORD will be set, and the PMB_ALERT will be asserted to notify the system host of an invalid transaction.

2.4.34 (51h) OT_WARN_LIMIT

The OT_WARN_LIMIT command sets the temperature, in degrees Celsius, of the unit at which it should indicate an Over-temperature Warning event. In response to the OT_WARN_LIMIT being exceeded, the device will:

- Set the TEMPERATURE bit in the STATUS_BYTE
- Set the Over-temperature Warning bit in the STATUS_TEMPERATURE register
- Notify the host (asserts PMB_ALERT, if the corresponding mask bit in SMBALERT_MASK is not set)

OT_WARN_LIMIT is a linear format command, as described in Section 2.1.1.

The OT_WARN_LIMIT command must be accessed through Read Word/Write Word transactions as shown in Section 2.1.2.

OT_WARN_LIMIT is a paged register. In order to access OT_WARN_LIMIT command for channel A, PAGE must be set to 00h. In order to access OT_WARN_LIMIT register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh.

15	14	13	12	11	10	9	8
R	R	R	R	R	RW	RW	RW
OTW_EXP					OTW_MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
OTW_MAN							

LEGEND: R/W = Read/Write; R = Read only

OT_WARN_LIMIT

Table 2-45. OT_WARN_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	OTF_EXP	R	00000b	Linear two's complement exponent, 0. LSB = 1 ºC
10:0	OTF_MAN	RW	105d	Linear two's complement mantissa. Default = 105 ºC

Attempts to write any value other than 00000b to the exponent bits will be treated as invalid data - invalid data will be ignored, the appropriate flags in STATUS_CML and STATUS_WORD will be set, and the PMB_ALERT will be asserted to notify the system host of an invalid transaction.

2.4.35 (55h) VIN_OV_FAULT_LIMIT

The VIN_OV_FAULT_LIMIT command sets the value of the input voltage that causes an input overvoltage fault.

VIN_OV_FAULT_LIMIT is a linear format command, as described in Section 2.1.1.

The VIN_OV_FAULT_LIMIT command must be accessed through Read Word/Write Word transactions as shown in Section 2.1.2.

The VIN_OV_FAULT_LIMIT command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

15	14	13	12	11	10	9	8
R	R	R	R	R	RW	RW	RW
VIN_OVF_EXP					VIN_OVF_MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VIN_OVF_MAN							

LEGEND: R/W = Read/Write; R = Read only

VIN_OV_FAULT_LIMIT

Table 2-46. VIN_OV_FAULT_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	VIN_OVF_EXP	R	00000b	Linear two's complement exponent, 0. LSB = 1 V
10:0	VIN_OVF_MAN	RW	NVM	Linear two's complement mantissa. Valid values of the mantissa range from 0d to 31d.

Attempts to write any value other than 00000b to the exponent bits, or a value greater than 31d to the mantissa bits will be treated as invalid data - invalid data will be ignored, the appropriate flags in STATUS_CML and STATUS_WORD will be set, and the PMB_ALERT will be asserted to notify the system host of an invalid transaction.

2.4.36 (56h) VIN_OV_FAULT_RESPONSE

The VIN_OV_FAULT_RESPONSE command instructs the device on what action to take in response to an input overvoltage fault. In response to the VIN_OV_LIMIT being exceeded, the device will:

- Set the OTHER bit in the STATUS_BYTE
- Set the INPUT bit in the upper byte of the STATUS_WORD
- Sets the VIN_OV_FAULT bit in the STATUS_INPUT register
- Notify the host (assert the PMB_ALERT signal, if the corresponding mask bit in Section 2.4.10 is not set)

The VIN_OV_FAULT_RESPONSE command must be accessed through Read Byte transactions as shown in Section 2.1.2.

The VIN_OV_FAULT_RESPONSE command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
VI_OVF_RESP							

LEGEND: R/W = Read/Write; R = Read only

VIN_OV_FAULT_RESPONSE

Table 2-47. VIN_OV_FAULT_RESPONSE Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VI_OVF_RESP	R	00h	00h: Ignore. The controller will set the appropriate status bits, and alert the host, but continue converting power.

2.4.37 (59h) VIN_UV_FAULT_LIMIT

The VIN_UV_FAULT_LIMIT command sets the value of the input voltage that causes an Input Under voltage Fault. This fault is masked until the input exceeds the value set by the VIN_ON command for the first time, and the unit has been enabled.

VIN_UV_FAULT_LIMIT is a linear format command, as described in Section 2.1.1.

The VIN_UV_FAULT_LIMIT command must be accessed through Read Word/Write Word transactions as shown in Section 2.1.2.

The VIN_UV_FAULT_LIMIT command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
VIN_UVF_EXP					VIN_UVF_MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VIN_UVF_MAN							

LEGEND: R/W = Read/Write; R = Read only

VIN_UV_FAULT_LIMIT

Table 2-48. VIN_UV_FAULT_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	VIN_UVF_EXP	RW	NVM	Linear two's complement exponent. See the table of acceptable values below.
10:0	VIN_UVF_MAN	RW	NVM	Linear two's complement mantissa. See the table of acceptable values below.

Table 2-49. Acceptable Values of VIN_UV_FAULT_LIMIT

VIN_UV_FAULT_LIMIT (hex)	VIN UVF Limit (V)
F011h	4.25
F80Bh	5.5
F80Dh	6.5
F80Fh	7.5
F811h	8.5
F813h	9.5
F815h	10.5
F817h	11.5

Attempts to write any value other than those specified above will be treated as invalid data - invalid data will be ignored, the appropriate flags in STATUS_CML and STATUS_WORD will be set, and the PMB_ALERT will be asserted to notify the system host of an invalid transaction.

2.4.38 (5Ah) VIN_UV_FAULT_RESPONSE

The VIN_UV_FAULT_RESPONSE command instructs the device on what action to take in response to an input overvoltage fault. In response to the VIN_UV_LIMIT being exceeded, the device will:

- Set the OTHER bit in the STATUS_BYTE
- Set the INPUT bit in the upper byte of the STATUS_WORD
- Set the VIN_UV_FAULT bit in the STATUS_INPUT register
- The device notifies the host (asserts PMB_ALERT, if the corresponding mask bit in SMBALERT_MASK is not set)

The VIN_UV_FAULT_RESPONSE command must be accessed through Read Byte transactions as shown in Section 2.1.2.

The VIN_UV_FAULT_RESPONSE command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
VI_UVF_RESP							

LEGEND: R/W = Read/Write; R = Read only

VIN_UV_FAULT_RESPONSE

Table 2-50. VIN_UV_FAULT_RESPONSE Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VI_UVF_RESP	R	C0h	C0h: Shutdown and restart when the fault condition is no longer present

Attempts to write to this command will be treated as invalid transactions - any data will be ignored, the appropriate flags in STATUS_CML and STATUS_WORD will be set, and the PMB_ALERT will be asserted to notify the system host of an invalid transaction.

2.4.39 (5Bh) IIN_OC_FAULT_LIMIT

The IIN_OC_FAULT_LIMIT command sets the value of the input current, in amperes, that causes the input over current fault condition.

IIN_OC_FAULT_LIMIT is a linear format command, as described in Section 2.1.1.

The IIN_OC_FAULT_LIMIT command must be accessed through Read Word/Write Word transactions as shown in Section 2.1.2.

The IIN_OC_FAULT_LIMIT command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

15	14	13	12	11	10	9	8
R	R	R	R	R	RW	RW	RW
IIN_OCF_EXP					IIN_OCF_MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
IIN_OCF_MAN							

LEGEND: R/W = Read/Write; R = Read only

IIN_OC_FAULT_LIMIT

Table 2-51. IIN_OC_FAULT_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	IIN_OCF_EXP	R	11111b	Linear two's complement format exponent, –1. LSB = 0.5 A.
10:0	IIN_OCF_MAN	RW	See below.	Linear two's complement format mantissa. Acceptable values range from 0d (0 A) to 127d (63.5 A).

During operation, the IIN_OC_FAULT_LIMIT may be changed to any valid value, as specified above. The IIN_OC_FAULT_LIMIT command has only limited NVM backup. The table below summarizes the values that IIN_OC_FAULT_LIMIT may be restored to following a reset, or RESTORE_DEFAULT_ALL operation.

Table 2-52. IIN_OC_FAULT_LIMIT reset values

Hex Value	IIN_OC_FAULT_LIMIT during NVM store operation	IIN_OC_FAULT_LIMIT following Reset/Restore Operation
F810h	8 A	8 A
F820h	16 A	16 A
F830h	24 A	24 A
F840h	32 A	32 A
F850h	40 A	40 A
F860h	48 A	48 A
F870h	56 A	56 A
F87Fh	63.5 A	63.5 A
Any other valid data	Any other valid data	63.5 A

Attempts to write any value other than 11111b to the exponent bits, or a value greater than 127d to the mantissa will be treated as invalid data - invalid data will be ignored, the appropriate flags in STATUS_CML and STATUS_WORD will be set, and the PMB_ALERT will be asserted to notify the system host of an invalid transaction.

2.4.40 (5Ch) IIN_OC_FAULT_RESPONSE

The IIN_OC_FAULT_RESPONSE command instructs the device on what action to take in response to an input over-current fault. Upon triggering the input over-current fault, the controller is latched off, and the following actions are taken:

- Set the OTHER bit in the STATUS_BYTE
- Set the INPUT bit in the STATUS_WORD
- Set the IIN_OC_FAULT bit in the STATUS_INPUT register
- The device notifies the host (asserts PMB_ALERT, if the corresponding mask bit in SMBALERT_MASK is not set)

The IIN_OC_FAULT_RESPONSE command must be accessed through Read Byte transactions as shown in Section 2.1.2.

The IIN_OC_FAULT_RESPONSE command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
IIN_OC_RESP							

LEGEND: R/W = Read/Write; R = Read only

IIN_OC_FAULT_RESPONSE

Table 2-53. IIN_OC_FAULT_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	IIN_OC_RESP	R	C0h	C0h: Latch-off and do not restart. To clear a shutdown event due to a fault event, the user must toggle the AVR_EN/BEN pin and/or the ON bit in OPERATION, per the settings in ON_OFF_CONFIG, or power cycle the bias power to the V3P3 pin of the controller device.

Attempts to write to this command will be treated as invalid transactions - any data will be ignored, the appropriate flags in STATUS_CML and STATUS_WORD will be set, and the PMB_ALERT will be asserted to notify the system host of an invalid transaction.

2.4.41 (5Dh) IIN_OC_WARN_LIMIT

The IIN_OC_WARN_LIMIT command sets the value of the input current, in amperes, that causes the input overcurrent warning condition. Upon triggering the over-current warning, the following actions are taken:

- Set the OTHER bit in the STATUS_BYTE
- Set the INPUT bit in the STATUS_WORD
- Set the IIN Over-current Warning bit in the STATUS_INPUT register
- The device notifies the host (asserts PMB_ALERT, if the corresponding mask bit in SMBALERT_MASK is not set)

The IIN_OC_WARN_LIMIT command must be accessed through Read Word/Write Word transactions as shown in Section 2.1.2.

IIN_OC_WARN_LIMIT is a linear format command, as described in Section 2.1.1.

The IIN_OC_WARN_LIMIT command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
IIN_OCW_EXP					IIN_OCW_MAN		
7	6	5	4	3	2	1	0
R	RW	RW	RW	RW	RW	RW	RW
IIN_OCW_MAN							

LEGEND: R/W = Read/Write; R = Read only

IIN_OC_WARN_LIMIT

Table 2-54. IIN_OC_FAULT_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	IIN_OCW_EXP	R	11111b	Linear two's complement format exponent, –1. LSB = 0.5 A.
10:0	IIN_OCW_MAN	RW	See below.	Linear two's complement format mantissa. Acceptable values range from 0d (0 A) to 127d (63.5 A).

During operation, the IIN_OC_FAULT_LIMIT may be changed to any valid value, as specified above. The IIN_OC_FAULT_LIMIT command has only limited NVM backup. The table below summarizes the values that IIN_OC_FAULT_LIMIT may be restored to following a reset, or RESTORE_DEFAULT_ALL operation.

Table 2-55. IIN_OC_WARN_LIMIT reset values

Hex Value	IIN_OC_WARN_LIMIT during NVM store operation	IIN_OC_WARN_LIMIT following Reset/Restore Operation
F810h	8 A	8 A
F820h	16 A	16 A
F830h	24 A	24 A
F840h	32 A	32 A
F850h	40 A	40 A
F860h	48 A	48 A
F870h	56 A	56 A
F87Fh	63.5 A	63.5 A
Any other valid data	Any other valid data	63.5 A

Attempts to write any value other than 11111b to the exponent bits, or a value greater than 127d to the mantissa will be treated as invalid data - invalid data will be ignored, the appropriate flags in STATUS_CML and STATUS_WORD will be set, and the PMB_ALERT will be asserted to notify the system host of an invalid transaction.

2.4.42 (60h) TON_DELAY

The TON_DELAY sets the time, in milliseconds, from when a start condition is received (as programmed by the ON_OFF_CONFIG command) until the output voltage starts to rise.

The TON_DELAY command must be accessed through Read Word/Write Word transactions as shown in Section 2.1.2.

TON_DELAY is a linear format command, as described in Section 2.1.1.

TON_DELAY is a paged register. In order to access TON_DELAY command for channel A, PAGE must be set to 00h. In order to access TON_DELAY register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh.

15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
TON_DLY_EXP					TON_DLY_MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
TON_DLY_EXP							

LEGEND: R/W = Read/Write; R = Read only

TON_DELAY

Table 2-56. IIN_OC_FAULT_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	TON_DLY_EXP	RW	NVM	Linear two's complement format exponent. See the table of acceptable values below.
10:0	TON_DLY_MAN	RW	NVM	Linear two's complement format mantissa. See the table of acceptable values below.

Table 2-57. Acceptable Values of TON_DELAY

TON_DELAY (hex)	Turn on delay (ms)
B1ECh	0.48
B396h	0.896
BAD1h	1.408
C26Eh	2.432

Attempts to write any value other than those specified above will be treated as invalid data - invalid data will be ignored, the appropriate flags in STATUS_CML and STATUS_WORD will be set, and the PMB_ALERT will be asserted to notify the system host of an invalid transaction.

2.4.43 (6Bh) PIN_OP_WARN_LIMIT

The PIN_OP_WARN_LIMIT command sets the value of the input power, in watts, that causes a warning that the input power is high. In response to the PIN_OP_WARN_LIMIT being exceeded, the following action is taken:

- Set the INPUT bit is the upper byte of the STATUS_WORD
- Set the PIN_OP_WARNING bit in STATUS_INPUT

NOTE: Valid writes to the value PIN_OP_WARN_LIMIT command will update the lower byte of the MFR_SPECIFIC_32 command. Likewise, valid writes to MFR_SPECIFIC_32 will also update the value of PIN_OP_WARN_LIMIT.

The PIN_OP_WARN_LIMIT command must be accessed through Read Word/Write Word transactions as shown in Section 2.1.2.

PIN_OP_WARN_LIMIT is a linear format command, as described in Section 2.1.1.

The PIN_OP_WARN_LIMIT command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
PIN_OPW_EXP					PIN_OPW_MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
PIN_OPW_MAN							

LEGEND: R/W = Read/Write; R = Read only

PIN_OP_WARN_LIMIT

Table 2-58. PIN_OP_WARN_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	PIN_OPW_EXP	RW	00001b	Linear two's complement format exponent, 1. LSB = 2 W
10:0	PIN_OPW_MAN	RW	225d	Linear two's complement format mantissa. Valid values range from 0d (0 W) to 255d (510 W).

During operation, the PIN_OP_WARN_LIMIT may be changed to any valid value, as specified above. This command does not have NVM backup, and will be restored to 450 W (08E1h) upon reset or RESTORE_DEFAULT_ALL operations.

Attempts to write any value other than 00001b to the exponent bits, or a value greater than 225d to the mantissa will be treated as invalid data - invalid data will be ignored, the appropriate flags in STATUS_CML and STATUS_WORD will be set, and the PMB_ALERT will be asserted to notify the system host of an invalid transaction.

2.4.44 (78h) STATUS_BYTE

The STATUS_BYTE command returns one byte of information with a summary of the most critical faults, such as over-voltage, overcurrent, over-temperature, etc. The status flags in this register may be cleared using the Section 2.4.4 command.

The STATUS_BYTE command must be accessed through Read Byte transactions as shown in Section 2.1.2.

STATUS_BYTE is a paged register. In order to access STATUS_WORD command for channel A, PAGE must be set to 00h. In order to access STATUS_WORD register for channel B, PAGE must be set to 01h. If PAGE is set FFh, the device return value will reflect the status of Channel A.

7	6	5	4	3	2	1	0
0	R	R	R	R	R	R	R
BUSY	OFF	VOUT_OV	IOUT_OC	VIN_UV	TEMP	CML	OTHER

Figure 2-20. STATUS_BYTE

Table 2-59. STATUS_BYTE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BUSY	R	0	Not supported and always set to 0.
6	OFF	R	Current Status	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled. 0: Raw status indicating the IC is providing power to VOUT. 1: Raw status indicating the IC is not providing power to VOUT.
5	VOUT_OV	R	Current Status	Output Over-Voltage Fault Condition 0: Latched flag indicating no VOUT OV fault has occurred. 1: Latched flag indicating a VOUT OV fault occurred
4	IOUT_OC	R	Current Status	Output Over-Current Fault Condition 0: Latched flag indicating no IOUT OC fault has occurred. 1: Latched flag indicating an IOUT OC fault has occurred.
3	VIN_UV	R	Current Status	Input Under-Voltage Fault Condition 0: Latched flag indicating VIN is above the UVLO threshold. 1: Latched flag indicating VIN is below the UVLO threshold.
2	TEMP	R	Current Status	Over-Temperature Fault/Warning 0: Latched flag indicating no OT fault or warning has occurred. 1: Latched flag indicating an OT fault or warning has occurred.
1	CML	R	Current Status	Communications, Memory or Logic Fault 0: Latched flag indicating no communication, memory, or logic fault has occurred. 1: Latched flag indicating a communication, memory, or logic fault has occurred.
0	OTHER	R	Current Status	Other Fault (None of the Above) This bit is used to flag faults not covered with the other bit faults. In this case, UVF or OCW faults are examples of other faults not covered by the bits [7:1] in this register. 0: No fault has occurred 1: A fault or warning not listed in bits [7:1] has occurred.

Per the description in the PMBus 1.3 specification, part II, TPS53681 does support clearing of status bits by writing to STATUS registers. However, the bits in the STATUS_BYTE are summary bits only and reflect the status of corresponding bits in STATUS_VOUT, STATUS_IOUT, etc... To clear these bits individually, the user must clear them by writing to the corresponding STATUS register. For example: the output overcurrent fault sets the IOUT_OC bit in STATUS_BYTE, and the IOUT_OC_FLT bit in STATUS_IOUT. Writing a 1 to the IOUT_OC_FLT bit in STATUS_IOUT clears the fault in both STATUS_BYTE and STATUS_IOUT. Hence, writes to STATUS_BYTE will be treated as invalid transactions.

2.4.45 (79h) STATUS_WORD

The STATUS_WORD command returns two bytes of information with a summary of critical faults, such as over-voltage, overcurrent, over-temperature, etc..

The STATUS_WORD command must be accessed through Read Word transactions as shown in Section 2.1.2.

STATUS_WORD is a paged register. In order to access STATUS_WORD command for channel A, PAGE must be set to 00h. In order to access STATUS_WORD register for channel B, PAGE must be set to 01h. If PAGE is set FFh, the device return value will reflect the status of Channel A.

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
VOUT	IOUT	INPUT	MFR	PGOOD	FANS	OTHER	UNKNOWN
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
BUSY	OFF	VOUT_OV	IOUT_OC	VIN_UV	TEMP	CML	OTHER

Figure 2-21. STATUS_WORD

Table 2-60. STATUS_WORD Register Field Descriptions

Bit	Field	Type	Reset	Description
15	VOUT	R	Current Status	Output Voltage Fault/Warning 0: Latched flag indicating no VOUT fault or warning has occurred. 1: Latched flag indicating a VOUT fault or warning has occurred.
14	IOUT	R	Current Status	Output Current Fault/Warning 0: Latched flag indicating no IOUT fault or warning has occurred. 1: Latched flag indicating an IOUT fault or warning has occurred.
13	INPUT	R	Current Status	Input Voltage/Current Fault/Warning 0: Latched flag indicating no VIN or IIN fault or warning has occurred. 1: Latched flag indicating a VIN or IIN fault or warning has occurred.
12	MFR	R	Current Status	MFR_SPECIFIC Fault 0: Latched flag indicating no MFR_SPECIFIC fault has occurred. 1: Latched flag indicating a MFR_SPECIFIC fault has occurred.
11	PGOOD	R	Current Status	Power Good Status 0: Raw status indicating VRRDY pin is at logic high. 1: Raw status indicating VRRDY pin is at logic low.
10	FANS	R	0	Not supported and always set to 0.
9	OTHER	R	0	Not supported and always set to 0.
8	UNKNOWN	R	0	Not supported and always set to 0.
7	BUSY	R	0	Not supported and always set to 0.
6	OFF	R	Current Status	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled. 0: Raw status indicating the IC is providing power to VOUT. 1: Raw status indicating the IC is not providing power to VOUT.
5	VOUT_OV	R	Current Status	Output Over-Voltage Fault Condition 0: Latched flag indicating no VOUT OV fault has occurred. 1: Latched flag indicating a VOUT OV fault occurred
4	IOUT_OC	R	Current Status	Output Over-Current Fault Condition 0: Latched flag indicating no IOUT OC fault has occurred. 1: Latched flag indicating an IOUT OC fault has occurred.
3	VIN_UV	R	Current Status	Input Under-Voltage Fault Condition 0: Latched flag indicating VIN is above the UVLO threshold. 1: Latched flag indicating VIN is below the UVLO threshold.
2	TEMP	R	Current Status	Over-Temperature Fault/Warning 0: Latched flag indicating no OT fault or warning has occurred. 1: Latched flag indicating an OT fault or warning has occurred.

Table 2-60. STATUS_WORD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CML	R	Current Status	Communications, Memory or Logic Fault 0: Latched flag indicating no communication, memory, or logic fault has occurred. 1: Latched flag indicating a communication, memory, or logic fault has occurred.
0	OTHER	R	Current Status	Other Fault (None of the Above) This bit is used to flag faults not covered with the other bit faults. In this case, UVF or OCW faults are examples of other faults not covered by the bits [7:1] in this register. 0: No fault has occurred 1: A fault or warning not listed in bits [7:1] has occurred.

Per the description in the PMBus 1.3 specification, part II, TPS53681 does support clearing of status bits by writing to STATUS registers. However, the bits in the STATUS_WORD are summary bits only and reflect the status of corresponding bits in STATUS_VOUT, STATUS_IOUT, etc... To clear these bits individually, the user must clear them by writing to the corresponding STATUS register. For example: the output overcurrent fault sets the IOUT_OC bit in STATUS_WORD, and the IOUT_OC_FLT bit in STATUS_IOUT. Writing a 1 to the IOUT_OC_FLT bit in STATUS_IOUT clears the fault in both STATUS_WORD and STATUS_IOUT. Hence, writes to STATUS_BYTE will be treated as invalid transactions.

2.4.46 (7Ah) STATUS_VOUT

The STATUS_VOUT command returns one byte of information relating to the status of the converter's output voltage related faults.

The STATUS_VOUT command must be accessed through Read Byte/Write Byte transactions as shown in Section 2.1.2.

STATUS_VOUT is a paged register. In order to access STATUS_VOUT command for channel A, PAGE must be set to 00h. In order to access STATUS_VOUT register for channel B, PAGE must be set to 01h. If PAGE is set FFh, the device return value will reflect the status of Channel A.

7	6	5	4	3	2	1	0
RW	0	0	RW	RW	0	0	0
VOUT_OVF	VOUT_OVW	VOUT_UVW	VOUT_UVF	VOUT_MIN_MAX	TON_MAX	TOFF_MAX	VOUT_TRACK

Figure 2-22. STATUS_VOUT

Table 2-61. STATUS_VOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VOUT_OVF	RW	Current Status	Output Over-Voltage Fault 0: Latched flag indicating no VOUT OV fault has occurred. 1: Latched flag indicating a VOUT OV fault has occurred.
6	VOUT_OVW	R	0	Not supported and always set to 0.
5	VOUT_UVW	R	0	Not supported and always set to 0.
4	VOUT_UVF	RW	Current Status	Output Under-Voltage Fault 0: Latched flag indicating no VOUT UV fault has occurred. 1: Latched flag indicating a VOUT UV fault has occurred.
3	VOUT_MIN_MAX	RW	Current Status	Output Voltage Max/Min Exceeded Warning 0: Latched flag indicating no VOUT_MAX/VOUT_MIN warning has occurred. 1: Latched flag indicating that an attempt has been made to set the output voltage to a value higher than allowed by the VOUT_MAX/VOUT_MIN command.
2	TON_MAX	R	0	Not supported and always set to 0.
1	TOFF_MAX	R	0	Not supported and always set to 0.
0	VOUT_TRACK	R	0	Not supported and always set to 0.

Per the description in the PMBus 1.3 specification, part II, TPS53681 does support clearing of status bits by writing to STATUS registers. Writing a 1 to any bit in this register will attempt to clear it as a fault condition.

2.4.47 (7Bh) STATUS_IOUT

The STATUS_IOUT command returns one byte of information relating to the status of the converter's output current related faults.

The STATUS_IOUT command must be accessed through Read Byte/Write Byte transactions as shown in Section 2.1.2.

STATUS_IOUT is a paged register. In order to access STATUS_IOUT command for channel A, PAGE must be set to 00h. In order to access STATUS_IOUT register for channel B, PAGE must be set to 01h. If PAGE is set FFh, the device return value will reflect the status of Channel A.

7	6	5	4	3	2	1	0
RW	0	RW	0	RW	0	0	0
IOUT_OCF	IOUT_OCUVF	IOUT_OCW	IOUT_UCF	CUR_SHAREF	POW_LIMIT	POUT_OPF	POUT_OPW

Figure 2-23. STATUS_IOUT

Table 2-62. STATUS_IOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	IOUT_OCF	RW	Current Status	Output Over-Current Fault 0: Latched flag indicating no IOUT OC fault has occurred. 1: Latched flag indicating a IOUT OC fault has occurred .
6	IOUT_OCUVF	R	0	Not supported and always set to 0.
5	IOUT_OCW	RW	Current Status	0: Latched flag indicating no IOUT OC warning has occurred 1: Latched flag indicating a IOUT OC warning has occurred
4	IOUT_UCF	R	0	Not supported and always set to 0.
3	CUR_SHAREF	RW	Current Status	0: Latched flag indicating no current sharing fault has occurred 1: Latched flag indicating a current sharing fault has occurred
2	POW_LIMIT	R	0	Not supported and always set to 0.
1	POUT_OPF	R	0	Not supported and always set to 0.
0	POUT_OPW	R	0	Not supported and always set to 0.

Per the description in the PMBus 1.3 specification, part II, TPS53681 does support clearing of status bits by writing to STATUS registers. Writing a 1 to any bit in this register will attempt to clear it as a fault condition.

2.4.48 (7Ch) STATUS_INPUT

The STATUS_INPUT command returns one byte of information relating to the status of the converter's input voltage and current related faults.

The STATUS_INPUT command must be accessed through Read Byte/Write Byte transactions as shown in Section 2.1.2.

The STATUS_INPUT command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

7	6	5	4	3	2	1	0
RW	0	0	RW	RW	RW	RW	RW
VIN_OVF	VIN_OVW	VIN_UVW	VIN_UVF	LOW_VIN	IIN_OCF	IIN_OCW	PIN_OPW

Figure 2-24. STATUS_INPUT Register

Table 2-63. STATUS_INPUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VIN_OVF	RW	Current Status	Input Over-Voltage Fault 0: Latched flag indicating no VIN OV fault has occurred. 1: Latched flag indicating a VIN OV fault has occurred.
6	VIN_OVW	R	0	Not supported and always set to 0.
5	VIN_UVW	R	0	Not supported and always set to 0.
4	VIN_UVF	RW	Current Status	Input Under-Voltage Fault 0: Latched flag indicating no VIN UV fault has occurred. 1: Latched flag indicating a VIN UV fault has occurred.
3	LOW_VIN	RW	Current Status	Unit Off for insufficient input voltage 0: Latched flag indicating no LOW_VIN fault has occurred. 1: Latched flag indicating a LOW_VIN fault has occurred
2	IIN_OCF	RW	Current Status	Input Over-Current Fault 0: Latched flag indicating no IIN OC fault has occurred. 1: Latched flag indicating a IIN OC fault has occurred.
1	IIN_OCW	RW	Current Status	Input Over-Current Warning 0: Latched flag indicating no IIN OC warning has occurred. 1: Latched flag indicating a IIN OC warning has occurred.
0	PIN_OPW	RW	Current Status	Input Over-Power Warning 0: Latched flag indicating no input over-power warning has occurred. 1: Latched flag indicating a input over-power warning has occurred.

Per the description in the PMBus 1.3 specification, part II, TPS53681 does support clearing of status bits by writing to STATUS registers. Writing a 1 to any bit in this register will attempt to clear it as a fault condition.

2.4.49 (7Dh) STATUS_TEMPERATURE

The STATUS_TEMPERATURE command returns one byte of information relating to the status of the converter's temperature related faults.

The STATUS_TEMPERATURE command must be accessed through Read Byte/Write Byte transactions as shown in Section 2.1.2.

STATUS_TEMPERATURE is a paged register. In order to access STATUS_TEMPERATURE command for channel A, PAGE must be set to 00h. In order to access STATUS_TEMPERATURE register for channel B, PAGE must be set to 01h. If PAGE is set FFh, the device return value will reflect the status of Channel A.

7	6	5	4	3	2	1	0
RW	RW	0	0	R	R	R	R
OTF	OTW	UTW	UTF	Reserved			

Figure 2-25. STATUS_TEMPERATURE Register

Table 2-64. STATUS_TEMPERATURE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OTF	RW	Current Status	Over-Temperature Fault 0: (Default) A temperature fault has not occurred. 1: A temperature fault has occurred.
6	OTW	RW	Current Status	Over-Temperature Warning 0: (Default) A temperature warning has not occurred. 1: A temperature warning has occurred.
5	UTW	R	0	Not supported and always set to 0.
4	UTF	R	0	Not supported and always set to 0.
3-0	Reserved	R	0000	Always set to 0.

Per the description in the PMBus 1.3 specification, part II, TPS53681 does support clearing of status bits by writing to STATUS registers. Writing a 1 to any bit in this register will attempt to clear it as a fault condition.

2.4.50 (7Eh) STATUS_CML

The STATUS_CML command returns one byte with contents regarding communication, logic, or memory conditions.

The STATUS_CML command must be accessed through Read Byte/Write Byte transactions as shown in Section 2.1.2.

The STATUS_CML command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

7	6	5	4	3	2	1	0
RW	RW	RW	RW	0	0	RW	0
IV_CMD	IV_DATA	PEC_FAIL	MEM	PRO_FAULT	Reserved	COM_FAIL	CML_OTHER

Figure 2-26. STATUS_CML Register

Table 2-65. STATUS_CML Register Field Descriptions

Bit	Field	Type	Reset	Description
7	IV_CMD	RW	Current Status	Invalid or Unsupported Command Received 0: Latched flag indicating no invalid or unsupported command has been received. 1: Latched flag indicating an invalid or unsupported command has been received.
6	IV_DATA	RW	Current Status	Invalid or Unsupported Data Received 0: Latched flag indicating no invalid or unsupported data has been received. 1: Latched flag indicating an invalid or unsupported data has been received.
5	PEC_FAIL	RW	Current Status	Packet Error Check Failed 0: Latched flag indicating no packet error check has failed 1: Latched flag indicating a packet error check has failed
4	Reserved	R	0	Always set to 0.
3	MEM	RW	Current Status	Memory/NVM Error 0: Latched flag indicating no memory error has occurred 1: Latched flag indicating a memory error has occurred
2	Reserved	R	0	Always set to 0.
1	COM_FAIL	RW	Current Status	Other Communication Faults 0: Latched flag indicating no communication fault other than the ones listed in this table has occurred. 1: Latched flag indicating a communication fault other than the ones listed in this table has occurred.
0	CML_OTHER	R	0	Not supported and always set to 0.

Per the description in the PMBus 1.3 specification, part II, TPS53681 does support clearing of status bits by writing to STATUS registers. Writing a 1 to any bit in this register will attempt to clear it as a fault condition.

2.4.51 (80h) STATUS_MFR_SPECIFIC

The STATUS_MFR_SPECIFIC command returns one byte containing manufacturer-specific faults or warnings.

The STATUS_MFR_SPECIFIC command must be accessed through Read Byte/Write Byte transactions as shown in Section 2.1.2.

STATUS_MFR_SPECIFIC is a paged register. In order to access STATUS_MFR_SPECIFIC command for channel A, PAGE must be set to 00h. In order to access STATUS_MFR_SPECIFIC register for channel B, PAGE must be set to 01h. If PAGE is set FFh, the device return value will reflect the status of Channel A.

Figure 2-27. STATUS_MFR_SPECIFIC Register

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW			RW
FLT_PS	VSNS_OPEN	MAX_PH_WARN	TSNS_LOW	RST_VID (Page 0)	Reserved		PHFLT

Table 2-66. STATUS_MFR_SPECIFIC Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MFR_FAULT_PS	RW	Current Status	Power Stage Fault 0b: Latched flag indicating no fault from TI power stage has occurred. 1b: Latched flag indicating a fault from TI power stage has occurred.
6	VSNS_OPEN	RW	Current Status	VSNS pin open 0b: Latched flag indicating VSNS pin was not open at power-up. 1b: Latched flag indicating VSNS pin was open at power-up.
5	MAX_PH_WARN	RW	Current Status	Maximum Phase Warning If the selected operational phase number is larger than the maximum available phase number specified by the hardware, then MAX_PH_WARN is set, and the operational phase number is changed to the maximum available phase number. 0b: Latched flag indicating no maximum phase warning has occurred. 1b: Latched flag indicating a maximum phase warning has occurred.
4	TSNS_LOW	RW	Current Status	0b: Latched flag indicating that TSEN < 150mV before soft-start. 1b: Latched flag indicating that TSEN ≥ 150mV before soft-start.
3	RST_VID (Page 0)	RW	Current Status	RST_VID (Page 0) 0b: A VID reset operation has NOT occurred 1b: A VID reset operation has occurred
2:1	Reserved	R	00b	Always set to 0.
0	PHFLT	RW	Current Status	Phase current share fault. The PHFLT bit will be set if any phase has current imbalance warnings occurring repetitively for 7 detection cycles (~500 µs continuously). Phases with current imbalance warnings may be read back via MFR_SPECIFIC_03. 0b: No repetitive current share fault has occurred 1b: Repetitive current share fault has occurred

Per the description in the PMBus 1.3 specification, part II, TPS53681 does support clearing of status bits by writing to STATUS registers. Writing a 1 to any bit in this register will attempt to clear it as a fault condition.

2.4.52 (88h) READ_VIN

The READ_VIN command returns the input voltage in volts. The two data bytes are formatted in the Linear Data format. The refresh rate is 1200 µs.

READ_VIN is a linear format command, as described in Section 2.1.1.

The READ_VIN command must be accessed through Read Word transactions as shown in Section 2.1.2.

The READ_VIN command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
READ_VIN_EXP					READ_VIN_MAN		
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
READ_VIN_MAN							

LEGEND: R/W = Read/Write; R = Read only

READ_VIN

Table 2-67. READ_VIN Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	READ_VIN_EXP	R	Current Status	Linear two's complement format exponent.
10:0	READ_VIN_MAN	R	Current Status	Linear two's complement format mantissa.

Attempts to write to this command will be treated as invalid transactions - invalid data will be ignored, the appropriate flags in STATUS_CML and STATUS_WORD will be set, and the PMB_ALERT will be asserted to notify the system host of an invalid transaction.

2.4.53 (89h) READ_IIN

The READ_IIN command returns the input current in amperes. The refresh rate is 100 us.

READ_IIN is a linear format command, as described in Section 2.1.1.

The READ_IIN command must be accessed through Read Word transactions as shown in Section 2.1.2.

The READ_IIN command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
READ_IIN_EXP					READ_IIN_MAN		
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
READ_IIN_MAN							

LEGEND: R/W = Read/Write; R = Read only

READ_IIN

Table 2-68. READ_IIN Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	READ_IIN_EXP	R	Current Status	Linear two's complement format exponent.
10:0	READ_IIN_MAN	R	Current Status	Linear two's complement format mantissa.

Attempts to write to this command will be treated as invalid transactions - invalid data will be ignored, the appropriate flags in STATUS_CML and STATUS_WORD will be set, and the PMB_ALERT will be asserted to notify the system host of an invalid transaction.

2.4.54 (8Bh) READ_VOUT

The READ_VOUT command returns the actual, measured output voltage. The two data bytes are formatted in the VID Data format, and the refresh rate is 1200 us. The output voltage may also be read back in linear format using the MFR_SPECIFIC_04 command.

The READ_VOUT command must be accessed through Read Word transactions as shown in Section 2.1.2.

READ_VOUT is a VID format command, as described in Section 2.1.1.

READ_VOUT is a paged register. In order to access READ_VOUT command for channel A, PAGE must be set to 00h. In order to access READ_VOUT register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh.

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
READ_VOUT_VID							

LEGEND: R/W = Read/Write; R = Read only

READ_VOUT

Table 2-69. READ_VOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	READ_VOUT_VID	R	Current Status	Output voltage, VID format

Attempts to write to this command will be treated as invalid transactions - invalid data will be ignored, the appropriate flags in STATUS_CML and STATUS_WORD will be set, and the PMB_ALERT will be asserted to notify the system host of an invalid transaction.

2.4.55 (8Ch) READ_IOUT

The READ_IOUT command returns the output current in amperes.

READ_IOUT is a linear format command, as described in Section 2.1.1.

READ_IOUT is a paged register. In order to access READ_IOUT for channel A, PAGE must be set to 00h. In order to access the READ_IOUT register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh. READ_IOUT is also a phased register. Depending on the configuration of the design, for channel A, PHASE must be set to 00h to access Phase 1, 01h to access Phase 2, etc... PHASE must be set to FFh to access all phases simultaneously. PHASE may also be set to 80h to readack the total phase current (sum of all active phase currents for the active channel) measurement, as described in . Note that READ_IOUT is only a phased command for Channel A (PAGE 0).

The READ_IOUT command must be accessed through Read Word transactions as shown in Section 2.1.2.

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
READ_IOUT_EXP					READ_IOUT_MAN		
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
READ_IOUT_MAN							

LEGEND: R/W = Read/Write; R = Read only

READ_IOUT

Table 2-70. READ_IOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	READ_IOUT_EXP	R	Current Status	Linear two's complement format exponent.
10:0	READ_IOUT_MAN	R	Current Status	Linear two's complement format mantissa.

Attempts to write to this command will be treated as invalid transactions - invalid data will be ignored, the appropriate flags in STATUS_CML and STATUS_WORD will be set, and the PMB_ALERT will be asserted to notify the system host of an invalid transaction.

2.4.56 (8Dh) READ_TEMPERATURE_1

The READ_TEMPERATURE_1 command returns the temperature in degree Celsius. The two data bytes are formatted in the Linear Data format. The refresh rate is 1200 us.

READ_TEMPERATURE_1 is a linear format command, as described in Section 2.1.1.

READ_TEMPERATURE_1 is a paged register. In order to access READ_TEMPERATURE_1 command for channel A, PAGE must be set to 00h. In order to access READ_TEMPERATURE_1 register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh.

The READ_TEMPERATURE_1 command must be accessed through Read Word transactions as shown in Section 2.1.2.

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
READ_TEMP_EXP					READ_TEMP_MAN		
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
READ_TEMP_MAN							

LEGEND: R/W = Read/Write; R = Read only

READ_TEMPERATURE_1

Table 2-71. READ_TEMPERATURE_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	READ_TEMP_EXP	R	Current Status	Linear two's complement format exponent.
10:0	READ_TEMP_MAN	R	Current Status	Linear two's complement format mantissa.

Attempts to write to this command will be treated as invalid transactions - invalid data will be ignored, the appropriate flags in STATUS_CML and STATUS_WORD will be set, and the PMB_ALERT will be asserted to notify the system host of an invalid transaction.

2.4.57 (96h) READ_POUT

The READ_POUT command returns the calculated output power, in watts for the active channel. The refresh rate is 1200 µs.

READ_POUT is a linear format command, as described in Section 2.1.1.

READ_POUT is a paged register. In order to access READ_POUT command for channel A, PAGE must be set to 00h. In order to access READ_POUT register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh.

The READ_POUT command must be accessed through Read Word transactions as shown in Section 2.1.2.

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
READ_POUT_EXP					READ_POUT_MAN		
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
READ_POUT_MAN							

LEGEND: R/W = Read/Write; R = Read only

READ_POUT

Table 2-72. READ_POUT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	READ_POUT_EXP	R	Current Status	Linear two's complement format exponent.
10:0	READ_POUT_MAN	R	Current Status	Linear two's complement format mantissa.

Attempts to write to this command will be treated as invalid transactions - invalid data will be ignored, the appropriate flags in STATUS_CML and STATUS_WORD will be set, and the PMB_ALERT will be asserted to notify the system host of an invalid transaction.

2.4.58 (97h) READ_PIN

The READ_PIN command returns the calculated input power. The refresh rate is 1200 µs.

READ_PIN is a linear format command, as described in Section 2.1.1.

The READ_PIN command must be accessed through Read Word transactions as shown in Section 2.1.2.

The READ_PIN command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
READ_PIN_EXP					READ_PIN_MAN		
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
READ_PIN_MAN							

LEGEND: R/W = Read/Write; R = Read only

READ_PIN

Table 2-73. READ_PIN Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	READ_PIN_EXP	R	Current Status	Linear two's complement format exponent.
10:0	READ_PIN_MAN	R	Current Status	Linear two's complement format mantissa.

2.4.59 (98h) PMBUS_REVISION

The PMBUS_REVISION command reads the revision of the PMBus to which the device is compliant.

The READ_PIN command must be accessed through Read Byte transactions as shown in Section 2.1.2.

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
PMB_REV_P1				PMB_REV_P2			

LEGEND: R/W = Read/Write; R = Read only

PMBUS_REVISION

Table 2-74. PMBUS_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	PMB_REV_P1	R	0011b	PMBus specification, Part I (General Requirements, Transport And Electrical Interface) compliance. 0011b: PMBus rev 1.3, Part I compliant
3:0	PMB_REV_P2	R	0011b	PMBus specification, Part II (Command Language) compliance. 0011b: PMBus rev 1.3, Part II compliant

2.4.60 (99h) MFR_ID

The MFR_ID command is used to either set or read the manufacturer's ID (name, abbreviation or symbol that identifies the unit's manufacturer).

The MFR_ID command must be accessed through Block Write/Block Read transactions as shown in Section 2.1.2.

The MFR_ID command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
MFR_ID							
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
MFR_ID							

LEGEND: R/W = Read/Write; R = Read only

MFR_ID

Table 2-75. MFR_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	MFR_ID	RW	NVM	Arbitrary 16 bits with NVM backup for Manufacturer identification

2.4.61 (9Ah) MFR_MODEL

The MFR_MODEL command is used to either set or read the manufacturer's model number.

The MFR_MODEL command must be accessed through Block Write/Block Read transactions as shown in Section 2.1.2.

The MFR_MODEL command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
MFR_MODEL							
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
MFR_MODEL							

LEGEND: R/W = Read/Write; R = Read only

MFR_MODEL

Table 2-76. MFR_MODEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	MFR_MODEL	RW	NVM	Arbitrary 16 bits with NVM backup for Model number identification

2.4.62 (9Bh) MFR_REVISION

The MFR_REVISION command is used to either set or read the manufacturer's revision number

The MFR_REVISION command must be accessed through Block Write/Block Read transactions as shown in Section 2.1.2.

The MFR_REVISION command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
MFR_REV							
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
MFR_REV							

LEGEND: R/W = Read/Write; R = Read only

MFR_REVISION

Table 2-77. MFR_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	MFR_REV	RW	NVM	Arbitrary 16 bits with NVM backup for revision number identification

2.4.63 (9Dh) MFR_DATE

The MFR_DATE command is used to either set or read the manufacturing date.

The MFR_DATE command must be accessed through Block Write/Block Read transactions as shown in Section 2.1.2.

The MFR_DATE command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
MFR_DATE							
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
MFR_DATE							

LEGEND: R/W = Read/Write; R = Read only

MFR_DATE

Table 2-78. MFR_DATE Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	MFR_DATE	RW	NVM	Arbitrary 16 bits with NVM backup for manufacture date identification

2.4.64 (9Eh) MFR_SERIAL

The MFR_SERIAL command is used to get the CRC of latest programmed NVM data. This may be used to verify that an NVM programming operation was successful. See for more information.

The MFR_SERIAL command must be accessed through Write/Block Read transactions as shown in Section 2.1.2.

The MFR_SERIAL command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

31	30	29	28	27	26	25	24
R	R	R	R	R	R	R	R
MFR_SERIAL							
23	22	21	20	19	18	17	16
R	R	R	R	R	R	R	R
MFR_SERIAL							
15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
MFR_SERIAL							
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
MFR_SERIAL							

LEGEND: R/W = Read/Write; R = Read only

MFR_SERIAL

Table 2-79. MFR_SERIAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MFR_SERIAL	R	NVM	32-bit CRC of the latest programmed NVM data.

2.4.65 (ADh) IC_DEVICE_ID

The IC_DEVICE_ID command is used to read the type or part number of an IC that is used for the PMBus interface. Each manufacturer uses the format of their choice for the IC device identification.

The IC_DEVICE_ID command must be accessed through Block Read transactions as shown in Section 2.1.2.

The IC_DEVICE_ID command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
IC_DEVICE_ID							
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
IC_DEVICE_ID							

LEGEND: R/W = Read/Write; R = Read only

IC_DEVICE_ID

Table 2-80. IC_DEVICE_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	IC_DEVICE_ID	R	81h	81h: TPS53681

Attempts to write to this command will be treated as invalid transactions - invalid data will be ignored, the appropriate flags in STATUS_CML and STATUS_WORD will be set, and the PMB_ALERT will be asserted to notify the system host of an invalid transaction.

2.4.66 (AEh) IC_DEVICE_REV

The IC_DEVICE_REV command is used to read the revision number of an IC.

The IC_DEVICE_REV command must be accessed through Block Read transactions as shown in Section 2.1.2.

The IC_DEVICE_REV command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
IC_DEVICE_REV							
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
IC_DEVICE_REV							

LEGEND: R/W = Read/Write; R = Read only

IC_DEVICE_REV

Table 2-81. IC_DEVICE_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	IC_DEVICE_REV	R	See Description.	Current device revision

Attempts to write to this command will be treated as invalid transactions - invalid data will be ignored, the appropriate flags in STATUS_CML and STATUS_WORD will be set, and the PMB_ALERT will be asserted to notify the system host of an invalid transaction.

2.4.67 (B0h) USER_DATA_00

The USER_DATA_00 command contains data from multiple other commands, and is intended to make NVM programming easier. See the product datasheet for more information.

The USER_DATA_00 command must be accessed through Block Write/Block Read transactions as shown in Section 2.1.2.

USER_DATA_00 is a paged register, however all relevant and user accessible bits reside in PAGE 0. Write and read transactions to this command with PAGE 0 active may be used for non-volatile memory programming. Read transactions to this command with PAGE 1 active will return the value of test/trim bits set by TI during device manufacturing, write transactions to this command with PAGE 1 active will be considered invalid transactions. When using this command for non-volatile memory programming, the user should only use the value from PAGE 0.

47	46	45	44	42	41	40	39
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_00							
39	38	37	36	35	34	33	32
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_00							
31	30	29	28	27	26	25	24
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_00							
23	22	21	20	19	18	17	16
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_00							
15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_00							
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_00							

LEGEND: R/W = Read/Write; R = Read only

USER_DATA_00

Table 2-82. USER_DATA_00 Register Field Descriptions

Bit	Field	Type	Reset	Description
47:0	USER_DATA_00	RW	NVM	6 bytes of user configuration data

2.4.68 (B1h) USER_DATA_01

The USER_DATA_01 command contains data from multiple other commands, and is intended to make NVM programming easier. See the product datasheet for more information.

The USER_DATA_01 command must be accessed through Block Write/Block Read transactions as shown in Section 2.1.2.

USER_DATA_01 is a paged register, however all relevant and user accessible bits reside in PAGE 0. Write and read transactions to this command with PAGE 0 active may be used for non-volatile memory programming. Read transactions to this command with PAGE 1 active will return the value of test/trim bits set by TI during device manufacturing, write transactions to this command with PAGE 1 active will be considered invalid transactions. When using this command for non-volatile memory programming, the user should only use the value from PAGE 0.

47	46	45	44	42	41	40	39
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_01							
39	38	37	36	35	34	33	32
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_01							
31	30	29	28	27	26	25	24
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_01							
23	22	21	20	19	18	17	16
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_01							
15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_01							
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_01							

LEGEND: R/W = Read/Write; R = Read only

USER_DATA_01

Table 2-83. USER_DATA_01 Register Field Descriptions

Bit	Field	Type	Reset	Description
47:0	USER_DATA_01	RW	NVM	6 bytes of user configuration data

2.4.69 (B2h) USER_DATA_02

The USER_DATA_02 command contains data from multiple other commands, and is intended to make NVM programming easier. See the product datasheet for more information.

The USER_DATA_02 command must be accessed through Block Write/Block Read transactions as shown in Section 2.1.2.

USER_DATA_02 is a paged register, however all relevant and user accessible bits reside in PAGE 0. Write and read transactions to this command with PAGE 0 active may be used for non-volatile memory programming. Read transactions to this command with PAGE 1 active will return the value of test/trim bits set by TI during device manufacturing, write transactions to this command with PAGE 1 active will be considered invalid transactions. When using this command for non-volatile memory programming, the user should only use the value from PAGE 0.

47	46	45	44	42	41	40	39
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_02							
39	38	37	36	35	34	33	32
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_02							
31	30	29	28	27	26	25	24
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_02							
23	22	21	20	19	18	17	16
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_02							
15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_02							
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_02							

LEGEND: R/W = Read/Write; R = Read only

USER_DATA_02

Table 2-84. USER_DATA_02 Register Field Descriptions

Bit	Field	Type	Reset	Description
47:0	USER_DATA_02	RW	NVM	6 bytes of user configuration data

2.4.70 (B3h) USER_DATA_03

The USER_DATA_03 command contains data from multiple other commands, and is intended to make NVM programming easier. See the product datasheet for more information.

The USER_DATA_03 command must be accessed through Block Write/Block Read transactions as shown in Section 2.1.2.

USER_DATA_03 is a paged register, however all relevant and user accessible bits reside in PAGE 0. Write and read transactions to this command with PAGE 0 active may be used for non-volatile memory programming. Read transactions to this command with PAGE 1 active will return the value of test/trim bits set by TI during device manufacturing, write transactions to this command with PAGE 1 active will be considered invalid transactions. When using this command for non-volatile memory programming, the user should only use the value from PAGE 0.

47	46	45	44	42	41	40	39
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_03							
39	38	37	36	35	34	33	32
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_03							
31	30	29	28	27	26	25	24
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_03							
23	22	21	20	19	18	17	16
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_03							
15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_03							
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_03							

LEGEND: R/W = Read/Write; R = Read only

USER_DATA_03

Table 2-85. USER_DATA_03 Register Field Descriptions

Bit	Field	Type	Reset	Description
47:0	USER_DATA_03	RW	NVM	6 bytes of user configuration data

2.4.71 (B4h) USER_DATA_04

The USER_DATA_04 command contains data from multiple other commands, and is intended to make NVM programming easier. See the product datasheet for more information.

The USER_DATA_04 command must be accessed through Block Write/Block Read transactions as shown in Section 2.1.2.

USER_DATA_04 is a paged register, however all relevant and user accessible bits reside in PAGE 0. Write and read transactions to this command with PAGE 0 active may be used for non-volatile memory programming. Read transactions to this command with PAGE 1 active will return the value of test/trim bits set by TI during device manufacturing, write transactions to this command with PAGE 1 active will be considered invalid transactions. When using this command for non-volatile memory programming, the user should only use the value from PAGE 0.

47	46	45	44	42	41	40	39
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_04							
39	38	37	36	35	34	33	32
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_04							
31	30	29	28	27	26	25	24
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_04							
23	22	21	20	19	18	17	16
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_04							
15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_04							
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_04							

LEGEND: R/W = Read/Write; R = Read only

USER_DATA_04

Table 2-86. USER_DATA_04 Register Field Descriptions

Bit	Field	Type	Reset	Description
47:0	USER_DATA_04	RW	NVM	6 bytes of user configuration data

2.4.72 (B5h) USER_DATA_05

The USER_DATA_05 command contains data from multiple other commands, and is intended to make NVM programming easier. See the product datasheet for more information.

The USER_DATA_05 command must be accessed through Block Write/Block Read transactions as shown in Section 2.1.2.

USER_DATA_05 is a paged register, however all relevant and user accessible bits reside in PAGE 0. Write and read transactions to this command with PAGE 0 active may be used for non-volatile memory programming. Read transactions to this command with PAGE 1 active will return the value of test/trim bits set by TI during device manufacturing, write transactions to this command with PAGE 1 active will be considered invalid transactions. When using this command for non-volatile memory programming, the user should only use the value from PAGE 0.

47	46	45	44	42	41	40	39
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_05							
39	38	37	36	35	34	33	32
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_05							
31	30	29	28	27	26	25	24
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_05							
23	22	21	20	19	18	17	16
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_05							
15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_05							
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_05							

LEGEND: R/W = Read/Write; R = Read only

USER_DATA_05

Table 2-87. USER_DATA_05 Register Field Descriptions

Bit	Field	Type	Reset	Description
47:0	USER_DATA_05	RW	NVM	6 bytes of user configuration data

2.4.73 (B6h) USER_DATA_06

The USER_DATA_06 command contains data from multiple other commands, and is intended to make NVM programming easier. See the product datasheet for more information.

The USER_DATA_06 command must be accessed through Block Write/Block Read transactions as shown in Section 2.1.2.

USER_DATA_06 is a paged register, however all relevant and user accessible bits reside in PAGE 0. Write and read transactions to this command with PAGE 0 active may be used for non-volatile memory programming. Read transactions to this command with PAGE 1 active will return the value of test/trim bits set by TI during device manufacturing, write transactions to this command with PAGE 1 active will be considered invalid transactions. When using this command for non-volatile memory programming, the user should only use the value from PAGE 0.

47	46	45	44	42	41	40	39
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_06							
39	38	37	36	35	34	33	32
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_06							
31	30	29	28	27	26	25	24
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_06							
23	22	21	20	19	18	17	16
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_06							
15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_06							
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_06							

LEGEND: R/W = Read/Write; R = Read only

USER_DATA_06

Table 2-88. USER_DATA_06 Register Field Descriptions

Bit	Field	Type	Reset	Description
47:0	USER_DATA_06	RW	NVM	6 bytes of user configuration data

2.4.74 (B7h) USER_DATA_07

The USER_DATA_07 command contains data from multiple other commands, and is intended to make NVM programming easier. See the product datasheet for more information.

The USER_DATA_07 command must be accessed through Block Write/Block Read transactions as shown in Section 2.1.2.

USER_DATA_07 is a paged register, however all relevant and user accessible bits reside in PAGE 0. Write and read transactions to this command with PAGE 0 active may be used for non-volatile memory programming. Read transactions to this command with PAGE 1 active will return the value of test/trim bits set by TI during device manufacturing, write transactions to this command with PAGE 1 active will be considered invalid transactions. When using this command for non-volatile memory programming, the user should only use the value from PAGE 0.

47	46	45	44	42	41	40	39
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_07							
39	38	37	36	35	34	33	32
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_07							
31	30	29	28	27	26	25	24
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_07							
23	22	21	20	19	18	17	16
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_07							
15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_07							
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_07							

LEGEND: R/W = Read/Write; R = Read only

USER_DATA_07

Table 2-89. USER_DATA_07 Register Field Descriptions

Bit	Field	Type	Reset	Description
47:0	USER_DATA_07	RW	NVM	6 bytes of user configuration data

2.4.75 (B8h) USER_DATA_08

The USER_DATA_08 command contains data from multiple other commands, and is intended to make NVM programming easier. See the product datasheet for more information.

The USER_DATA_08 command must be accessed through Block Write/Block Read transactions as shown in Section 2.1.2.

USER_DATA_08 is a paged register, however all relevant and user accessible bits reside in PAGE 0. Write and read transactions to this command with PAGE 0 active may be used for non-volatile memory programming. Read transactions to this command with PAGE 1 active will return the value of test/trim bits set by TI during device manufacturing, write transactions to this command with PAGE 1 active will be considered invalid transactions. When using this command for non-volatile memory programming, the user should only use the value from PAGE 0.

47	46	45	44	42	41	40	39
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_08							
39	38	37	36	35	34	33	32
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_08							
31	30	29	28	27	26	25	24
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_08							
23	22	21	20	19	18	17	16
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_08							
15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_08							
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_08							

LEGEND: R/W = Read/Write; R = Read only

USER_DATA_08

Table 2-90. USER_DATA_08 Register Field Descriptions

Bit	Field	Type	Reset	Description
47:0	USER_DATA_08	RW	NVM	6 bytes of user configuration data

2.4.76 (B9h) USER_DATA_09

The USER_DATA_09 command contains data from multiple other commands, and is intended to make NVM programming easier. See the product datasheet for more information.

The USER_DATA_09 command must be accessed through Block Write/Block Read transactions as shown in Section 2.1.2.

USER_DATA_09 is a shared register. Write transactions to this register will affect both channels, and read transactions to this register will return the same data regardless of the current PAGE.

47	46	45	44	42	41	40	39
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_09							
39	38	37	36	35	34	33	32
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_09							
31	30	29	28	27	26	25	24
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_09							
23	22	21	20	19	18	17	16
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_09							
15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_09							
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_09							

LEGEND: R/W = Read/Write; R = Read only

USER_DATA_09

Table 2-91. USER_DATA_09 Register Field Descriptions

Bit	Field	Type	Reset	Description
47:0	USER_DATA_09	RW	NVM	6 bytes of user configuration data

2.4.77 (BAh) USER_DATA_10

The USER_DATA_10 command contains data from multiple other commands, and is intended to make NVM programming easier. See the product datasheet for more information.

The USER_DATA_10 command must be accessed through Block Write/Block Read transactions as shown in Section 2.1.2.

USER_DATA_10 is a shared register. Write transactions to this register will affect both channels, and read transactions to this register will return the same data regardless of the current PAGE.

47	46	45	44	42	41	40	39
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_10							
39	38	37	36	35	34	33	32
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_10							
31	30	29	28	27	26	25	24
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_10							
23	22	21	20	19	18	17	16
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_10							
15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_10							
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_10							

LEGEND: R/W = Read/Write; R = Read only

USER_DATA_10

Table 2-92. USER_DATA_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
47:0	USER_DATA_10	RW	NVM	6 bytes of user configuration data

2.4.78 (BBh) USER_DATA_11

The USER_DATA_11 command contains data from multiple other commands, and is intended to make NVM programming easier. See the product datasheet for more information. USER_DATA_11 also contains the CHB_2PH anc CHB_3PH bits, which control the phase number for Channel B. Unlike other configuration bits, the CHB_3PH bit is not mapped into an MFR_SPECIFIC register.

WARNING

Enabling 3-phase mode for Channel B requires the user to update the CHB_3PH bit in USER_DATA_11. Note that the other bits in USER_DATA_11 are mapped to miscellaneous NVM configuration. The user must be careful to update only the CHB_2PH/CHB_3PH bits as specified below. Changing the other bit fields in USER_DATA_11 may lead to unexpected behavior. Refer to Bit Indexing For Block Commands for more information about updating USER_DATA commands.

The USER_DATA_11 command must be accessed through Block Write/Block Read transactions as shown in Section 2.1.2.

USER_DATA_11 is a shared register. Write transactions to this register will affect both channels, and read transactions to this register will return the same data regardless of the current PAGE.

47	46	45	44	42	41	40	39
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_11							
39	38	37	36	35	34	33	32
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_11							
31	30	29	28	27	26	25	24
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_11							
23	22	21	20	19	18	17	16
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_11							
15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_11						CHB_2PH (PAGE0)	CHB_3PH (PAGE0)
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_11							

LEGEND: R/W = Read/Write; R = Read only

USER_DATA_11

Table 2-93. USER_DATA_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
47:10 7:0	USER_DATA_11	RW	NVM	6 bytes of user configuration data.

Table 2-93. USER_DATA_11 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	CHB_2PH (PAGE 0 only)	RW	NVM	**CHB_2PH (PAGE 0):** Controls Channel B Phase number. Refer to Table 2-94. Note this bit is mirrored into MFR_SPECIFIC_11. Updates to CHB_2PH via USER_DATA_11 will be reflected in MFR_SPECIFIC_11. Likewise, updates to CHB_2PH via MFR_SPECIFIC_11 will be reflected in USER_DATA_11.
8	CHB_3PH (PAGE 0 only)	RW	NVM	**CHB_3PH (PAGE 0):** Controls Channel B Phase number. This bit is not mapped into a MFR_SPECIFIC register, and must be updated via USER_DATA_11.

Table 2-94. Channel B Phase Configuration

Channel B Phases	CHB_2PH	CHB_3PH
1	1b	0b
2	0b	0b
3	0b	1b

2.4.79 (BCh) USER_DATA_12

The USER_DATA_12 command contains data from multiple other commands, and is intended to make NVM programming easier. See the product datasheet for more information.

The USER_DATA_12 command must be accessed through Block Write/Block Read transactions as shown in Section 2.1.2.

USER_DATA_12 is a shared register. Write transactions to this register will affect both channels, and read transactions to this register will return the same data regardless of the current PAGE.

47	46	45	44	42	41	40	39
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_12							
39	38	37	36	35	34	33	32
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_12							
31	30	29	28	27	26	25	24
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_12							
23	22	21	20	19	18	17	16
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_12							
15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_12							
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
USER_DATA_12							

LEGEND: R/W = Read/Write; R = Read only

USER_DATA_12

Table 2-95. USER_DATA_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
47:0	USER_DATA_12	RW	NVM	6 bytes of user configuration data

2.4.80 (D0h) MFR_SPECIFIC_00

The MFR_SPECIFIC_00 command is used to configure per-phase overcurrent levels, current share thresholds, and other miscellaneous settings.

The MFR_SPECIFIC_00 command must be accessed through Write Word/Read Word transactions as shown in Section 2.1.2.

MFR_SPECIFIC_00 is a paged register. Note that PAGE 0 and PAGE 1 do not refer to Channel A/Channel B functionality.

15	14	13	12	11	10	9	8
R	R	RW	RW	RW	RW	RW	RW
0	0	TSNSB (PAGE 0) TI_INTERNAL (PAGE 1)	TI_INTERNAL (PAGE 0) XRLFLT (PAGE 1)	TI_INTERNAL (PAGE 0) FXOVFB_EN (PAGE 1)	TI_INTERNAL	VDACDWN_OFS	
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VDACUP_OFS		CUR_SHARE_TH		PHASE_OCL			

LEGEND: R/W = Read/Write; R = Read only

MFR_SPECIFIC_00

Table 2-96. MFR_SPECIFIC_00 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	Not used	R	00b	Not used and always set to 0b.
13	TSNSB (PAGE 0) TI_INTERNAL (PAGE 1)	RW	NVM	**TSNSB (PAGE 0):** Channel B TSNS enable bit 0b: Channel B is configured for temperature sensing. TSNS for channel B is enabled. 1b: Channel B is not configured for temperature sensing, TSNS for channel B is disabled. **TI_INTERNAL (PAGE 1):** This bit is writable, but should not be modified from factory default.
12	TI_INTERNAL (PAGE 0) XRLFLT (PAGE 1)	RW	NVM	**TI_INTERNAL (PAGE 0):** This bit is writable, but should not be modified from factory default. **XRLFLT (PAGE 1):** 0b: A fault in one channel will turn off the other channel (either hiccup or latch-off) 1b: A fault in one channel does not affect the other channel.
11	TI_INTERNAL (PAGE 0) FXOVFB_EN (PAGE 1)	RW	NVM	**TI_INTERNAL (PAGE 0):** These bits are writable, but should not be modified from factory default. **FXOVFB_EN (PAGE 1):** 0b: Fixed overvoltage fault for channel B is enabled 1b: Fixed overvoltage fault for channel B is disabled.
10	TI_INTERNAL	RW	NVM	These bits are writable, but should not be modified from factory default. Note that this is a paged bit. There are separate settings for PAGE 0 and PAGE 1, which may have different values, and should not be modified from factory default settings.

Table 2-96. MFR_SPECIFIC_00 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9:8	VDACDWN_OFS	RW	NVM	Used to configure the reference DAC offset applied to each channel (PAGE 0 for channel A and PAGE 1 for channel B) during DVID down operations. 00b: Add 0 to DAC counter 01b: Add 2 to DAC counter 10b: Add 4 to DAC counter 11b: Add 6 to DAC counter
7:6	VDACUP_OFS	RW	NVM	Used to configure the reference DAC offset applied to each channel (PAGE 0 for channel A and PAGE 1 for channel B) during DVID up operations. 00b: Add 0 to DAC counter 01b: Add 2 to DAC counter 10b: Add 4 to DAC counter 11b: Add 6 to DAC counter
5:4	CUR_SHARE_TH	RW	NVM	Current imbalance warning threshold. Sets the maximum allowable current imbalance between phases in a given channel (PAGE 0 for channel A, PAGE 1 for channel B). 00b: 5A 01b: 10A 10b: 20A 11b: Current imbalance warning disabled.
3:0	PHASE_OCL	RW	NVM	Per-phase over-current limit for the phases in a given channel (PAGE 0 for channel A, PAGE 1 for channel B). See the table below for more information

The table below describes the per-phase overcurrent limit settings.

Table 2-97. PHASE_OCL settings

PHASE_OCL (binary)	Per-phase overcurrent limit (A)
0000b (0h)	14 A
0001b (1h)	18 A
0010b (2h)	22 A
0011b (3h)	26 A
0100b (4h)	30 A
0101b (5h)	34 A
0110b (6h)	38 A
0111b (7h)	42 A
1000b (8h)	46 A
1001b (9h)	50 A
1010b (Ah)	54 A
1011b (Bh)	58 A
1100b (Ch)	62 A
1101b (Dh)	66 A
1110b (Eh)	70 A
1111b (Fh)	74 A

2.4.81 (D3h) MFR_SPECIFIC_03

The MFR_SPECIFIC_03 command is used to return information regarding current imbalance warnings for each phase.

The MFR_SPECIFIC_03 command must be accessed through Read Word transactions as shown in Section 2.1.2.

MFR_SPECIFIC_03 is a paged register. In order to access MFR_SPECIFIC_03 command for channel A, PAGE must be set to 00h. In order to access the MFR_SPECIFIC_03 register for channel B, PAGE must be set to 01h.

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	PH6_IB
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
PH5_IB	PH4_IB	PH3_IB	PH2_IB	PH1_IB	ACTIVE_PHASES		

LEGEND: R/W = Read/Write; R = Read only

MFR_SPECIFIC_03

Table 2-98. MFR_SPECIFIC_03 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:9	Not used	R	0	Not used and always set to 0.
8	PH6_IB	R	0	0b: Phase 6 current of the active PAGE is NOT imbalanced 1b: Phase 6 current of the active PAGE is imbalanced
7	PH5_IB	R	0	0b: Phase 5 current of the active PAGE is NOT imbalanced 1b: Phase 5 current of the active PAGE is imbalanced
6	PH4_IB	R	0	0b: Phase 4 current of the active PAGE is NOT imbalanced 1b: Phase 4 current of the active PAGE is imbalanced
5	PH3_IB	R	0	0b: Phase 3 current of the active PAGE is NOT imbalanced 1b: Phase 3 current of the active PAGE is imbalanced
4	PH2_IB	R	0	0b: Phase 2 current of the active PAGE is NOT imbalanced 1b: Phase 2 current of the active PAGE is imbalanced
3	PH1_IB	R	0	0b: Phase 1 current of the active PAGE is NOT imbalanced 1b: Phase 1 current of the active PAGE is imbalanced
2:0	ACTIVE_PHASES	R	Current Status	Returns the number of active phases for the current PAGE, accounting for phases which may have been dropped due to dynamic phase shedding

Bits 8:3 will be cleared to 0b following a successful read of MFR_SPECIFIC_03, with PAGE 0 active.

Bits 5:3 will be cleared to 0b following a successful read of MFR_SPECIFIC_03, with PAGE 1 active.

Note that phases 4-6 are not available for channel B (PAGE 1).

Attempts to write to this command will be ignored.

2.4.82 (D4h) MFR_SPECIFIC_04

The MFR_SPECIFIC_04 command is used to return the output voltage for the active channel, in linear format (READ_VOUT uses the VID format).

The MFR_SPECIFIC_04 command must be accessed through Read Word transactions as shown in Section 2.1.2.

MFR_SPECIFIC_04 is a Linear format command, as described in Section 2.1.1.

MFR_SPECIFIC_04 is a paged register. In order to access MFR_SPECIFIC_04 command for channel A, PAGE must be set to 00h. In order to access the MFR_SPECIFIC_04 register for channel B, PAGE must be set to 01h.

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
VOUT_LIN_EXP					VOUT_LIN_MAN		
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
VOUT_LIN_MAN							

LEGEND: R/W = Read/Write; R = Read only

MFR_SPECIFIC_04

Table 2-99. MFR_SPECIFIC_04 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	VOUT_LIN_EXP	R	Current Status	Linear format two's complement exponent.
10:0	VOUT_LIN_MAN	R	Current Status	Linear format two's complement mantissa.

Attempts to write to this command will be ignored.

2.4.83 (D5h) MFR_SPECIFIC_05

The MFR_SPECIFIC_05 command is used to trim the output voltage of the active channel, by applying an offset to the currently selected VID code.

The MFR_SPECIFIC_05 command must be accessed through Write Byte/Read Byte transactions as shown in Section 2.1.2. The effective VID offset is calculated as shown below:

VID_{OFFSET} = VID_OFFSET × 1.25 mV + VID_OFFSET_EXTN

MFR_SPECIFIC_05 is a paged register. In order to access MFR_SPECIFIC_05 command for channel A, PAGE must be set to 00h. In order to access the MFR_SPECIFIC_05 register for channel B, PAGE must be set to 01h.

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VID_OFFSET_EXTN		VID_OFFSET					

LEGEND: R/W = Read/Write; R = Read only

MFR_SPECIFIC_05

Table 2-100. MFR_SPECIFIC_05 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	VID_OFFSET_EXTN	RW	NVM	VID offset extension. See below for more information.
5:0	VID_OFFSET	RW	NVM	VID offset in signed two's complement format. LSB = 1.25 mV. See below for more information.

Table 2-101. VID Offset settings

VID_OFFSET_EXTN (binary)	Offset "Extension" Added to VID_OFFSET[5:0]
00b	0 mV
01b	20 mV
10b	0 mV
11b	-19.375 mV

2.4.84 (D6h) MFR_SPECIFIC_06

The MFR_SPECIFIC_06 command is used to configure dynamic load line options for both channels, and select Auto-DCM operation.

The MFR_SPECIFIC_06 command must be accessed through Write Word/Read Word transactions as shown in Section 2.1.2.

MFR_SPECIFIC_06 is a paged register. In order to access MFR_SPECIFIC_06 command for channel A, PAGE must be set to 00h. In order to access the MFR_SPECIFIC_06 register for channel B, PAGE must be set to 01h.

15	14	13	12	11	10	9	8
RW	RW	RW	RW	R	RW	RW	RW
NOSKIP	DAC_DOWN_DCLL			0	DAC_UP_DCLL		
7	6	5	4	3	2	1	0
R	RW	RW	RW	RW	RW	RW	RW
0	DAC_DOWN_ACLL			DAC_UP_ACLL			

LEGEND: R/W = Read/Write; R = Read only

MFR_SPECIFIC_06

Table 2-102. MFR_SPECIFIC_06 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	NOSKIP	RW	NVM	0b: Auto DCM is disabled. Device will use SKIP pin when DCM is required. 1b: Auto DCM is enabled. Device will tri-state PWM pins when DCM is required.
14:12	DAC_DOWN_DCLL	RW	NVM	DC Loadline during VID down transition. See Table 2-103 and Table 2-104 for more information.
11	Not used.	R	0	Not used and set to 0.
10:8	DAC_UP_DCLL	RW	NVM	DC load line during VID up transition. See Table 2-105 and Table 2-106 for more information.
7	Not used.	R	0	Not used and set to 0.
6:4	DAC_DOWN_ACLL	RW	NVM	AC load line during VID down transition. See Table 2-107 for more information.
3:0	DAC_UP_ACLL	RW	NVM	AC load line during VID up transition. See Table 2-108 for more information.

The dynamic DC load line settings are calculated based on the configuration of VOUT_DROOP. There are 64 available VOUT_DROOP "bins" for channel A, and 16 for channel B. During dynamic VID transitions, the effective load line setting will changed according to the tables below. In the tables below, *CURRENT_BIN*, refers to the currently selected static VOUT_DROOP setting.

The dynamic AC load line settings are calculated based on the configuration of MFR_SPECIFIC_07. Similarly, in the tables below, *CURRENT_BIN*, refers to the currently selected setting of the ACLL bits in MFR_SPECIFIC_07.

Table 2-103. Dynamic DC Load Line Settings, VID Down Transition, Channel A

DAC_DOWN_DCLL (PAGE 0) (binary)	Effective VOUT_DROOP "bin"
000b	*CURRENT_BIN*
001b	*MIN(63d, CURRENT_BIN + 1d)*
010b	*MIN(63d, CURRENT_BIN + 2d)*
011b	*MIN(63d, CURRENT_BIN + 3d)*
100b	*MIN(63d, CURRENT_BIN + 4d)*
101b	*MIN(63d, CURRENT_BIN + 8d)*
110b	*MIN(63d, CURRENT_BIN + 12d)*

Table 2-103. Dynamic DC Load Line Settings, VID Down Transition, Channel A (continued)

DAC_DOWN_DCLL (PAGE 0) (binary)	Effective VOUT_DROOP "bin"
111b	*MIN(63d, CURRENT_BIN + 16d)*

Table 2-104. Dynamic DC Load Line Settings, VID Down Transition, Channel B

DAC_DOWN_DCLL (PAGE 1) (binary)	Effective VOUT_DROOP "bin"
000b	*CURRENT_BIN*
001b	*MIN(15d, CURRENT_BIN + 1d)*
010b	*MIN(15d, CURRENT_BIN + 2d)*
011b	*MIN(15d, CURRENT_BIN + 3d)*
100b	*MIN(15d, CURRENT_BIN + 4d)*
101b	*MIN(15d, CURRENT_BIN + 8d)*
110b	*MIN(15d, CURRENT_BIN + 12d)*
111b	15d

Table 2-105. Dynamic DC Load Line Settings, VID Up Transition, Channel A

DAC_UP_DCLL (PAGE 0) (binary)	Effective VOUT_DROOP "bin"
000b	*CURRENT_BIN*
001b	*MAX(0d, CURRENT_BIN - 1d)*
010b	*MAX(0d, CURRENT_BIN - 2d)*
011b	*MAX(0d, CURRENT_BIN - 4d)*
100b	*MAX(0d, CURRENT_BIN - 8d)*
101b	*MAX(0d, CURRENT_BIN - 12d)*
110b	*MAX(0d, CURRENT_BIN - 16d)*
111b	*MAX(0d, CURRENT_BIN - 20d)*

Table 2-106. Dynamic DC Load Line Settings, VID Up Transition, Channel B

DAC_UP_DCLL (PAGE 1) (binary)	Effective VOUT_DROOP "bin"
000b	*CURRENT_BIN*
001b	*MAX(0d, CURRENT_BIN - 1d)*
010b	*MAX(0d, CURRENT_BIN - 2d)*
011b	*MAX(0d, CURRENT_BIN - 4d)*
100b	*MAX(0d, CURRENT_BIN - 8d)*
101b	*MAX(0d, CURRENT_BIN - 12d)*
110b	*MAX(0d, CURRENT_BIN - 16d)*
111b	*MAX(0d, CURRENT_BIN - 20d)*

Table 2-107. Dynamic AC Load Line Settings, VID Down Transition, Channels A and B

DAC_DOWN_ACLL (PAGE 0/1) (binary)	Effective AC Load line "bin"
000b	*CURRENT_BIN*
001b	*MIN(63d, CURRENT_BIN + 1d)*
010b	*MIN(63d, CURRENT_BIN + 2d)*
011b	*MIN(63d, CURRENT_BIN + 3d)*
100b	*MIN(63d, CURRENT_BIN + 4d)*
101b	*MIN(63d, CURRENT_BIN + 5d)*

Table 2-107. Dynamic AC Load Line Settings, VID Down Transition, Channels A and B (continued)

DAC_DOWN_ACLL (PAGE 0/1) (binary)	Effective AC Load line "bin"
110b	*MIN(63d, CURRENT_BIN + 6d)*
111b	*MIN(63d, CURRENT_BIN + 7d)*

Table 2-108. Dynamic AC Load Line Settings, VID Up Transition, Channels A and B

DAC_UP_ACLL (PAGE 0/1) (binary)	Effective AC Load line "bin"
0000b	*CURRENT_BIN*
0001b	*MAX(0d, CURRENT_BIN - 1d)*
0010b	*MAX(0d, CURRENT_BIN - 2d)*
0011b	*MAX(0d, CURRENT_BIN - 3d)*
0100b	*MAX(0d, CURRENT_BIN - 4d)*
0101b	*MAX(0d, CURRENT_BIN - 5d)*
0110b	*MAX(0d, CURRENT_BIN - 6d)*
0111b	*MAX(0d, CURRENT_BIN - 7d)*
1000b	*MAX(0d, CURRENT_BIN - 8d)*
1001b	*MAX(0d, CURRENT_BIN - 9d)*
1010b	*MAX(0d, CURRENT_BIN - 10d)*
1011b	*MAX(0d, CURRENT_BIN - 11d)*
1100b	*MAX(0d, CURRENT_BIN - 12d)*
1101b	*MAX(0d, CURRENT_BIN - 13d)*
1110b	*MAX(0d, CURRENT_BIN - 14d)*
1111b	*MAX(0d, CURRENT_BIN - 15d)*

2.4.85 (D7h) MFR_SPECIFIC_07

The MFR_SPECIFIC_07 command is used to configure the internal loop compensation for both channels. See the product datasheet for more information.

The MFR_SPECIFIC_07 command must be accessed through Write Word/Read Word transactions as shown in Section 2.1.2.

MFR_SPECIFIC_07 is a paged register. In order to access MFR_SPECIFIC_07 command for channel A, PAGE must be set to 00h. In order to access the MFR_SPECIFIC_07 register for channel B, PAGE must be set to 01h.

15	14	13	12	11	10	9	8
R	R	RW	RW	RW	RW	RW	RW
0	0	INT_GAIN		INT_TC			
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
AC_GAIN		ACLL					

LEGEND: R/W = Read/Write; R = Read only

MFR_SPECIFIC_07

Table 2-109. MFR_SPECIFIC_07 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	Not used	R	0	Not used and set to 0.
13:12	INT_GAIN	RW	NVM	Integration path gain. See Table 2-110.
11:8	INT_TC	RW	NVM	Integration time constant. See Table 2-111.
7:6	AC_GAIN	RW	NVM	AC path gain. See Table 2-112.
5:0	ACLL	RW	NVM	AC Load Line. See Table 2-113.

Table 2-110. Integration path gain settings

INT_GAIN (binary)	Integration path gain (V/V)
00b	2 × AC_GAIN
01b	1 × AC_GAIN
10b	0.66 × AC_GAIN
11b	0.5 × AC_GAIN

Table 2-111. Integration time constant settings

INT_TC (binary)	Time constant (µs)
0000b	5
0001b	10
0010b	15
0011b	20
0100b	25
0101b	30
0110b	35
0111b	40
1000b	1
1001b	2
1010b	3
1011b	4
1100b	5

Table 2-111. Integration time constant settings (continued)

INT_TC (binary)	Time constant (µs)
1101b	6
1110b	7
1111b	8

Table 2-112. AC path gain settings

AC_GAIN (binary)	AC path gain (V/V)
00b	1
01b	1.5
10b	2
11b	0.5

Table 2-113. AC Load line settings

Bin	ACLL (hex)	AC Load line (mΩ)
0	00h	0.0000
1	01h	0.1250
2	02h	0.2500
3	03h	0.3125
4	04h	0.3750
5	05h	0.4375
6	06h	0.5000
7	07h	0.5625
8	08h	0.6250
9	09h	0.7500
10	0Ah	0.7969
11	0Bh	0.8125
12	0Ch	0.8281
13	0Dh	0.8438
14	0Eh	0.8594
15	0Fh	0.8750
16	10h	0.8906
17	11h	0.9063
18	12h	0.9219
19	13h	0.9375
20	14h	0.9531
21	15h	0.9688
22	16h	0.9844
23	17h	1.000
24	18h	1.0156
25	19h	1.0313
26	1Ah	1.0469
27	1Bh	1.0625
28	1Ch	1.1250
29	1Dh	1.2500
30	1Eh	1.3750
31	1Fh	1.5000
32	20h	1.6250

Table 2-113. AC Load line settings (continued)

Bin	ACLL (hex)	AC Load line (mΩ)
33	21h	1.7500
34	22h	1.8750
35	23h	1.9375
36	24h	2.000
37	25h	2.0625
38	26h	2.1250
39	27h	2.1875
40	28h	2.2500
41	29h	2.375
42	2Ah	2.4218
43	2Bh	2.4375
44	2Ch	2.4531
45	2Dh	2.4687
46	2Eh	2.4843
47	2Fh	2.5000
48	30h	2.5156
49	31h	2.5312
50	32h	2.5468
51	33h	2.5625
52	34h	2.5781
53	35h	2.5937
54	36h	2.609
55	37h	2.625
56	38h	2.6406
57	39h	2.6562
58	3Ah	2.6718
59	3Bh	2.6875
60	3Ch	2.750
61	3Dh	2.875
62	3Eh	3.000
63	3Fh	3.125

2.4.86 (D8h) MFR_SPECIFIC_08

The MFR_SPECIFIC_08 command is used to identify catastrophic faults which occur first, and store this information to NVM. See the product datasheet for more information.

The MFR_SPECIFIC_08 command must be accessed through Write Byte/Read Byte transactions as shown in Section 2.1.2.

MFR_SPECIFIC_08 is a shared register. Transactions to this register do not require specific PAGE settings. However, note that channels A and B have independent bit fields within the command.

7	6	5	4	3	2	1	0
R	R	RW	RW	RW	RW	RW	RW
0	0	CF_CHA			CF_CHB		

LEGEND: R/W = Read/Write; R = Read only

MFR_SPECIFIC_08

Table 2-114. MFR_SPECIFIC_08 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	Not used	R	0	Not used and set to 0.
5:3	CF_CHA	RW	NVM	Catastrophic fault record for channel A.
2:0	CF_CHB	RW	NVM	Catastrophic fault record for channel B.

Whenever a catastrophic fault occurs, the first event detected will trigger the MFR_SPECIFIC_08 command to update according to the tables below. This recording happens independently for channel A and channel B. If the PMBus host issues a STORE_DEFAULT_ALL, this information will be committed to NVM, and may be retrieved at a later time. In order to clear the record for either channel, the PMBus host must write the corresponding bits (CF_CHA for channel A, CF_CHB for channel B) to 000b, and issue STORE_DEFAULT_ALL.

Attempts to write any non-zero value to this command will be treated as invalid data - data will be ignored, the appropriate flags in STATUS_CML, and STATUS_WORD, will be set, and the PMB_ALERT pin will be asserted to notify the host of the invalid transaction.

Table 2-115. Catastrophic Fault Recording Interpretation

CF_CHA / CF_CHB (binary)	Interpretation
000b	No fault occurred
001b	OVF occurred, power conversion was disabled
010b	OVF occurred, power conversion was enabled
011b	IIN Overcurrent fault occurred
100b	IOUT Overcurrent fault occurred
101b	Overtemperature fault occurred
110b	Power stage fault occurred
111b	Input overpower warning occurred

2.4.87 (D9h) MFR_SPECIFIC_09

The MFR_SPECIFIC_09 command is used to configure non-linear transient performance enhancements such as undershoot reduction (USR) and overshoot reduction (OSR). See the product datasheet for more information.

The MFR_SPECIFIC_09 command must be accessed through Write Word/Read Word transactions as shown in Section 2.1.2.

MFR_SPECIFIC_09 is a paged register. In order to access MFR_SPECIFIC_09 command for channel A, PAGE must be set to 00h. In order to access the MFR_SPECIFIC_09 register for channel B, PAGE must be set to 01h.

15	14	13	12	11	10	9	8
RW	RW	RW	RW	R	RW	RW	RW
USR2 (PAGE 0 only)				0	MINOFF		TBLANK
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
TBLANK		PH_USR1	OSR_USR_HYS		USR1		

LEGEND: R/W = Read/Write; R = Read only

MFR_SPECIFIC_09

Table 2-116. MFR_SPECIFIC_09 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	USR2 (PAGE 0 only)	RW	NVM	Undershoot reduction level 2 settings. These bits are supported for PAGE 0 (channel A) only. See Table 2-117.
11	Not used	R	0	Not used and set to 0.
10:9	MINOFF	RW	NVM	Minimum OFF time settings. See Table 2-118.
8:6	TBLANK	RW	NVM	Rising edge blanking time. See Table 2-119.
5	PH_USR1	RW	NVM	Maximum number of phases added in USR level 1. 0b: USR level 1 may add up to 3 phases maximum 1b: USR level 1 may add up to 4 phases maximum
4:3	OSR_USR_HYS	RW	NVM	Overshoot reduction, undershoot reduction hysteresis. See Table 2-120.
2:0	USR1	RW	NVM	Undershoot reduction level 1 settings. See Table 2-121.

Table 2-117. USR Level 2 Settings

USR2 (PAGE 0 only)	USR Level 2 Voltage Setting (mV)
000b	140
001b	180
010b	220
011b	260
100b	300
101b	340
110b	380
111b	Disabled

Table 2-118. Minimum OFF Time Settings

MINOFF (binary)	Minimum Off Time (ns)
00b	45
01b	60
10b	75

Table 2-118. Minimum OFF Time Settings (continued)

MINOFF (binary)	Minimum Off Time (ns)
11b	90

Table 2-119. Rising Edge Blanking Time Settings

TBLANK (binary)	Rising Edge Blanking Time (ns)
000b	36
001b	42
010b	48
011b	54
100b	60
101b	66
110b	72
111b	78

Table 2-120. OSR/USR Voltage Hysteresis

OSR_USR_HYS (binary)	OSR/USR Hysteresis (mV)
00b	5
01b	10
10b	15
11b	20

Table 2-121. USR Level 1 Settings

USR1 (binary)	USR Level 1 Settings (mV)
000b	90
001b	120
010b	150
011b	180
100b	210
101b	240
110b	270
111b	Disabled

2.4.88 (DAh) MFR_SPECIFIC_10

The MFR_SPECIFIC_10 command is used to configure input current sensing, and set the maximum output current. These values are used for input current and output current telemetry. See the product datasheet for more information.

The MFR_SPECIFIC_10 command must be accessed through Write Word/Read Word transactions as shown in Section 2.1.2.

MFR_SPECIFIC_10 is a paged register. In order to access MFR_SPECIFIC_10 command for channel A, PAGE must be set to 00h. In order to access the MFR_SPECIFIC_10 register for channel B, PAGE must be set to 01h. Note that input current calibration is shared across both channels, but the configuration makes use of both PAGEs.

15	14	13	12	11	10	9	8
RW	RW	RW	RW	R	RW	RW	RW
IIN_MAX (PAGE 0, bits 15:8) IIN_GAIN_CTRL (PAGE 1, bit 13) IIN_OFS (PAGE 1, bits 12:8)							
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
IOUT_MAX (PAGE 0, PAGE 1)							

LEGEND: R/W = Read/Write; R = Read only

MFR_SPECIFIC_10

Table 2-122. MFR_SPECIFIC_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	IIN_MAX (PAGE 0)	RW	NVM	Maximum IIN setting. LSB = 0.25 A. Valid values range from 0 A to 63.75 A.
13	IIN_GAIN_CTRL (PAGE 1)	RW	NVM	Used to increase the effective IIN_RGAIN. See IIN_RGAIN in MFR_SPECIFIC_12 for more information.
12:8	IIN_OFS (PAGE 1)	RW	NVM	Input current sense offset calibration. See the product datasheet for more information.
7:0	IOUT_MAX	RW	NVM	Sets the maximum output current for each channel (PAGE 0 for channel A, PAGE 1 for channel B). LSB = 1A. This value is used in telemetry calculations, as well as to determine the default IOUT_OC_FAULT_LIMIT and IOUT_OC_WARN_LIMIT values.

Table 2-123. Input Current Offset Calibration Settings

IIN_OFS (hex)	IIN Offset (A)
00h	0
01h	0.1
02h	0.2
03h	0.3
04h	0.4
05h	0.5
06h	0.6
07h	0.7
08h	0.8
09h	0.9
0Ah	1.0
0Bh	1.1
0Ch	1.2
0Dh	1.3
0Eh	1.4

Table 2-123. Input Current Offset Calibration Settings (continued)

IIN_OFS (hex)	IIN Offset (A)
0Fh	1.5
10h	-1.6
11h	-1.5
12h	-1.4
13h	-1.3
14h	-1.2
15h	-1.1
16h	-1.0
17h	-0.9
18h	-0.8
19h	-0.7
1Ah	-0.6
1Bh	-0.5
1Ch	-0.4
1Dh	-0.3
1Eh	-0.2
1Fh	-0.1

2.4.89 (DBh) MFR_SPECIFIC_11

The MFR_SPECIFIC_11 command is used to configure the boot-up voltage for each channel.

The MFR_SPECIFIC_11 command must be accessed through Write Byte/Read Byte transactions as shown in Section 2.1.2.

MFR_SPECIFIC_11 is a paged register. In order to access MFR_SPECIFIC_11 command for channel A, PAGE must be set to 00h. In order to access the MFR_SPECIFIC_11 register for channel B, PAGE must be set to 01h.

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VBOOT_VID							

LEGEND: R/W = Read/Write; R = Read only

MFR_SPECIFIC_11

Table 2-124. MFR_SPECIFIC_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VBOOT_VID	RW	NVM	Sets the output voltage for each channel at boot-up, in VID format.

2.4.90 (DCh) MFR_SPECIFIC_12

The MFR_SPECIFIC_12 command is used to configure input current sensing, OSR, and other miscellaneous settings.

The MFR_SPECIFIC_12 command must be accessed through Write Word/Read Word transactions as shown in Section 2.1.2.

MFR_SPECIFIC_12 is a paged register. In order to access MFR_SPECIFIC_12 command for channel A, PAGE must be set to 00h. In order to access the MFR_SPECIFIC_12 register for channel B, PAGE must be set to 01h.

15	14	13	12	11	10	9	8
RW	RW	R	RW	RW	RW	RW	RW
IIN_RGAIN (PAGE 0 only)		0	IIN_CALC_EN (PAGE 0 only)	IIN_CALC_MODE (PAGE 0 only)	OSR		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
OSR_INT_SET				OSR_TRUNC_BB	TI_INTERNAL		

LEGEND: R/W = Read/Write; R = Read only

MFR_SPECIFIC_12

Table 2-125. MFR_SPECIFIC_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	IIN_RGAIN (PAGE 0 only)	RW	NVM	Input shunt resistance value. Combined with IIN_RGAIN, IIN_OFS, IIN_MAX to calibrate measured input current sensing. See Table 2-126 for more information. Note that finer adjustments can be made using IIN_MAX. See the product datasheet for more information.
12	IIN_CALC_EN (PAGE 0 only)	RW	NVM	0b: Input current reporting is calculated based input voltage, and output power. 1b: Input current reporting is measured using the voltage at the VIN_CSNIN and CSPIN pins.
11	IIN_CALC_MODE (PAGE 0 only)	RW	NVM	0b: Include both channels in calculated input current reporting 1b: Include only channel A in calculated input current reporting
10:8	OSR	RW	NVM	Overshoot reduction threshold settings. See Table 2-127
7:4	OSR_INTSET	RW	NVM	Integration time constant during OSR operation. See Table 2-127.
3	OSR_TRUNC_BB	RW	NVM	0b: Disable pulse truncation and body breaking during OSR 1b: Enable pulse truncation and body breaking during OSR
2:0	TMAX	RW	NVM	Selects the temperature at which the VR_HOT pin is asserted. Refer to Table 2-129

Table 2-126. Input Current Shunt Resistance Value

IIN_GAIN_CTRL (binary) (See MFR_SPECIFIC_10)	IIN_RGAIN (binary)	Effective IIN Shunt Value (mΩ)
0b	00b	0.15
0b	01b	0.25
0b	10b	0.3
0b	11b	0.5
1b	00b	1.2
1b	01b	2.0
1b	10b	2.4
1b	11b	4.0

Table 2-127. Overshoot reduction (OSR) Threhold Settings

OSR (binary)	OSR Threshold (mV)
000b	100
001b	150
010b	200
011b	250
100b	300
101b	350
110b	400
111b	Disabled

Table 2-128. Integration Time Constant during OSR

OSR_INTSET (binary)	Integration Time Constant (µs)
0000b	1
0001b	2
0010b	3
0011b	4
0100b	5
0101b	6
0110b	7
0111b	8
1000b	12
1001b	13
1010b	14
1011b	15
1100b	16
1101b	17
1110b	18
1111b	19

Table 2-129. Maximum Temperature Settings

TMAX (binary)	Maximum Temperature (°C)
000b	90
001b	95
010b	100
011b	105
100b	110
101b	115
110b	120
111b	125

2.4.91 (DDh) MFR_SPECIFIC_13

The MFR_SPECIFIC_13 command is used to configure output voltage slew rates, VR Mode, and other miscellaneous settings.

The MFR_SPECIFIC_13 command must be accessed through Write Word/Read Word transactions as shown in Section 2.1.2.

MFR_SPECIFIC_13 is a paged register. In order to access MFR_SPECIFIC_13 command for channel A, PAGE must be set to 00h. In order to access the MFR_SPECIFIC_13 register for channel B, PAGE must be set to 01h.

15	14	13	12	11	10	9	8
RW	RW	R	RW	RW	RW	R	RW
PIN_OPW_EN (PAGE 0 only)	BLK_TAO_LOW (PAGE 0 only)	0	CHB_2PH (PAGE 0 only)	OTF_DFLT (PAGE 0 only)	TAO_LOW_TH (PAGE 0 only)	0	VBOOT_SR
7	6	5	4	3	2	1	0
RW	RW	RW	RW	R	RW	RW	RW
VR_MODE			TI_INTERNAL				

LEGEND: R/W = Read/Write; R = Read only

MFR_SPECIFIC_13

Table 2-130. MFR_SPECIFIC_13 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PIN_OPW_EN (PAGE 0 only)	RW	NVM	Enable or disable input over-power warning 0b: Enable input overpower warning 1b: Disable input overpower warning
14	BLK_TAO_LOW (PAGE 0 only)	RW	NVM	Enable or disable TAO low fault detection 0b: TAO Low fault enabled 1b: TAO Low fault disabled
12	CHB_2PH (PAGE 0 only)	RW	NVM	Selects whether channel B has 1 or 2 phases available 0b: Channel B may be up to two phases. 1b: Channel B may be one phase only.
11	OTF_DFLT (PAGE 0 only)	RW	NVM	Selects the default value of OT_FAULT_LIMIT 0b: Default OT_FAULT_LIMIT is 115 °C 1b: Default OT_FAULT_LIMIT is 135 °C
10	TAO_LOW_TH (PAGE 0 only)	RW	NVM	Selects the TAO voltage thresholds for detection of TAO Low faults. 0b: 160 mV rising, 100 mV falling 1b: 280 mV rising, 230 mV falling
8	VBOOT_SR	RW	NVM	Selects rise time of the output voltage during boot-up (soft-start time) 0b: Boot-up occurs at 1/4 the slew rate commanded by VOUT_TRANSITION_RATE. 1b: Boot-up occurs at 1/16 the slew rate commanded by VOUT_TRANSITION_RATE.
7:5	VR_MODE	RW	NVM	100b: 10-mV DAC Mode 111b: 5-mV DAC Mode
4:0	TI_INTERNAL	RW	NVM	TI Internal bits. These bits should not be modified from factory default settings

2.4.92 (DEh) MFR_SPECIFIC_14

The MFR_SPECIFIC_14 command is used to configure dynamic phase shedding, and compensation ramp amplitude, and dynamic ramp amplitude during USR, and different power states.

The MFR_SPECIFIC_14 command must be accessed through Write Word/Read Word transactions as shown in Section 2.1.2.

MFR_SPECIFIC_14 is a paged register. In order to access MFR_SPECIFIC_14 command for channel A, PAGE must be set to 00h. In order to access the MFR_SPECIFIC_14 register for channel B, PAGE must be set to 01h.

15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
DPS_6TO5_FINE_DROP (PAGE 0 only)		DPS_5TO4_FINE_DROP (PAGE 0 only)		DPS_4TO3_FINE_DROP (PAGE 0 only)		DPS_3TO2_FINE_DROP	
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
DPS_EN	DYN_RAMP_USR		DYN_RAMP_2 PH	DYN_RAMP_1 PH	RAMP		

LEGEND: R/W = Read/Write; R = Read only

MFR_SPECIFIC_14

Table 2-131. MFR_SPECIFIC_14 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	DPS_6TO5_FINE_DROP (PAGE 0 only)	RW	NVM	Dynamic phase drop threshold, fine adjustment, 6 phases to 5 phases. Set as an offset from peak efficiency point per phase in Amperes. Phases drop when average phase current reaches the stated threshold. $I_{EFF(PEAK)}$ refers to the value selected by DPS_COURSE_TH in MFR_SPECIFIC_15. 00b: Threshold = 5 × $I_{EFF(PEAK)}$ – 2 A 01b: Threshold = 5 × $I_{EFF(PEAK)}$ 10b: Threshold = 5 × $I_{EFF(PEAK)}$ + 2 A 11b: Threshold = 5 × $I_{EFF(PEAK)}$ + 4 A
13:12	DPS_5TO4_FINE_DROP (PAGE 0 only)	RW	NVM	Dynamic phase drop threshold, fine adjustment, 5 phases to 4 phases. Set as an offset from peak efficiency point per phase in Amperes. Phases drop when average phase current reaches the stated threshold. $I_{EFF(PEAK)}$ refers to the value selected by DPS_COURSE_TH in MFR_SPECIFIC_15. 00b: Threshold = 4 × $I_{EFF(PEAK)}$ – 2 A 01b: Threshold = 4 × $I_{EFF(PEAK)}$ 10b: Threshold = 4 × $I_{EFF(PEAK)}$ + 2 A 11b: Threshold = 4 × $I_{EFF(PEAK)}$ + 4 A
11:10	DPS_4TO3_FINE_DROP (PAGE 0 only)	RW	NVM	Dynamic phase drop threshold, fine adjustment, 4 phases to 3 phases. Set as an offset from peak efficiency point per phase in Amperes. Phases drop when average phase current reaches the stated threshold. $I_{EFF(PEAK)}$ refers to the value selected by DPS_COURSE_TH in MFR_SPECIFIC_15. 00b: Threshold = 3 × $I_{EFF(PEAK)}$ – 2 A 01b: Threshold = 3 × $I_{EFF(PEAK)}$ 10b: Threshold = 3 × $I_{EFF(PEAK)}$ + 2 A 11b: Threshold = 3 × $I_{EFF(PEAK)}$ + 4 A

Table 2-131. MFR_SPECIFIC_14 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9:8	DPS_3TO2_FINE_DROP	RW	NVM	Dynamic phase drop threshold, fine adjustment, 3 phases to 2 phases. Set as an offset from peak efficiency point per phase in Amperes. Phases drop when average phase current reaches the stated threshold. $I_{EFF(PEAK)}$ refers to the value selected by DPS_COURSE_TH in MFR_SPECIFIC_15. 00b: Threshold = 2 × $I_{EFF(PEAK)}$ – 2 A 01b: Threshold = 2 × $I_{EFF(PEAK)}$ 10b: Threshold = 2 × $I_{EFF(PEAK)}$ + 2 A 11b: Threshold = 2 × $I_{EFF(PEAK)}$ + 4 A
7	DPS_EN	RW	NVM	Enable or Disable Dynamic Phase Shedding 0b: Disable dynamic phase shedding 1b: Enable dynamic phase shedding
6:5	DYN_RAMP_USR	RW	NVM	Dynamic ramp amplitude setting during USR operation. Only applies to USR Level 1. 00b: Equal to the settings in the RAMP bits 01b: 40 mV 10b: 80 mV 11b: 120 mV
4	DYN_RAMP_2PH	RW	NVM	Dynamic ramp amplitude setting during 2 phase operation. 0b: Equal to the settings in the RAMP bits 1b: 120 mV
3	DYN_RAMP_1PH	RW	NVM	Dynamic ramp amplitude setting during 1 phase operation. 0b: Equal to the settings in the RAMP bits 1b: 80 mV
2:0	RAMP	RW	NVM	Ramp amplitude settings. See Table 2-132.

Table 2-132. Ramp Amplitude Settings

RAMP (binary)	Ramp Amplitude Setting (mV)
000b	40
001b	80
010b	120
011b	160
100b	200
101b	235
110b	275
111b	320

2.4.93 (DFh) MFR_SPECIFIC_15

The MFR_SPECIFIC_15 command is used to configure dynamic phase shedding.

The MFR_SPECIFIC_15 command must be accessed through Write Word/Read Word transactions as shown in Section 2.1.2.

MFR_SPECIFIC_15 is a paged register. In order to access MFR_SPECIFIC_15 command for channel A, PAGE must be set to 00h. In order to access the MFR_SPECIFIC_15 register for channel B, PAGE must be set to 01h.

15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
DPS_DCM	DPS_2TO1_FINE_DROP		DPS_5TO6_FINE_ADD (PAGE 0 only)		DPS_4TO5_FINE_ADD (PAGE 0 only)		DPS_3TO4_FINE_ADD (PAGE 0 only)
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
DPS_3TO4_FINE_ADD (PAGE 0 only)	DPS_2TO3_FINE_ADD		DPS_1TO2_FINE_ADD		2TO1_PH_EN	DPS_COURSE_TH	

LEGEND: R/W = Read/Write; R = Read only

MFR_SPECIFIC_15

Table 2-133. MFR_SPECIFIC_15 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	DPS_DCM	RW	NVM	Enable DCM mode during 1 phase operation, when higher order phases are dropped due to dynamic phase shedding. 0b: Disable DCM operation during 1 phase operation 1b: Enable DCM operation during 1 phase operation
14:13	DPS_2TO1_FINE_DROP	RW	NVM	Dynamic phase drop threshold, fine adjustment, 2 phases to 1phase. Set as an offset from peak efficiency point per phase in Amperes. Phases drop when average phase current reaches the stated threshold. $I_{EFF(PEAK)}$ refers to the value selected by DPS_COURSE_TH below. 00b: Threshold = 1× $I_{EFF(PEAK)}$ – 2 A 01b: Threshold = 1 × $I_{EFF(PEAK)}$ 10b: Threshold = 1 × $I_{EFF(PEAK)}$ + 2 A 11b: Threshold = 1 × $I_{EFF(PEAK)}$ + 4 A
12:11	DPS_5TO6_FINE_ADD (PAGE 0 only)	RW	NVM	Dynamic phase add threshold, fine adjustment, 5 phases to 6 phases. Set as an offset from peak efficiency point per phase in Amperes. Phases add when peak phase current reaches the stated threshold. $I_{EFF(PEAK)}$ refers to the value selected by DPS_COURSE_TH below. 00b: Threshold = 5 × $I_{EFF(PEAK)}$ + 6A 01b: Threshold = 5 × $I_{EFF(PEAK)}$ + 8 A 10b: Threshold = 5 × $I_{EFF(PEAK)}$ + 10 A 11b: Threshold = 5 × $I_{EFF(PEAK)}$ + 12 A
10:9	DPS_4TO5_FINE_ADD (PAGE 0 only)	RW	NVM	Dynamic phase add threshold, fine adjustment, 4 phases to 5 phases. Set as an offset from peak efficiency point per phase in Amperes. Phases add when peak phase current reaches the stated threshold. $I_{EFF(PEAK)}$ refers to the value selected by DPS_COURSE_TH below 00b: Threshold = 4 × $I_{EFF(PEAK)}$ + 6A 01b: Threshold = 4 × $I_{EFF(PEAK)}$ + 8 A 10b: Threshold = 4 × $I_{EFF(PEAK)}$ + 10 A 11b: Threshold = 4 × $I_{EFF(PEAK)}$ + 12 A

Table 2-133. MFR_SPECIFIC_15 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8:7	DPS_3TO4_FINE_ADD (PAGE 0 only)	RW	NVM	Dynamic phase add threshold, fine adjustment, 3 phases to 4 phases. Set as an offset from peak efficiency point per phase in Amperes. Phases add when peak phase current reaches the stated threshold. $I_{EFF(PEAK)}$ refers to the value selected by DPS_COURSE_TH below 00b: Threshold = 3 × $I_{EFF(PEAK)}$ + 6A 01b: Threshold = 3 × $I_{EFF(PEAK)}$ + 8 A 10b: Threshold = 3 × $I_{EFF(PEAK)}$ + 10 A 11b: Threshold = 3 × $I_{EFF(PEAK)}$ + 12 A
6:5	DPS_2TO3_FINE_ADD	RW	NVM	Dynamic phase add threshold, fine adjustment, 2 phases to 3 phases. Set as an offset from peak efficiency point per phase in Amperes. Phases add when peak phase current reaches the stated threshold. $I_{EFF(PEAK)}$ refers to the value selected by DPS_COURSE_TH below 00b: Threshold = 2 × $I_{EFF(PEAK)}$ + 6A 01b: Threshold = 2 × $I_{EFF(PEAK)}$ + 8 A 10b: Threshold = 2 × $I_{EFF(PEAK)}$ + 10 A 11b: Threshold = 2 × $I_{EFF(PEAK)}$ + 12 A
5:4	DPS_1TO2_FINE_ADD	RW	NVM	Dynamic phase add threshold, fine adjustment, 1 phase to 2 phases. Set as an offset from peak efficiency point per phase in Amperes. Phases add when peak phase current reaches the stated threshold. $I_{EFF(PEAK)}$ refers to the value selected by DPS_COURSE_TH below 00b: Threshold = 1 × $I_{EFF(PEAK)}$ + 6A 01b: Threshold = 1 × $I_{EFF(PEAK)}$ + 8 A 10b: Threshold = 1 × $I_{EFF(PEAK)}$ + 10 A 11b: Threshold = 1 × $I_{EFF(PEAK)}$ + 12 A
3	2TO1_PH_EN	RW	NVM	Enable phase dropping from 2 phases to 1 phase operation. 0b: Disable phase shedding to 1 phase 1b: Enable phase shedding to 1 phase
2:0	DPS_COURSE_TH	RW	NVM	Sets the peak efficiency point per phase. This is used to determine phase add/drop thresholds. 00b: $I_{EFF(PEAK)}$ = 12 A 01b: $I_{EFF(PEAK)}$ = 14 A 10b: $I_{EFF(PEAK)}$ = 16 A 11b: $I_{EFF(PEAK)}$ = 18 A

2.4.94 (E4h) MFR_SPECIFIC_20

The MFR_SPECIFIC_20 command is used to set the maximum operational phase number, on-the-fly.

The MFR_SPECIFIC_20 command must be accessed through Read Byte/Write Byte transactions as shown in Section 2.1.2.

MFR_SPECIFIC_20 is a paged register. In order to access MFR_SPECIFIC_20 command for channel A, PAGE must be set to 00h. In order to access the MFR_SPECIFIC_20 register for channel B, PAGE must be set to 01h.

7	6	5	4	3	2	1	0
R	R	R	R	R	RW	RW	RW
0	0	0	0	0	PHASE_NUM		

LEGEND: R/W = Read/Write; R = Read only

MFR_SPECIFIC_20

Table 2-134. MFR_SPECIFIC_20 Register Field Descriptions

Bit	Field	Type	Reset	Description
2:0	PHASE_NUM	RW	See below.	Used to program the maximum number of operational phases, on-the-fly, for the active PAGE. 000b: 1 Phase 001b: 2 Phase 010b: 3 Phase 011b: 4 Phase 100b: 5 Phase 101b: 6 Phase

Note that the maximum number of available phases for each channel are configured in hardware. The MFR_SPECIFIC_20 command can be used to further limit the maximum number of available phases via the PMBus interface.

When the TPS53681 is initially powered on, and power conversion has not been enabled for either channel, MFR_SPECIFIC_20 will read 00h. Once either channel has been enabled, it will read whichever is lower, the maximum number of available phases in hardware, or the last programmed value of MFR_SPECIFIC_20.

If the programmed maximum number of phases, via the MFR_SPECIFIC_20 command exceeds the number available, as configured in hardware, the MAX_PH_WARN bit in STATUS_MFR_SPECIFIC register will be set and the PMBus host alerted via the PMB_ALERT pin.

2.4.95 (F0h) MFR_SPECIFIC_32

The MFR_SPECFIC_32 command sets the value of the input power, in watts, that causes a warning that the input power is high. Refer to PIN_OP_WARN_LIMIT for more information.

The MFR_SPECIFIC_32 command must be accessed through Read Word/Write Word transactions as shown in Section 2.1.2.

MFR_SPECIFIC_32 is a shared register. Write transactions to this register will affect both channels, and read transactions to this register will return the same data regardless of the current PAGE.

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
PIN_OP_WARN_LIMIT							

LEGEND: R/W = Read/Write; R = Read only

MFR_SPECIFIC_32

Table 2-135. MFR_SPECIFIC_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PIN_OP_WARN_LIMIT	RW	00E1h	Input overpower warning limit. LSB = 2 W.

2.4.96 (FAh) MFR_SPECIFIC_42

The MFR_SPECIFIC_42 command can be optionally used to set a password for NVM programming. To prevent a hacker from simply sending the password command with all possible passwords, the TPS53681 goes into a special extra-secure state when an incorrect password is received. In this state, all passwords are rejected, even the valid one. The device must be power cycled to clear this state so that another password attempt may be made. When NVM security is enabled, the TPS53681 will not accept writes to any command other than PAGE and PHASE, which are necessary for reading certain parameters.

The MFR_SPECIFIC_42 command must be accessed through Read Word/Write Word transactions as shown in Section 2.1.2.

MFR_SPECIFIC_42 is a shared register. Write transactions to this register will apply to both channels, and read transactions to this register will return the same data regardless of the current PAGE.

15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
NVM_SECURITY_KEY							
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
NVM_SECURITY_KEY							

LEGEND: R/W = Read/Write; R = Read only

MFR_SPECIFIC_42

Table 2-136. MFR_SPECIFIC_42 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	NVM_SECURITY_KEY	RW	NVM	16 bit code for NVM security key.

Enabling NVM Security

When security has not yet been enabled or has been disabled, writing to the MFR_SPECIFIC_42 command sets the new password. After the password is set to any value other than FFFFh, security is enabled. After security has been enabled, a STORE_DEFAULT_ALL command must be issued to store the security setting after the device is reset.

1. Set the NVM password. Write MFR_SPECIFIC_42 to a value other than FFFFh.
2. Issue STORE_DEFAULT_ALL
3. Wait 100ms for the NVM store to complete
4. Power cycle

Disabling NVM Security

To disable NVM security, use the following procedure:

1. Write the password MFR_SPECIFIC_42 to *temporarily* disable NVM security. Once the correct password has been given, NVM security will be disabled, and the device will once again accept write transactions to configuration registers.
2. To *permanently* disable NVM Security, follow steps 3-5.
3. After writing the password to MFR_SPECIFIC_42, again write MFR_SPECIFIC_42 to FFFFh.
4. Issue STORE_DEFAULT_ALL
5. Wait 100ms for the NVM store to complete.

Determining Whether NVM Security is Active

Reads to the MFR_SPECIFIC_42 command will return one of three values:

1. 0000h = NVM Security is Disabled
2. 0001h = NVM Security is Enabled
3. 0002h = MFR_SPECIFIC_42 is locked due to incorrect password entry

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