A10-A, Tiny, DC/DC Module Design Using the TPS40304

This document describes a customized reference design using a tiny non-isolated dc/dc module (TPS40304) to achieve the operation of a high-efficiency buck converter with synchronous rectification (SR). This dc/dc module provides 10 A of current to the main board of a telecommunication system. The module has the capability of operating with an input voltage between 3.0 V and 7.0 V. A thorough analysis of SR converter operation and performance including design guidelines are presented. The experimental results obtained from a 10-A application are provided. This design can be easily modified for similar applications.

Contents

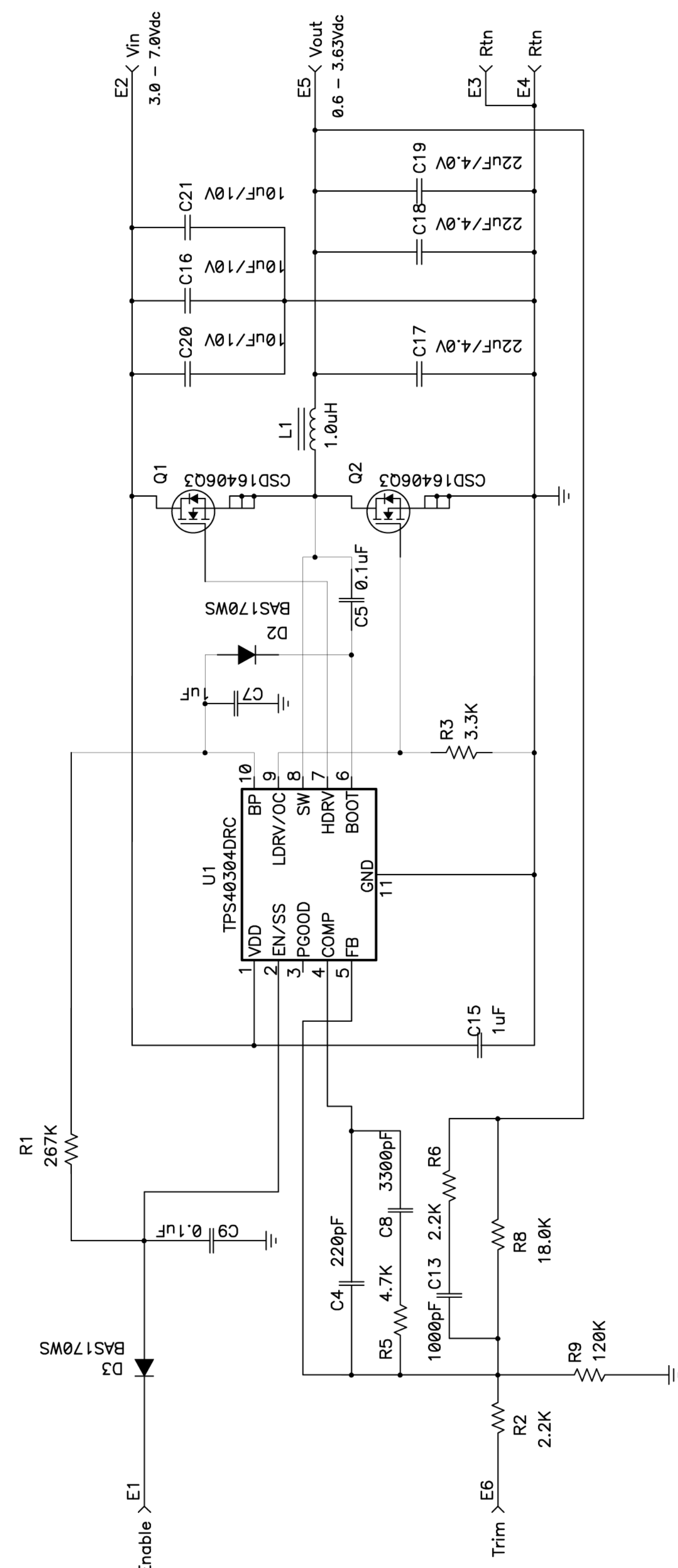
1 Introduction

This wide range and extremely low input dc/dc converter design uses the TPS40304 synchronous rectification controller to step down a 3-V to 7-V input to 0.6 V to 3.63 V output. The TPS40304 is ideal for this application because it offers a variety of user-programmable functions such as soft start, voltage feed forward, and pre-bias output. The complete device operation is specified in the TPS40304 product datasheet.

2 TPS40304 Electrical Performance Specifications

PARAMETER		CONDITIONS	MIN	MAX	UNITS
V_{IN}	Input voltage		3		V
V_{OUT}	Output voltage		0.60	3.63	V
I_{OUT}	Output current		0	10	A
η	Efficiency	V_{IN} = 6 V, V_{OUT} = 3.6 V	94%		
	Load regulation	V_{IN} = 6 V			mV
	Line regulation	I_{OUT} = 10 A			mV
V_{RIPPLE}	Ripple and noise	I_{OUT} = 10 A		60	mV
t_{START}	Start-up time	I_{OUT} = 10 A		15	ms
	Dynamic what?	25%-50%-25%, 50%-75%-50% 1 A/us		120	mV
I_{OCP}	Overcurrent protection value	V_{IN} = 6 V		16	A
t_{DLY}	Hiccup delay time	V_{IN} = 6 V,	40		ms

3 Schematic



NOTE: For reference only; see Table 1: *List of Materials* for specific values.

Figure 1. TPS40304 Reference Design Application Schematic

4 Printed Circuit Board Layout

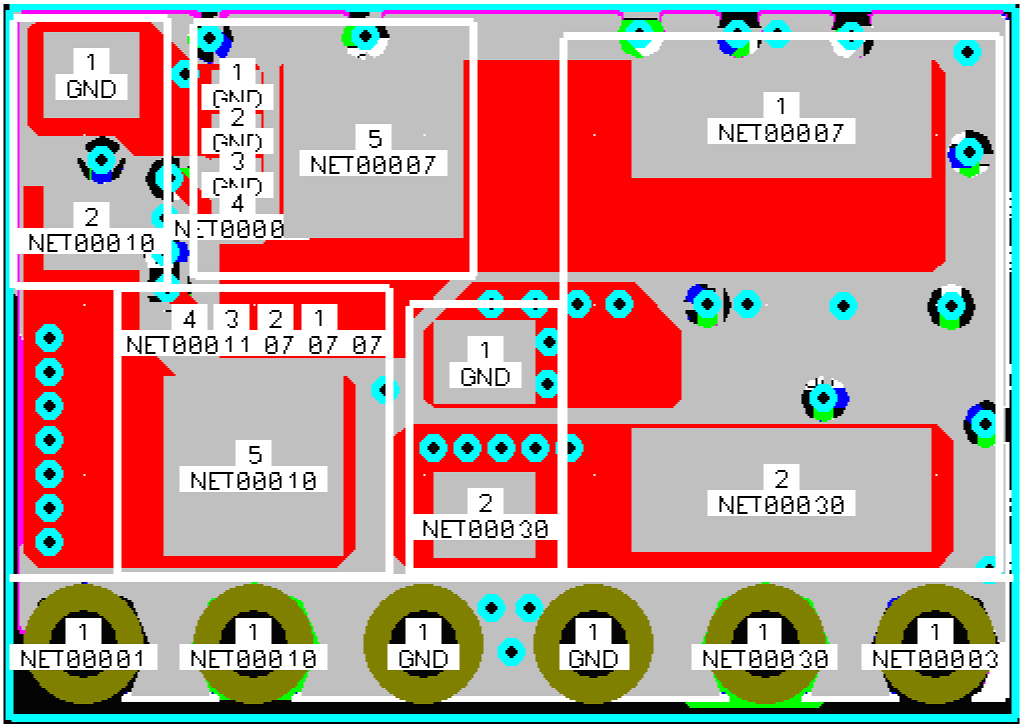


Figure 2. Component Side (15 mm x 10 mm)

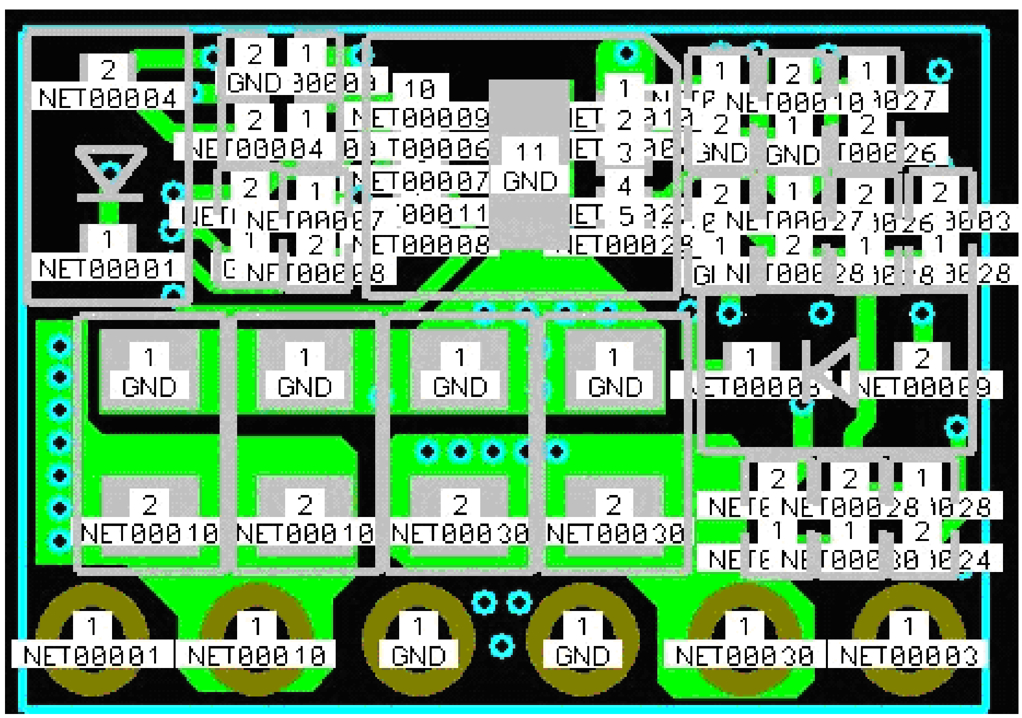


Figure 3. Bottom Side (15 mm x 10 mm)

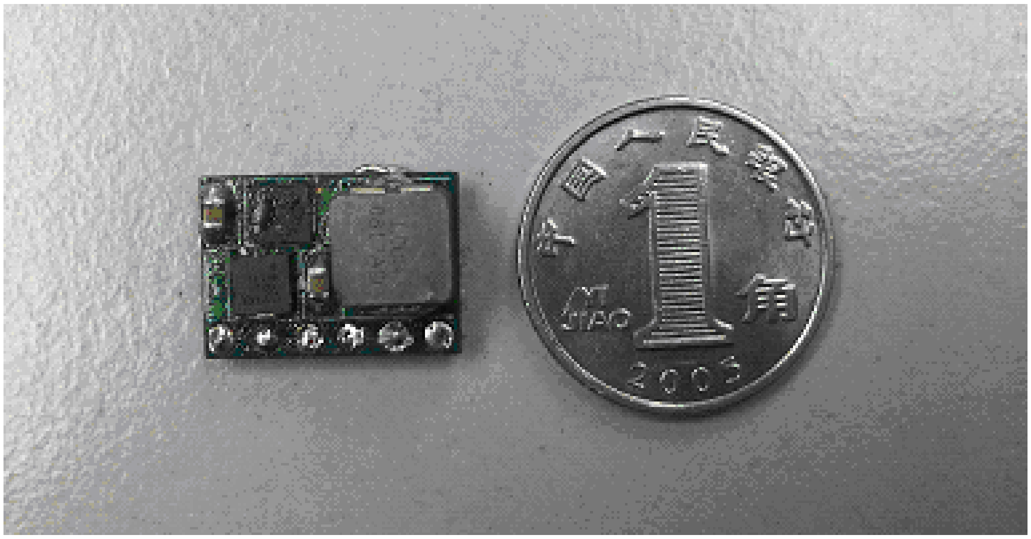


Figure 4. Photo

5 Circuit Description

5.1 Novel Controller : TPS40304

The TPS40304 is a cost-effective synchronous buck controller that operates with an extremely low-input voltage (from 3 V to 20 V) and high-end features such as a frequency spread spectrum (FSS) mode of operation. The TPS40304 also implements a voltage-mode control with input-voltage feed-forward compensation that responds instantly to input voltage change. The operating frequency of the TPS40304 is 600 kHz. This controller offers design flexibility with a variety of user-programmable functions, including soft-start, overcurrent protection (OCP) levels, and pre-bias output.

5.2 Power Stage

5.2.1 Circuit Operation

The power stage is a synchronous rectification buck converter designed to improve the efficiency of a traditional buck converter. The rectification MOSFET (Q1), freewheeling MOSFET (Q2), and primary inductor (L1) combine to create the buck converter. The dead time between Q1 and Q2 is controlled internally by the TPS40304 device. The output voltage can be adjusted by the external trim terminal.

Circuit control and protection can be fully implemented by the TPS40304. The input voltage is fed to the VDD pin of the TPS40304. A 1-µF capacitor is connected to this pin to maintain the high voltage with filtering. The EN/SS pin, which controls the soft-start and converter modes of operation is connected to BP pin with a resistor of 270 kΩ to enable FSS mode. A 0.1-µF capacitor connects the BP pin to the ground for filtering. The external enable terminal connected to the EN/SS pin through a diode can shut down the device when disabling the operation. An additional bootstrap diode (D2) provides an external charging path to bootstrap capacitor C5.

5.2.2 5.2.2 Power Loss Analysis

Power losses exist from three primary source. The first source is the conduction power dissipation that comes from the on-time resistance ($R_{DS(on)}$) of MOSFETs Q1 and Q2, the dc resistance of inductor L1, and the equivalent series resistance (ESR) of C_{IN} and C_{OUT}. At this time the conduction dissipation of the PCB trace is is so small as to be negligible. The second source of power loss is the power dissipation that occurs during the switching process of both switches, which includes the switch power consumption of Q1, and the reverse recover power consumption and conduction consumption of the Q2 diode. The third source of power loss is the gate drive power consumption which is not only in proportion to the frequency of the switch input voltage, but also Qg (the electronic quantity stored in the gate of Q1 and Q2).

Additionally, the power consumption when the output capacitors C_{OSS} of both MOSFET charge and discharge and the power loss on the input and output capacitor ESR also contribute to the power loss. To improve the efficiency of the converter, choose a MOSFET with small on-time resistance and low Qg, and choose low input and output junction capacitance with low ESR in the main inductor which reduces the ripple current to a low level.

To summarize, the sources of power loss are.

- Input voltage: V_{IN}= 5 V
- Output voltage: V_{OUT}= 2.6 V
- Output current: I_{OUT}= 10 A
- f_{SW}= 600 kΩ

The duty cycle, D, is calculated by Equation 1 .

$$D = \frac{2.6}{5} = 0.52 \quad (1)$$

Refer to the TPS40304 and CDS16406q3 data sheets to find the related coefficients, including t_{RISE}, t_{FALL} ,$t_{DLY(on)}$,$t_{DLY(off)}$, Qg, Q_{RR} and V_f.

The high-side MOSFET power dissipation is described in these calculations.

$$P_{COND} = (I_{OUT})^2 \times R_{DS(on)} = 0.52 \times 10^2 \times 0.0065 = 0.338\,W \quad (2)$$

$$P_{SW} == (t_{RISE} + t_{FALL}) \times \left(\frac{(V_{IN} \times I_{OUT} \times f_{SW})}{2} \right) = \left(15n \times \left(\frac{0.84n}{5n} \right) \right) \times 5 \times 10 \times \frac{600k\Omega}{2} = 0.06\,W \quad (3)$$

$$P_{GD} = Q_{g1} \times V_{gs1} \times f_{SW} = 5.8n \times 5.7 \times 600k\Omega = 0.02\,W \quad (4)$$

$$P_{OSS} = C_{OSS1} \times (V_{IN})^2 \times \frac{f_{SW}}{2} = 680p \times 5^2 \times \frac{600k\Omega}{2} = 0.005\,W$$

where

- I_{OUT} is the output current
- V_{gs1} is the voltage between gate and source of Q1
- Q_{g1} is the gate charge
- f_{SW} is the switch frequency
- t_{RISE} is the rise time of the high side drive
- t_{FALL} is the fall time of high side drive
- C_{OSS1} is the output capacity of Q1 (5)

The total power loss of Q1 is shown in Equation 6.

$$P_{TOTAL} = P_{COND} + P_{SW} + P_{GD} + P_{OSS} = 0.423\,W \quad (6)$$

The low-side MOSFET power dissipation is calculated in the following equations.

$$P_{COND} == (1 - D) \times (I_{OUT})^2 \times R_{DS(on)2} = 0.48 \times 10^2 \times 0.0065 = 0.312\,W \quad (7)$$

$$P_{DIODE} = (t_{DLY(on)} + t_{DLY(off)}) \times V_f \times I_{OUT} \times f_{SW} = (7.3n + 8.5n) \times 0.85 \times 10 \times 600k\Omega = 0.081W \quad (8)$$

$$P_{RR} = Q_{RR} \times V_{IN} \times f_{SW} = 18ns \times 5 \times 600kHz = 0.054\,W \quad (9)$$

$$P_{GD} = Q_{g2} \times V_{gs2} \times f_{SW} = 5.8n \times 6.5 \times 600kHz = 0.023\,W \quad (10)$$

$$P_{OSS} = C_{OSS2} \times (V_{IN})^2 \times \left(\frac{f_{SW}}{2}\right) = 680\,pF \times 5^2 \times \frac{600\,kHz}{2} = 0.005\,W$$

where

- $t_{DLY(on)}$ is the conduct time of the diode in Q2 when turn on
- $t_{DLY(off)}$ is the conduct time of the diode in Q2 when turn on
- C_{OSS2} is the output capacity of Q2
- Q_{RR} is reverse recover charge (11)

The total power loss of Q2 is calculated in Equation 12.

$$P_{TOTAL} = P_{COND} + P_{SW} + P_{GD} + P_{OSS} = 0.475\,W \quad (12)$$

The power loss of the input capacitor is calculated in Equation 13.

$$P_{C(IN)} = D \times (1 - D) \times (I_{OUT})^2 \times R_{C(IN)} = 0.52 \times 0.48 \times 10^2 \times 10\,m = 0.25\,W \quad (13)$$

Equation 14 shows the additional power loss that can be attributed to other sources; these losses are negligible compared to the power loss of the MOSFET.

$$P_{OTHER} = P_{COUT} + P_{LR(dc)} + P_{RS} = \frac{1}{12} \times (\Delta I_{LOAD})^2 \times R_{COUT} + (I_{OUT})^2 \times R_{L(dc)} + D^2 \times (I_{OUT})^2 \times R_S$$

where

- R_S is the series resistor of the input trace (14)

Thus, from the calculations, the total power loss can be estimated as 4.5%. Efficiency test results under a variety of conditions are shown in Section 7.4.

5.3 *Output Feedback*

This design uses Type III compensation for the power stage. The output voltage can be regulated with resistors R8 and R9, considering that the voltage of FB pin is equal to the internal reference voltage of the TPS40304, which is 0.6 V. The output voltage can also be changed when R8 and R9 have been selected and by a resistor from external trim terminal to the ground.

6 TPS40304 Reference Design List of Materials

6.1 List of Materials

Table 1 lists the reference design components as configured according to the schematic shown in Figure 1.

Table 1. TPS40304 List of Materials

REFERENCE DESIGNATOR	QTY	VALUE	DESCRIPTION	PART NUMBER	MFR
C4	1	220 pF	Capacitor, ceramic, 16 V, X7R, 15%, 0402	Std	muRata
C5, C9, C15	3	0.1 µF	Capacitor, ceramic, 16 V, X7R, 15%, 0402	Std	muRata
C7	1	1 µF	Capacitor, ceramic, 16 V, X7R, 15%, 0402	Std	muRata
C8	1	3300 pF	Capacitor, ceramic, 16 V, X7R, 15%, 0402	Std	muRata
C13	1	1000 pF	Capacitor, ceramic, 16V, X7R, 15%, 0402	Std	muRata
C16, C20, C21	3	10 µF/10.0 V	Capacitor, ceramic, 6.3V, X5R, 15%, 0805	GRM21BE70G226ME51	muRata
C17, C18, C19	3	22 µF/4.0 V	Capacitor, ceramic, 6.3V, X5R, 15%, 0805	GRM21BE70G226ME51	muRata
D2, D3	2	BAS16	Diode, wwitching, 150 mA, 75 V, 350 mW	BAS16	Vishay-Liteon
E1	1	Enable	Pad, TH, 0.038 inch		Emulation Tech
E2	1	V_{IN}	Pad, TH, 0.038 inch		Emulation Tech
E3	1	Return	Pad, TH, 0.038 inch		Emulation Tech
E4	1	Return	Pad, TH, 0.038 inch		Emulation Tech
E5	1	V_{OUT}	Pad, TH, 0.038 inch		Emulation Tech
E6	1	Trim	Pad, TH, 0.038 inch		
L1	1	1.0 µH	Industor, power, 8.6 mΩ, 12A,	IHLP2525EZ-1R5	Vishay
Q1, Q2	2	CSD16406Q3	MOSFET, N-channel, 25 V, 60 A, 5.9 mΩ	CSD16406Q3	TI
R1	1	270 kΩ	Resistor, chip, 1/16W, 1%, 0402	Std	Std
R2	1	2.2 kΩ	Resistor, chip, 1/16W, 1%, 0402	Std	Std
R3	1	3.3 kΩ	Resistor, chip, 1/16W, 1%, 0402	Std	Std
R5	1	4.7 kΩ	Resistor, chip, 1/16W, 1%, 0402	Std	Std
R6	1	2.2 kΩ	Resistor, chip, 1/16W, 1%, 0402	Std	Std
R8	1	18.0 kΩ	Resistor, chip, 1/16W, 1%, 0402	Std	Std
R9	1	120 kΩ	Resistor, chip, 1/16W, 1%, 0402	Std	Std
U1	1	QFN-10P	Low-voltage dc/dc synchronous buck controller,	TPS40304DBC	TI

7 Electrical Performance

7.1 Module Startup, V_{OUT} = 2.6 V

Startup waveforms for V_{OUT} = 2.6 V are shown in Figure 5 through Figure 8.

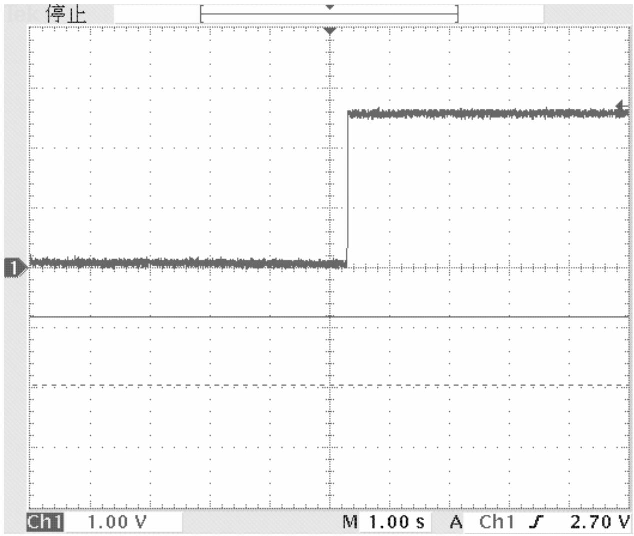


Figure 5. V_{IN} = 3 V, I_{OUT} = 0 A

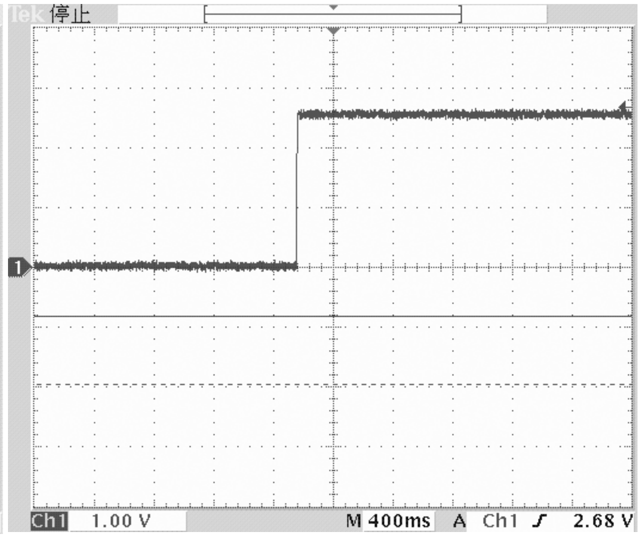


Figure 6. V_{IN} = 3 V, I_{OUT} = 4 A

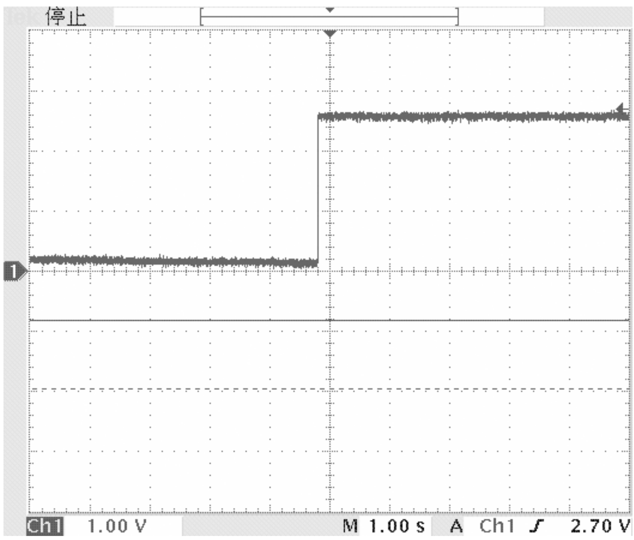


Figure 7. V_{IN} = 7 V, I_{OUT} = 0 A

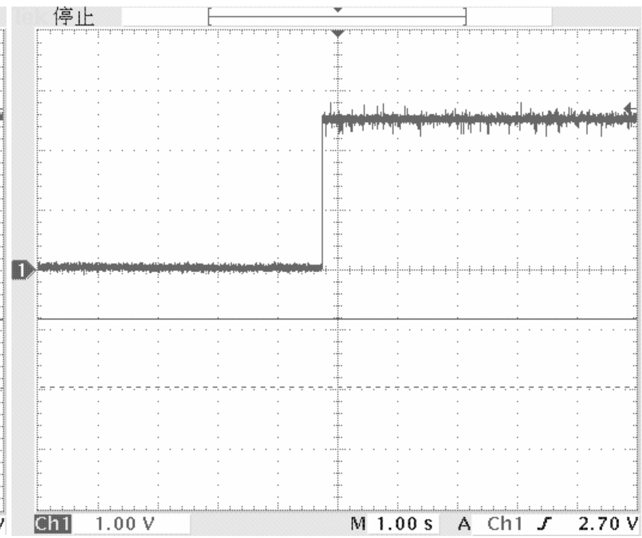


Figure 8. V_{IN} = 7 V, I_{OUT} = 10 A

7.2 Module Startup, V_{OUT} = 0.6 V

Startup waveforms for V_{OUT} = 0.6 V are shown in Figure 9 through Figure 10.

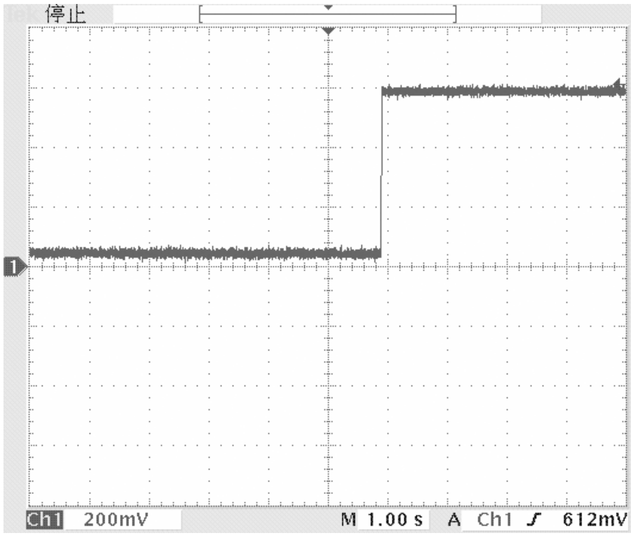


Figure 9. V_{IN} = 3 V, I_{OUT} = 0 A

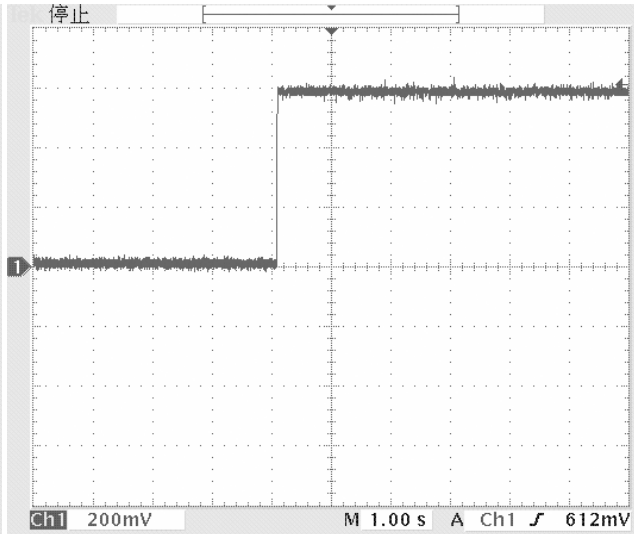


Figure 10. V_{IN} = 7 V, I_{OUT} = 0 A

7.3 Module Startup, V_{OUT} = 3.6 V

Startup waveforms for V_{OUT} = 3.6 V are shown in Figure 11 through Figure 14.

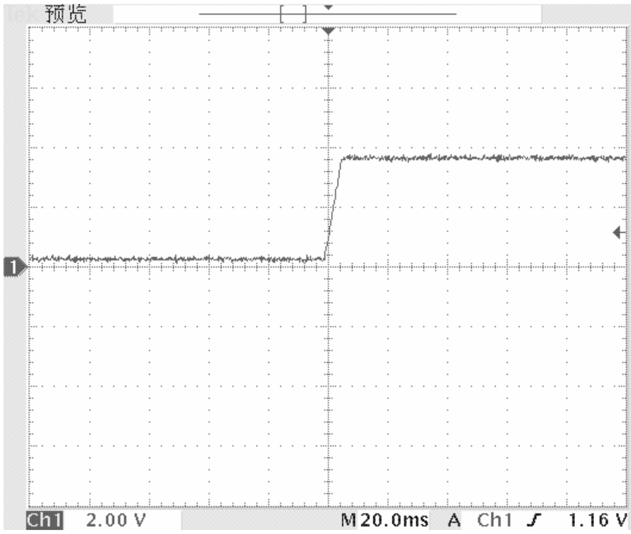


Figure 11. V_{IN} = 6 V, I_{OUT} = 10 A

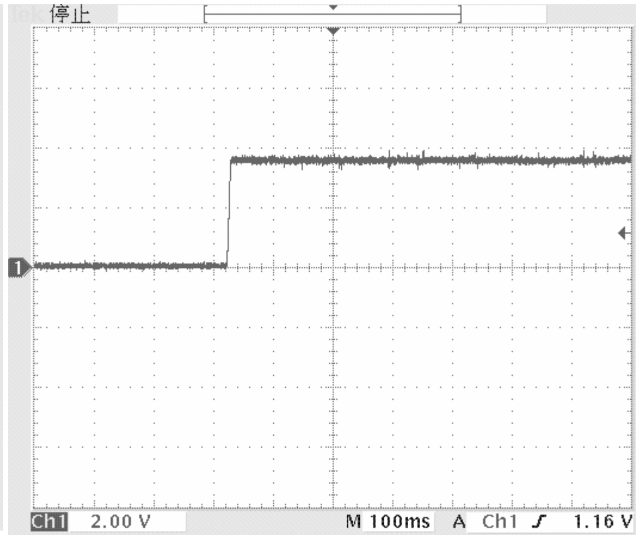


Figure 12. V_{IN} = 7 V, I_{OUT} = 0 A

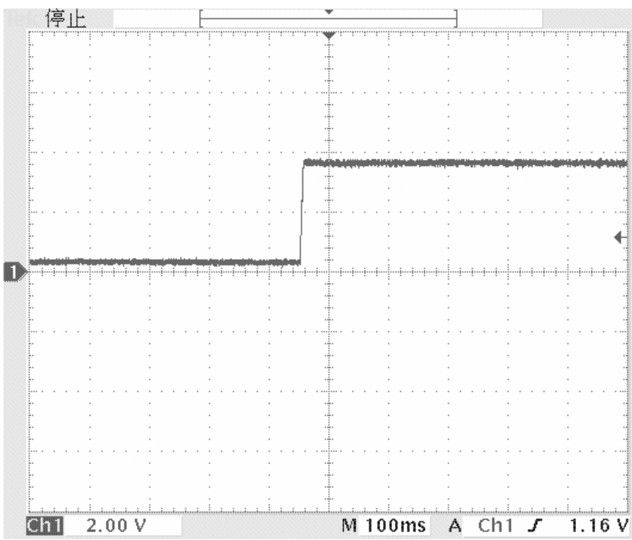


Figure 13. V_{IN} = 7 V, I_{OUT} = 0 A

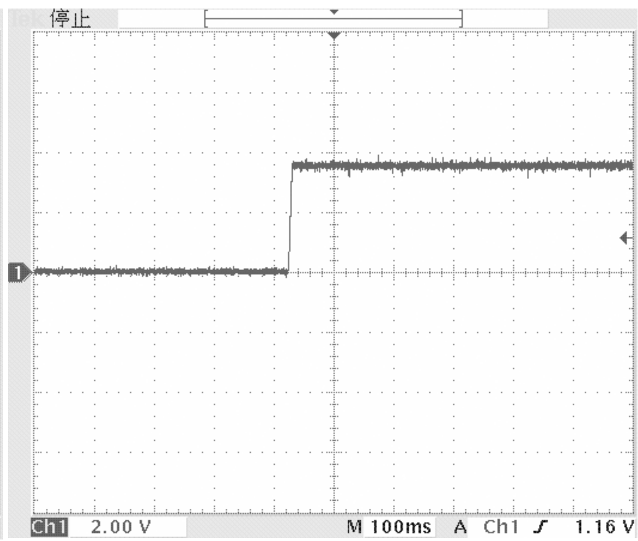


Figure 14. V_{IN} = 7 V, I_{OUT} = 10 A

7.4 Operating Waveforms

Figure 15 shows the circuit efficiency, and Figure 16 illustrates the line regulation performance.

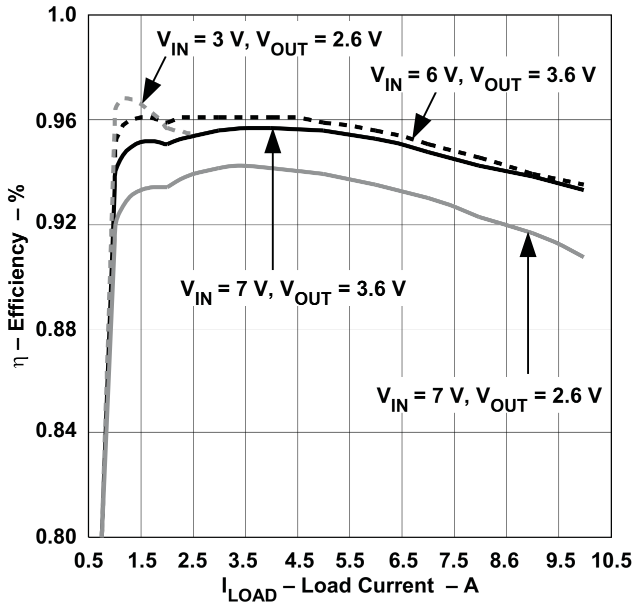


Figure 15. Efficiency vs. Load Current

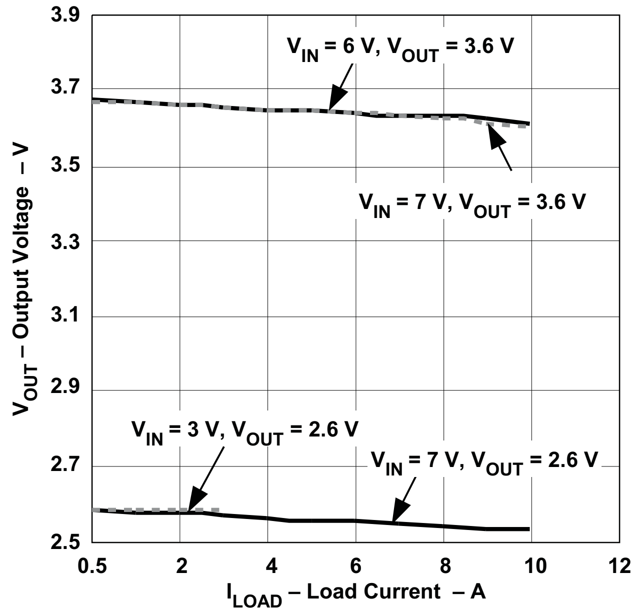


Figure 16. Load Regulation

7.5 Output Ripple, V_{OUT} = 2.6

The output ripple waveforms with a 2.6-V output voltage are show in Figure 17 through Figure 20.

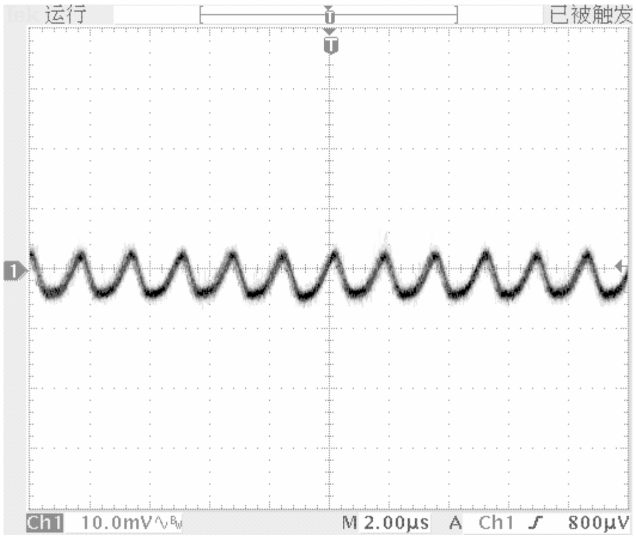


Figure 17. V_{IN} = 3 V, I_{OUT} = 0 A

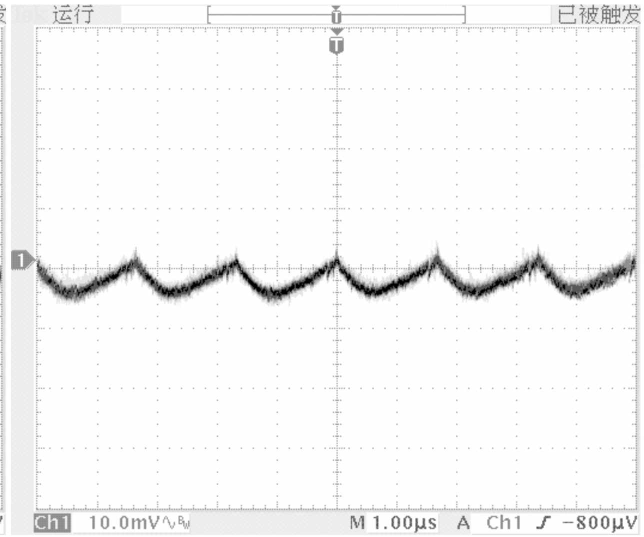


Figure 18. V_{IN} = 3 V, I_{OUT} = 3.5 A

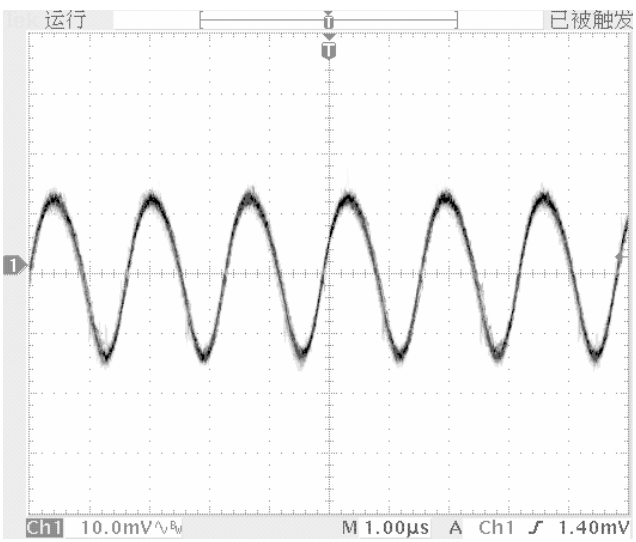


Figure 19. V_{IN} = 7 V, I_{OUT} = 0 A

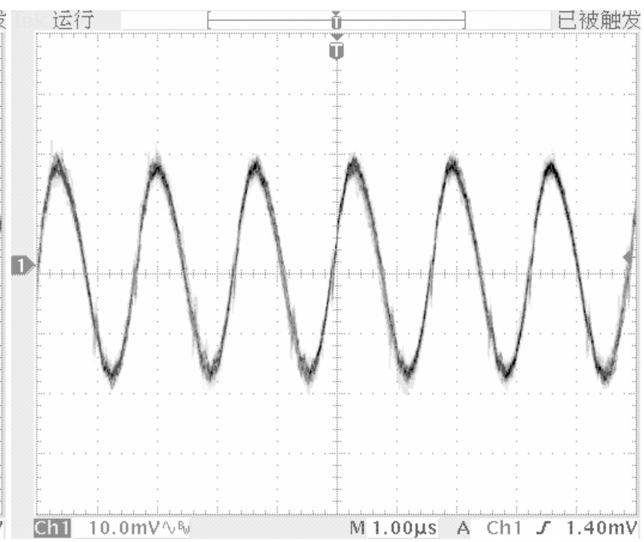


Figure 20. V_{IN} = 7 V, I_{OUT} = 10 A

7.6 Output Ripple, V_{OUT} = 0.6

The output ripple waveforms with a 0.6-V output voltage is show in Figure 21 and Figure 22.

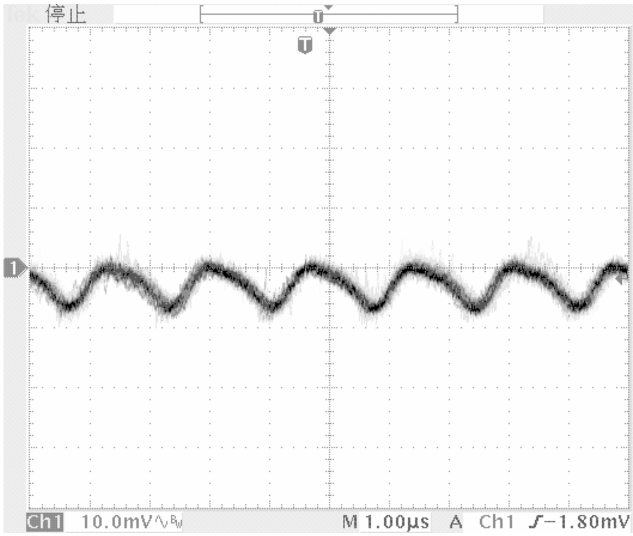


Figure 21. V_{IN} = 3 V, I_{OUT} = 0 A

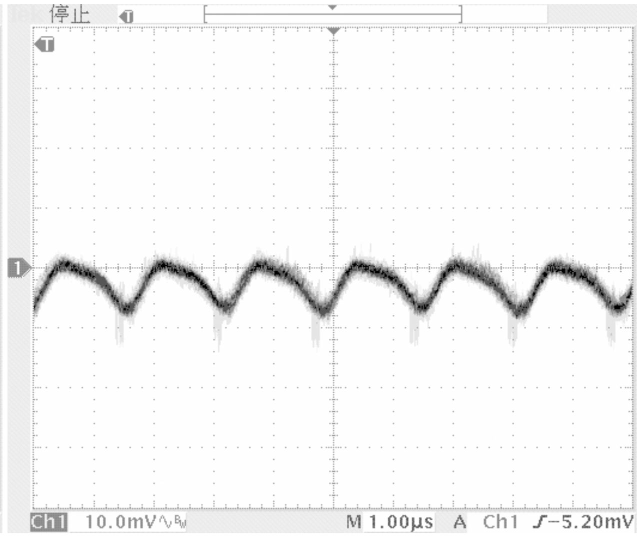


Figure 22. V_{IN} = 7 V, I_{OUT} = 0 A

7.7 Output Ripple, V_{OUT} = 3.6

The output ripple voltage with a 3.6-V output voltage is show in Figure 23 and Figure 26.

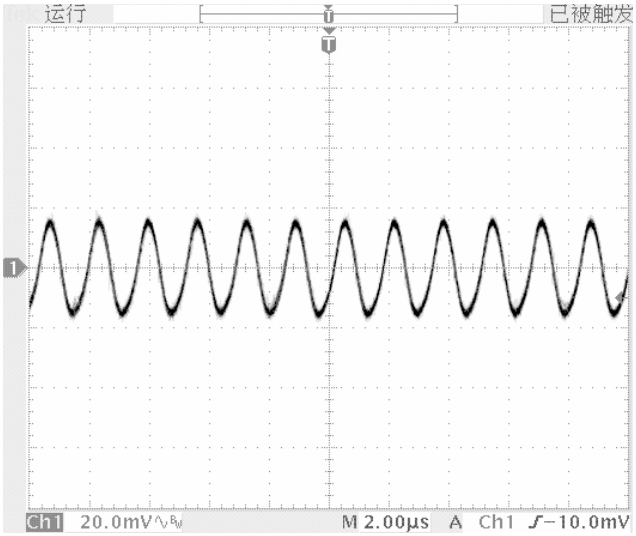


Figure 23. V_{IN} = 6 V, I_{OUT} = 0 A

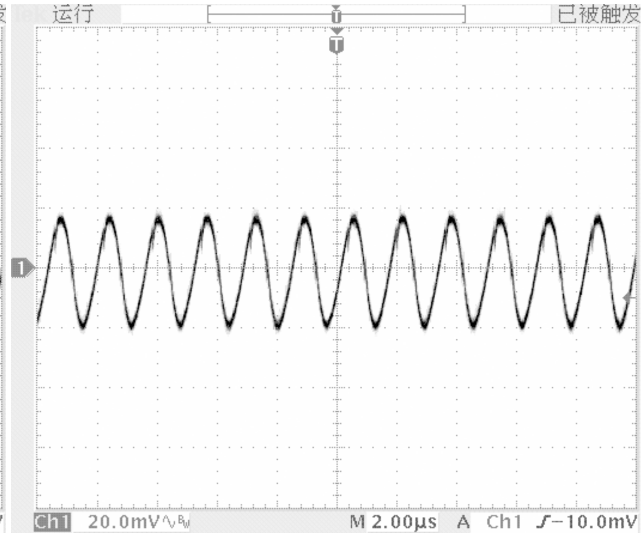


Figure 24. V_{IN} = 6 V, I_{OUT} = 10 A

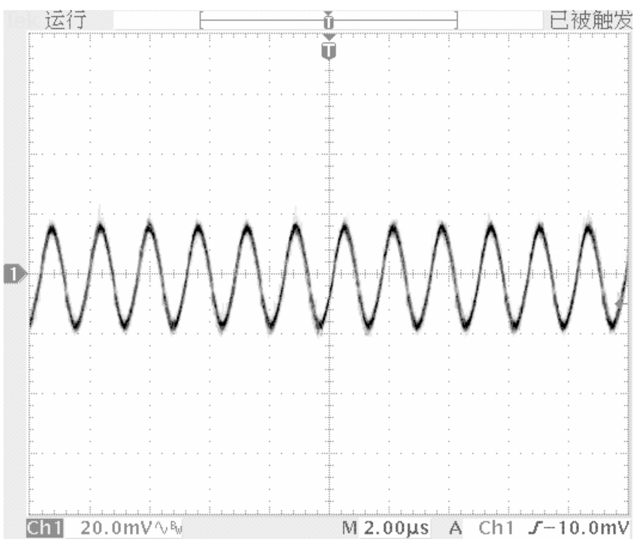


Figure 25. V_{IN} = 7 V, I_{OUT} = 0 A

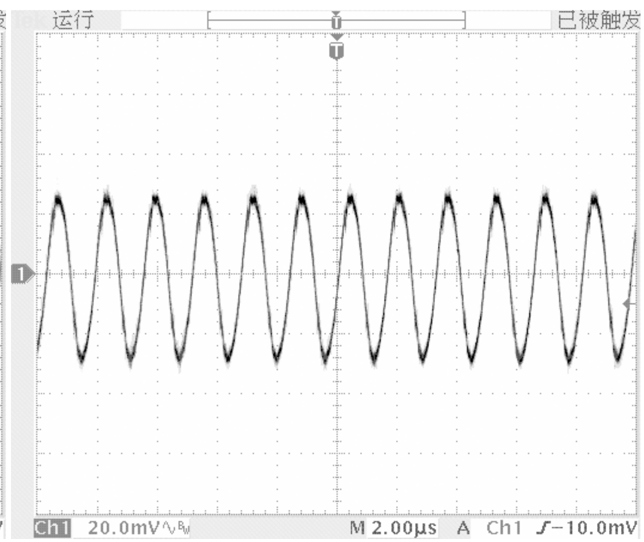


Figure 26. V_{IN} = 7 V, I_{OUT} = 10 A

7.8 Load Transients, V_{OUT} = 2.6 V

Figure 27 and Figure 28 show the load transient with output voltage of 2.6 V. Channel 1: V_{OUT} (200 mV/div). Channel 3: I_{OUT} (2 A/div) In Figure 27, the output response is 0.5~2.5 (96mA/µs). In Figure 28 the output response is 2.5A~7.5A load step (96 mA/µs) .

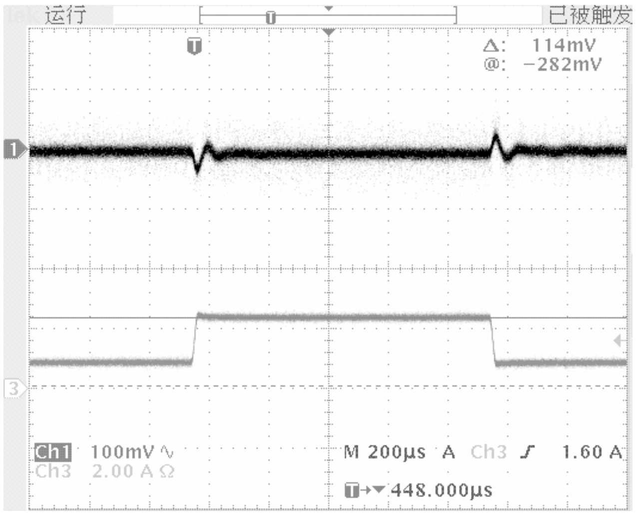


Figure 27. V_{IN} = 3 V

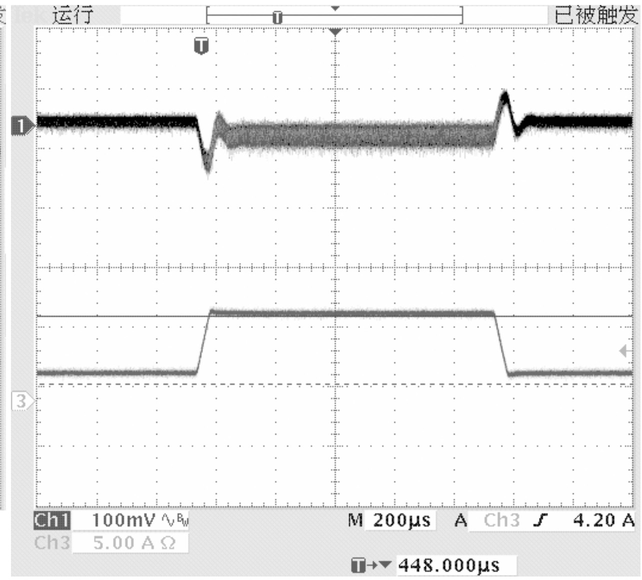


Figure 28. V_{IN} = 7 V

7.9 Load Transients, V_{OUT} = 3.6 V

Figure 29 and Figure 30 show load transients with output voltage of 3.6 V and the output response a 2.5A~7.5A load step (96 mA/µs) . Channel 1: V_{OUT} (200 mV/div). Channel 3: I_{OUT} (10 A/div)

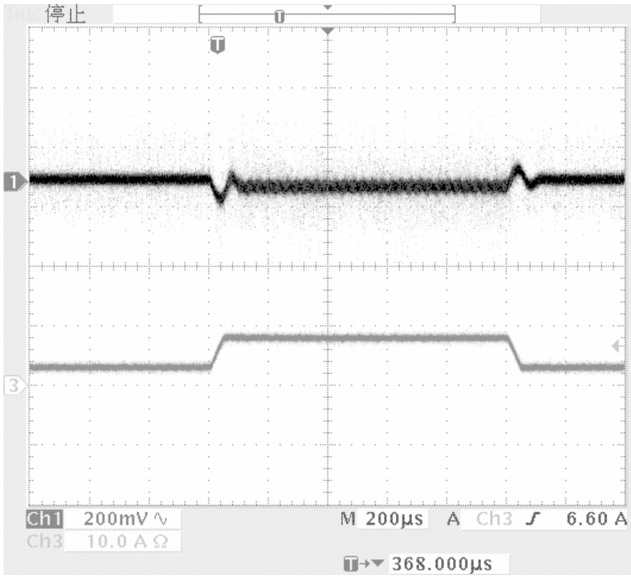


Figure 29. V_{IN} = 6 V

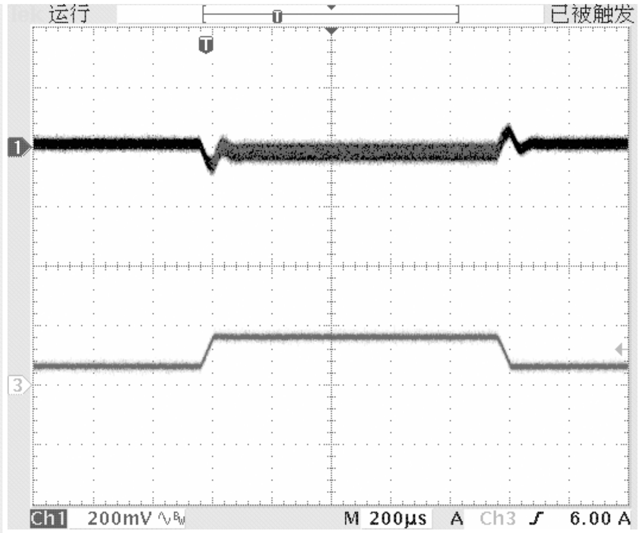


Figure 30. V_{IN} = 7 V

7.10 *Switch Node Waveforms, V_{OUT} = 2.6 V*

Figure 31 through Figure 34 show the switch node waveforms with the output voltage is set 2.6.

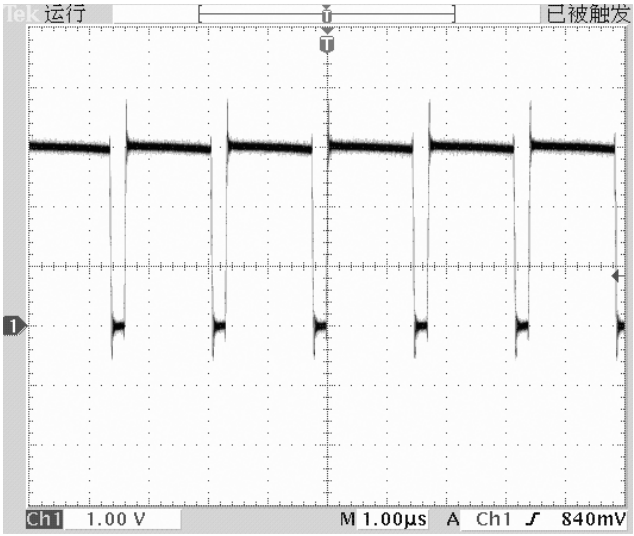


Figure 31. V_{IN} = 3 V, I_{OUT} = 10 A

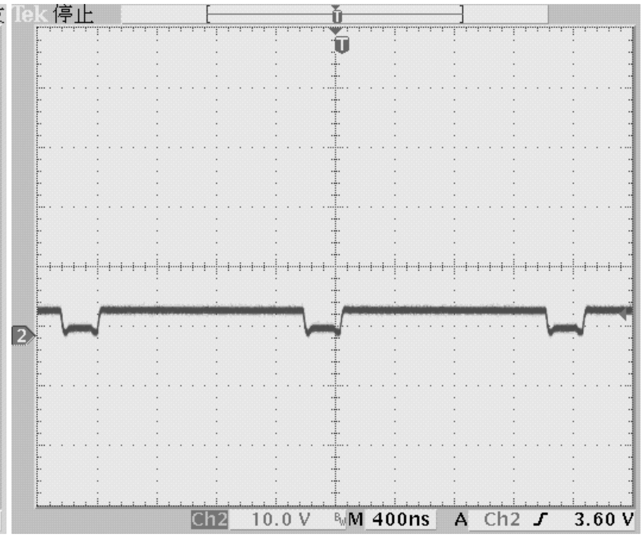


Figure 32. V_{IN} = 3 V, I_{OUT} = 4 A

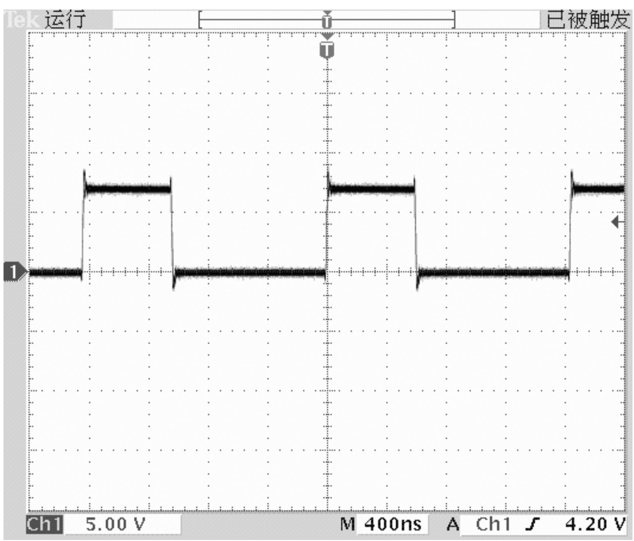


Figure 33. V_{IN} = 7 V, I_{OUT} = 0 A

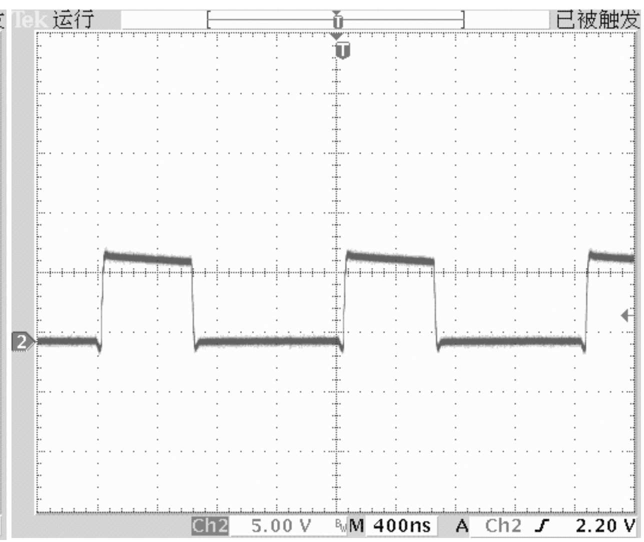


Figure 34. V_{IN} = 7 V, I_{OUT} = 10 A

7.11 Switch Node Waveforms, V_{OUT} = 3.6 V

Figure 35 through Figure 38 show the switch node waveforms with the output voltage set to 3.6 V.

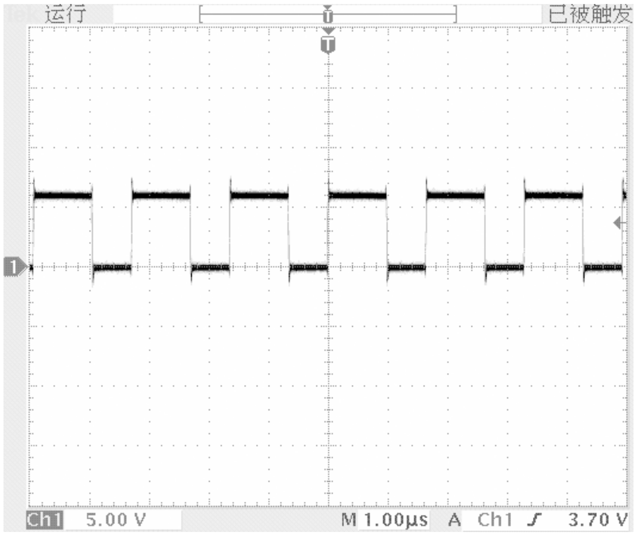


Figure 35. V_{IN} = 6 V, I_{OUT} = 0 A

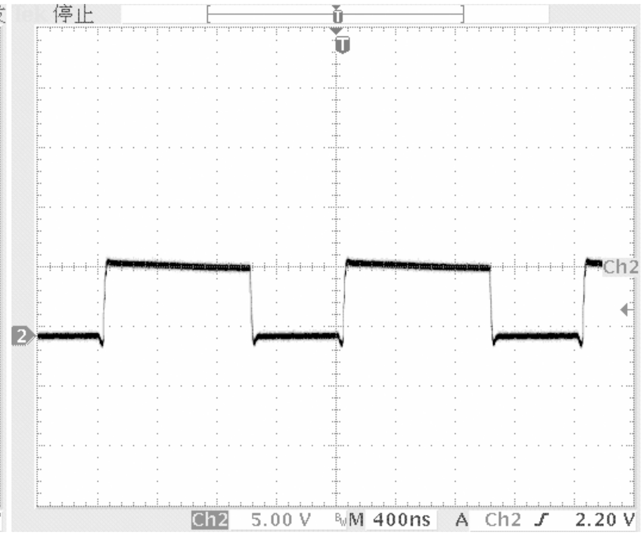


Figure 36. V_{IN} = 6 V, I_{OUT} = 10 A

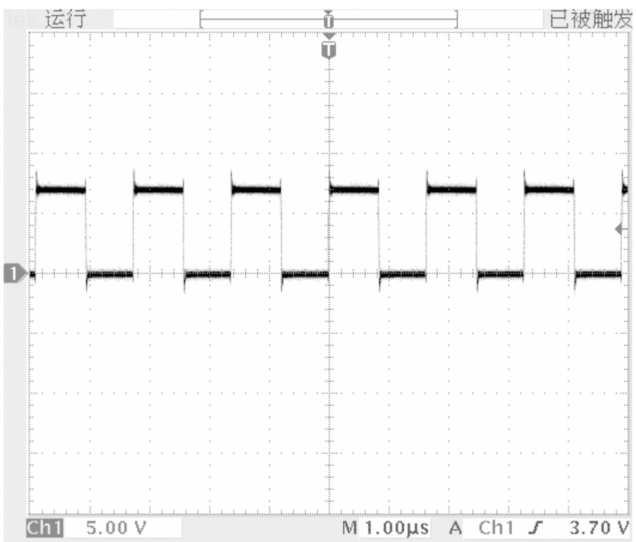


Figure 37. V_{IN} = 7 V, I_{OUT} = 0 A

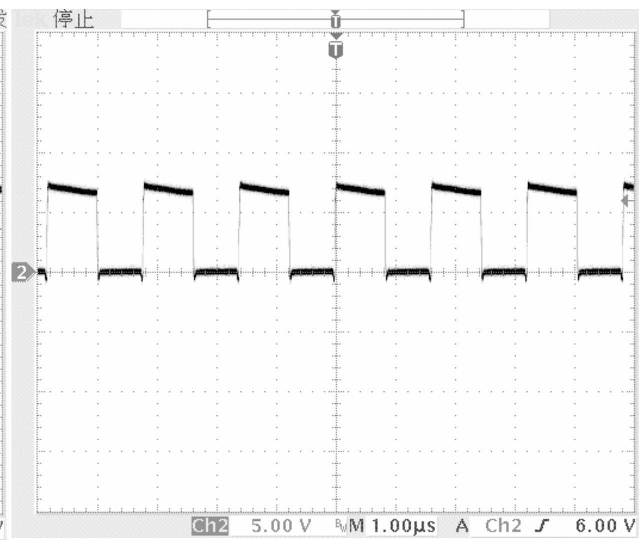


Figure 38. V_{IN} = 7 V, I_{OUT} = 10 A

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 8 V to 14 V and the output voltage range of 0.6 V to 3.3 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 50°C. The EVM is designed to operate properly with certain components above 50°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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