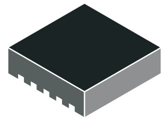


HIGH PERFORMANCE, SINGLE SYNCHRONOUS STEP-DOWN CONTROLLER FOR NOTEBOOK POWER SUPPLY

Check for Samples: TPS51218

FEATURES

- **Wide Input Voltage Range: 3 V to 28 V**
- **Output Voltage Range: 0.7 V to 2.6 V**
- **Wide Output Load Range: 0 to 20A+**
- **Built-in 0.5% 0.7 V Reference**
- **D-CAP™ Mode with 100-ns Load Step Response**
- **Adaptive On Time Control Architecture With 4 Selectable Frequency Setting**
- **4700 ppm/°C $R_{DS(on)}$ Current Sensing**
- **Internal 1-ms Voltage Servo Softstart**
- **Pre-Charged Start-up Capability**
- **Built in Output Discharge**
- **Power Good Output**
- **Integrated Boost Switch**
- **Built-in OVP/UVP/OCP**
- **Thermal Shutdown (Non-latch)**
- **SON-10 (DSC) Package**

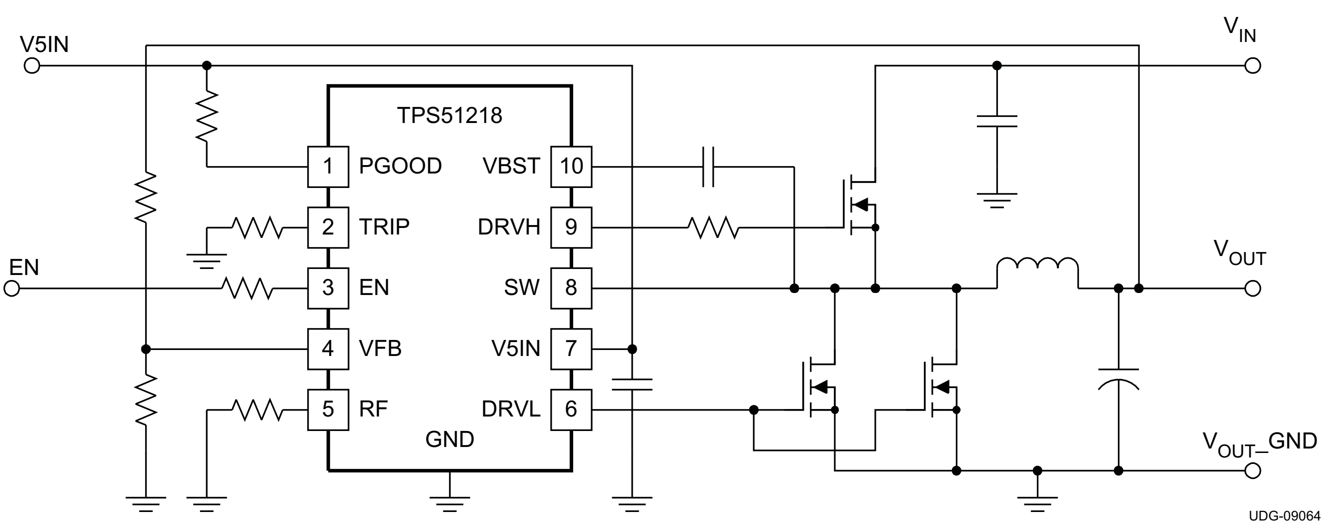
APPLICATIONS

- **Notebook Computers**
- **I/O Supplies**
- **System Power Supplies**

DESCRIPTION

The TPS51218 is a small-sized single buck controller with adaptive on-time D-CAP™ mode. The device is suitable for low output voltage, high current, PC system power rail and similar point-of-load (POL) power supply in digital consumer products. A small package with minimal pin-count saves space on the PCB, while a dedicated EN pin and pre-set frequency selections minimize design effort required for new designs. The skip-mode at light load condition, strong gate drivers and low-side FET $R_{DS(on)}$ current sensing supports low-loss and high efficiency, over a broad load range. The conversion input voltage which is the high-side FET drain voltage ranges from 3 V to 28 V and the output voltage ranges from 0.7 V to 2.6 V. The device requires an external 5-V supply. The TPS51218 is available in a 10-pin SON package specified from –40°C to 85°C.

TYPICAL APPLICATION CIRCUIT



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

D-CAP is a trademark of Texas Instruments.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

T_A	PACKAGE	ORDERING DEVICE NUMBER	PINS	OUTPUT SUPPLY	MINIMUM QUANTITY
–40°C to 85°C	Plastic SON PowerPAD	TPS51218DSCR	10	Tape and reel	3000
		TPS51218DSCT	10	Mini reel	250

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
Input voltage range(2)	VBST	–0.3 to 37	V
	VBST(3)	–0.3 to 7	
	SW	–5 to 30	
	V5IN, EN, TRIP, VFB, RF	–0.3 to 7	
Output voltage range(2)	DRVH	–5 to 37	V
	DRVH(3)	–0.3 to 7	
	DRVH(3), pulse width < 20 ns	–2.5 to 7	
	DRVL	–0.5 to 7	
	DRVL, pulse width < 20 ns	–2.5 to 7	
	PGOOD	–0.3 to 7	
T_J	Junction temperature range	150	°C
T_{STG}	Storage temperature range	–55 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal unless otherwise noted.
(3) Voltage values are with respect to the SW terminal.

DISSIPATION RATINGS

2-oz. trace and copper pad with solder.

PACKAGE	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C POWER RATING
10-pin DSC(1)	1.54 W	15 mW/°C	0.62 W

(1) Enhanced thermal conductance by thermal vias is used beneath thermal pad as shown in Land Pattern information.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
Supply voltage	V5IN	4.5		6.5	V
Input voltage range	VBST	–0.1		34.5	V
	SW	–1		28	
	SW(1)	–4		28	
	VBST(2)	–0.1		6.5	
	EN, TRIP, VFB, RF	–0.1		6.5	
Output voltage range	DRVH	–1		34.5	V
	DRVH(1)	–4		34.5	
	DRVH(2)	–0.1		6.5	
	DRVL	–0.3		6.5	
	PGOOD	–0.1		6.5	
T_A	Operating free-air temperature	–40		85	°C

(1) This voltage should be applied for less than 30% of the repetitive period.
(2) Voltage values are with respect to the SW terminal.

ELECTRICAL CHARACTERISTICS

over recommended free-air temperature range, V5IN=5V. (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{V5IN}	V5IN supply current	V5IN current, T_A = 25°C, No Load, V_{EN} = 5 V, V_{VFB} = 0.735 V		320	500	µA
$I_{V5INSDN}$	V5IN shutdown current	V5IN current, T_A = 25°C, No Load, V_{EN} = 0 V			1	µA
INTERNAL REFERENCE VOLTAGE						
V_{VFB}	VFB regulation voltage	VFB voltage, CCM condition[1]		0.7000		V
		T_A = 25°C, skip mode	0.7005	0.7040	0.7075	V
		T_A = 0°C to 85°C, skip mode	0.6984	0.7040	0.7096	
		T_A = –40°C to 85°C, skip mode	0.6970	0.7040	0.7110	
I_{VFB}	VFB input current	V_{VFB} = 0.735 V, T_A = 25°C, skip mode		0.01	0.2	µA
OUTPUT DISCHARGE						
I_{Dischg}	Output discharge current from SW pin	V_{EN} = 0 V, V_{SW} = 0.5 V	5	13		mA
OUTPUT DRIVERS						
R_{DRVH}	DRVH resistance	Source, I_{DRVH} = –50 mA		1.5	3	Ω
		Sink, I_{DRVH} = 50 mA		0.7	1.8	
R_{DRVL}	DRVL resistance	Source, I_{DRVL} = –50 mA		1.0	2.2	
		Sink, I_{DRVL} = 50 mA		0.5	1.2	
t_D	Dead time	DRVH-off to DRVL-on	7	17	30	ns
		DRVL-off to DRVH-on	10	22	35	
BOOT STRAP SWITCH						
V_{FBST}	Forward voltage	$V_{V5IN-VBST}$, I_F = 10 mA, T_A = 25°C		0.1	0.2	V
I_{VBSTLK}	VBST leakage current	V_{VBST} = 34.5 V, V_{SW} = 28 V, T_A = 25°C		0.01	1.5	µA
DUTY AND FREQUENCY CONTROL						
$t_{OFF(min)}$	Minimum off-time	T_A = 25°C	150	260	400	ns
$t_{ON(min)}$	Minimum on-time	V_{IN} = 28 V, V_{OUT} = 0.7 V, R_{RF} = 39kΩ, T_A = 25°C[1]		79		
SOFTSTART						
t_{ss}	Internal SS time	From V_{EN} = high to V_{OUT} = 95%		1		ms
POWERGOOD						
V_{THPG}	PG threshold	PG in from lower	92.5%	95%	97.5%	
		PG in from higher	107.5%	110%	112.5%	
		PG hysteresis	2.5%	5%	7.5%	
I_{PGMAX}	PG sink current	V_{PGOOD} = 0.5 V	3	6		mA
t_{PGDEL}	PG delay	Delay for PG in	0.8	1	1.2	ms
LOGIC THRESHOLD AND SETTING CONDITIONS						
V_{EN}	EN voltage threshold	Enable	1.8			V
		Disable			0.5	
I_{EN}	EN input current	V_{EN} = 5V			1.0	µA
f_{SW}	Switching frequency	R_{RF} = 470 kΩ, T_A = 25°C[2]	266	290	314	kHz
		R_{RF} = 200 kΩ, T_A = 25°C[2]	312	340	368	
		R_{RF} = 100 kΩ, T_A = 25°C[2]	349	380	411	
		R_{RF} = 39 kΩ, T_A = 25°C[2]	395	430	465	
V_{RF}	CCM setting voltage	CCM	1.8			V
		Auto-skip			0.5	

(1) Ensured by design. Not production tested.
(2) Not production tested. Test condition is V_{IN}= 8 V, V_{OUT}= 1.1 V, I_{OUT} = 10 A using application circuit shown in Figure 21.

ELECTRICAL CHARACTERISTICS (continued)

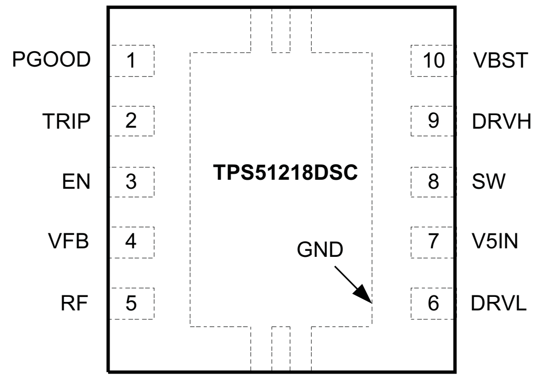
over recommended free-air temperature range, V5IN=5V. (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PROTECTION: CURRENT SENSE						
I_{TRIP}	TRIP source current	V_{TRIP} = 1V, T_A = 25°C	9	10	11	µA
TC_{ITRIP}	TRIP current temperature coeffficient	On the basis of 25°C		4700		ppm/°C
V_{TRIP}	Current limit threshold setting range	$V_{TRIP-GND}$ Voltage	0.2		3	V
V_{OCL}	Current limit threshold	V_{TRIP} = 3.0 V	355	375	395	mV
		V_{TRIP} = 1.6 V	185	200	215	
		V_{TRIP} = 0.2 V	17	25	33	
V_{OCLN}	Negative current limit threshold	V_{TRIP} = 3.0 V	–395	–375	–355	mV
		V_{TRIP} = 1.6 V	–215	–200	–185	
		V_{TRIP} = 0.2 V	–33	–25	–17	
V_{AZCADJ}	Adaptive zero cross adjustable range	Positive	3	15		mV
		Negative		–15	–3	
PROTECTION: UVP AND OVP						
V_{OVP}	OVP trip threshold	OVP detect	115%	120%	125%	
t_{OVPDEL}	OVP propagation delay time	50-mV overdrive		1		µs
V_{UVP}	Output UVP trip threshold	UVP detect	65%	70%	75%	
t_{UVPDEL}	Output UVP propagation delay time		0.8	1	1.2	ms
t_{UVPEN}	Output UVP enable delay time	From Enable to UVP workable	1.0	1.2	1.4	ms
UVLO						
V_{UVV5IN}	V5IN UVLO threshold	Wake up	4.20	4.38	4.50	V
		Shutdown	3.7	3.93	4.1	
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold	Shutdown temperature (3)		145		°C
		Hysteresis (3)		10		

(3) Ensured by design. Not production tested.

DEVICE INFORMATION

DSC PACKAGE
(TOP VIEW)

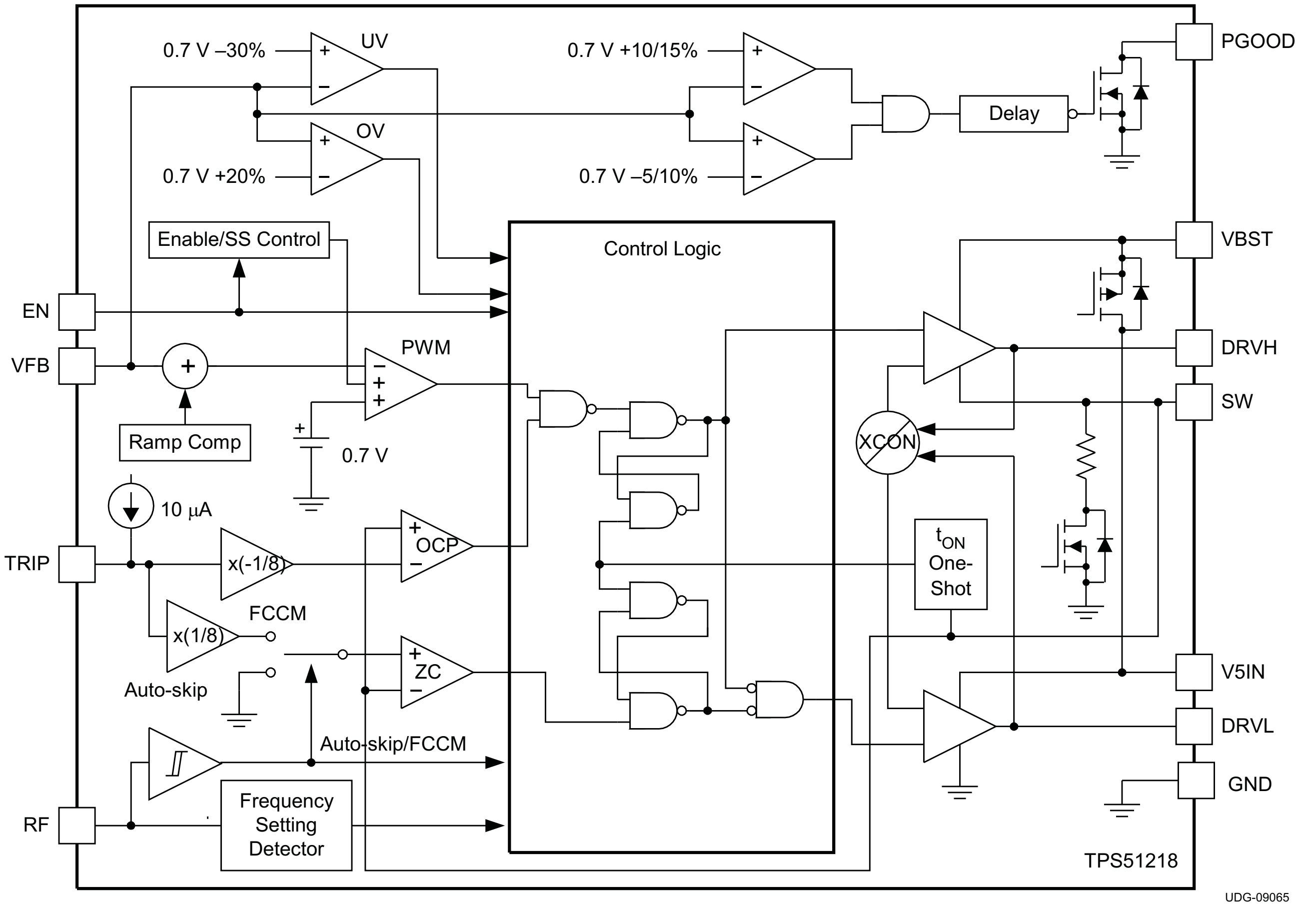


Thermal pad is used as an active terminal of GND.

PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
DRVH	9	O	High-side MOSFET driver output. The SW node referenced floating driver. The gate drive voltage is defined by the voltage across VBST to SW node bootstrap flying capacitor
DRVL	6	O	Synchronous MOSFET driver output. The GND referenced driver. The gate drive voltage is defined by V5IN voltage.
EN	3	I	SMPS enable pin. Short to GND to disable the device.
GND	Thermal Pad	I	Ground
PGOOD	1	O	Power Good window comparator open drain output. Pull up with resistor to 5 V or appropriate signal voltage. Continuous current capability is 1 mA. PGOOD goes high 1 ms after VFB becomes within specified limits. Power bad, or the terminal goes low, after a 2- µs delay.
RF	5	I	Switching frequency selection. Connect a resistance to select switching frequency as shown in Table 1. The switching frequency is detected and stored into internal registers during startup. This pin also controls Auto-skip or forced CCM selection. Pull down to GND with resistor : Auto-Skip Connect to PGOOD with resistor: forced CCM after PGOOD becomes high.
SW	8	I	Switch node. A high-side MOSFET gate drive return. Also used for on time generation and output discharge.
TRIP	2	I	OCL detection threshold setting pin. 10 µA at room temperature, 4700 ppm/°C current is sourced and set the OCL trip voltage as follows. $V_{OCL} = \frac{V_{TRIP}}{8}$ $(0.2\ V \le V_{TRIP} \le 3\ V)$
V5IN	7	I	5 V +30%/–10% power supply input.
VBST	10	I	Supply input for high-side MOSFET driver (bootstrap terminal). Connect a flying capacitor from this pin to the SW pin. Internally connected to V5IN via bootstrap MOSFET switch.
VFB	4	I	SMPS feedback input. Connect the feedback resistor divider.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

V5IN SUPPLY CURRENT
vs
JUNCTION TEMPERATURE

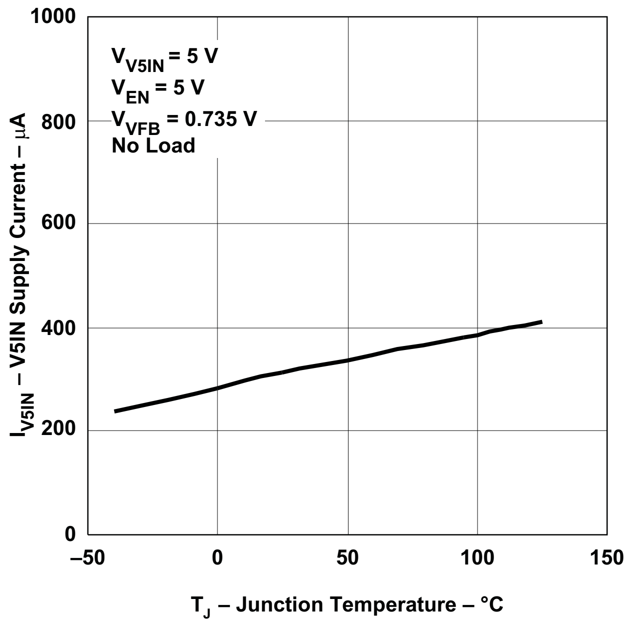


Figure 1.

V5IN SHUTDOWN CURRENT
vs
JUNCTION TEMPERATURE

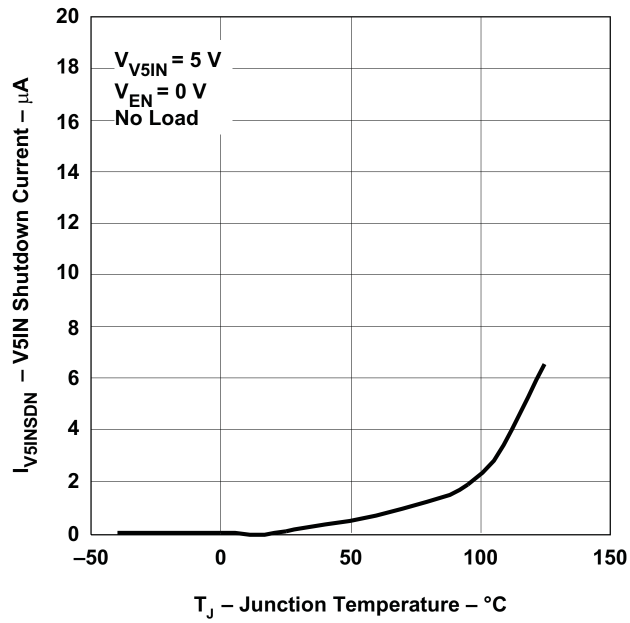


Figure 2.

OVP/UVP THRESHOLD
vs
JUNCTION TEMPERATURE

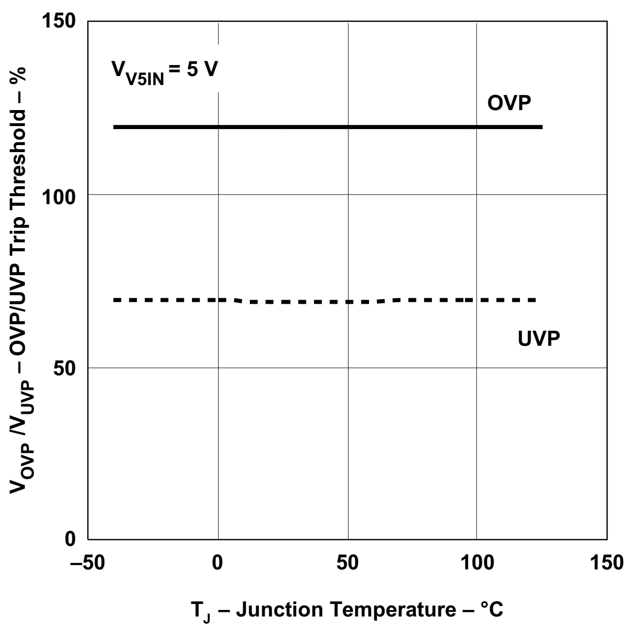


Figure 3.

CURRENT SENSE CURRENT (I_{TRIP})
vs
JUNCTION TEMPERATURE

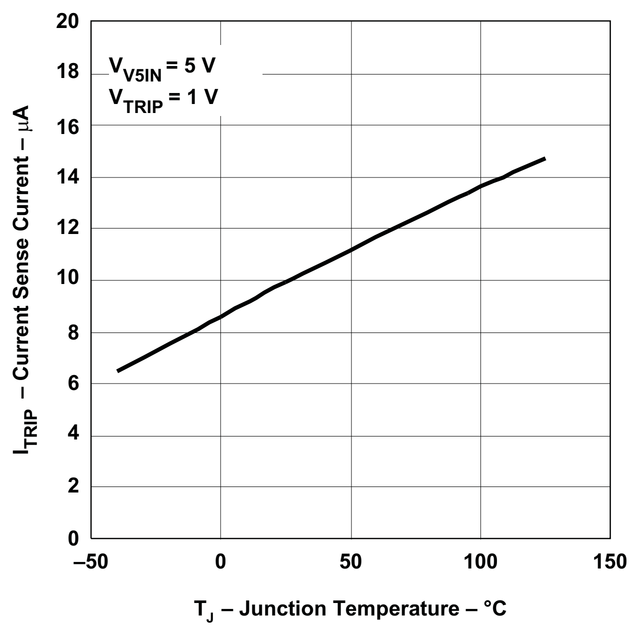


Figure 4.

TYPICAL CHARACTERISTICS (continued)

SWITCHING FREQUENCY
vs
INPUT VOLTAGE

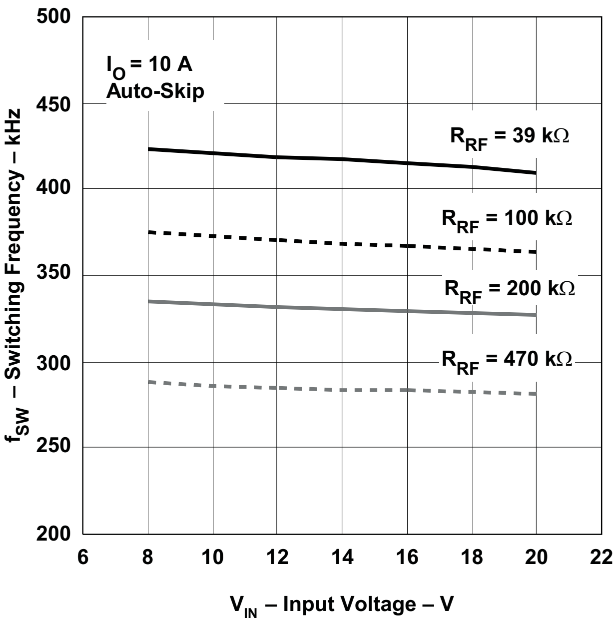


Figure 5.

SWITCHING FREQUENCY
vs
OUTPUT CURRENT

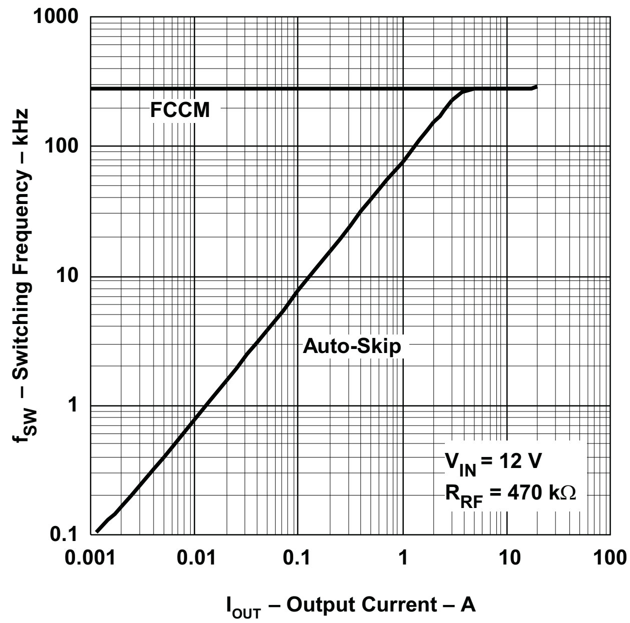


Figure 6.

SWITCHING FREQUENCY
vs
OUTPUT CURRENT

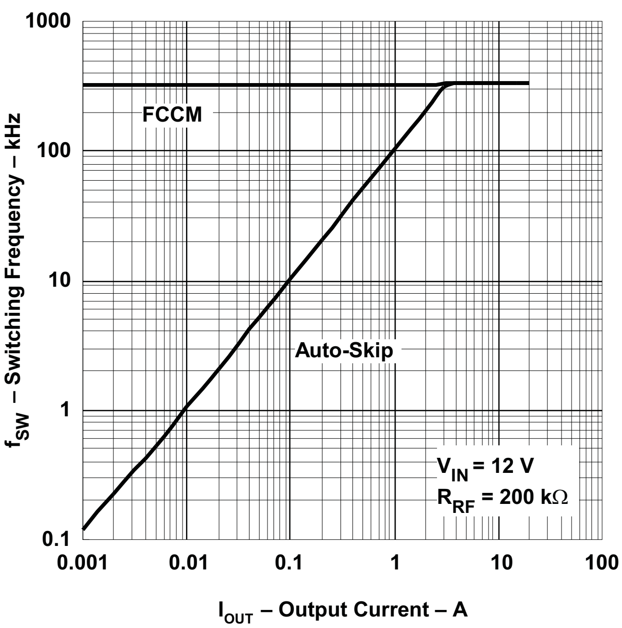


Figure 7.

SWITCHING FREQUENCY
vs
OUTPUT CURRENT

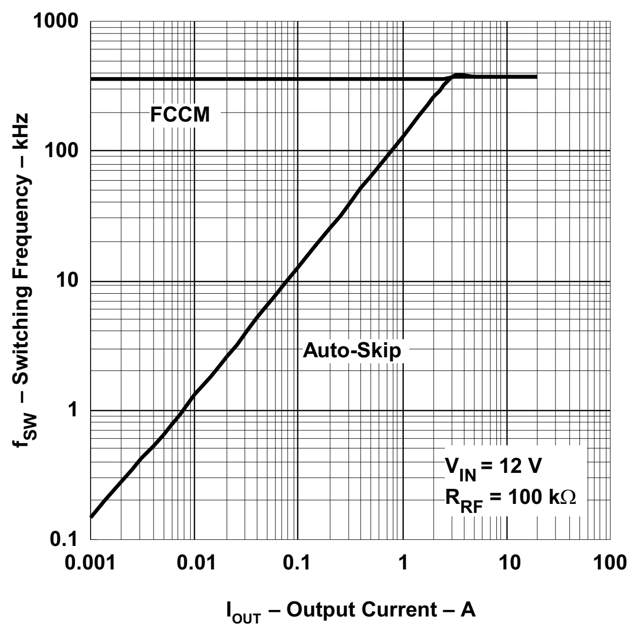


Figure 8.

TYPICAL CHARACTERISTICS (continued)

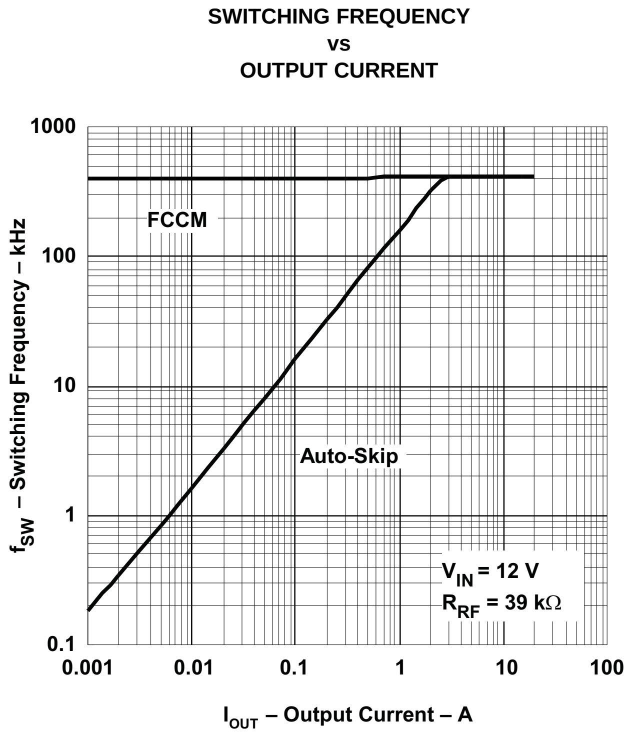


Figure 9.

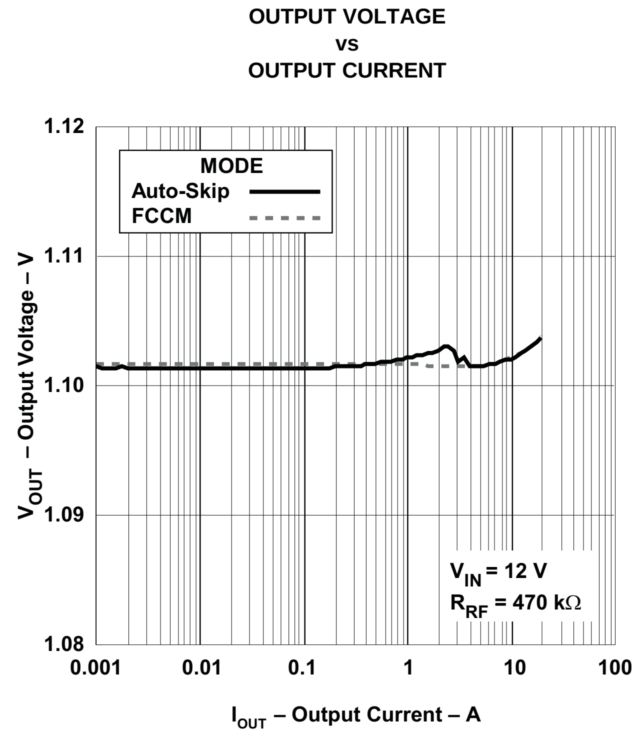


Figure 10.

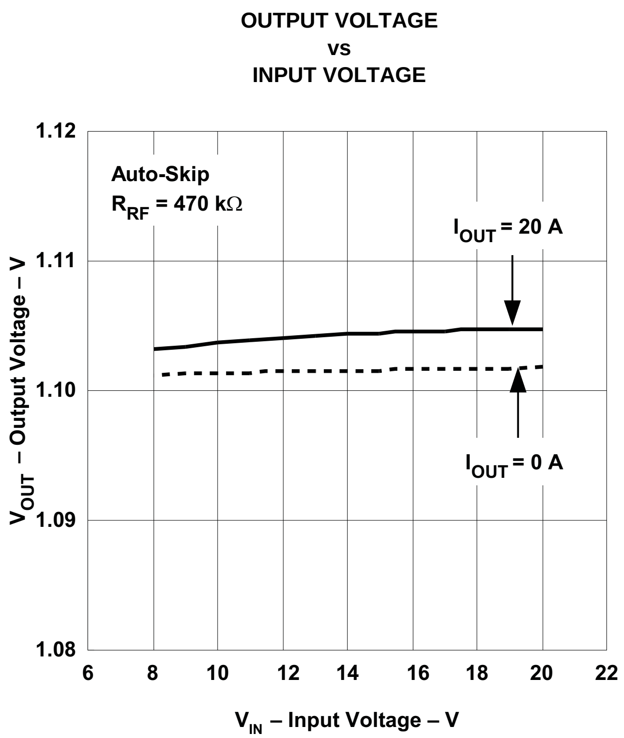


Figure 11.

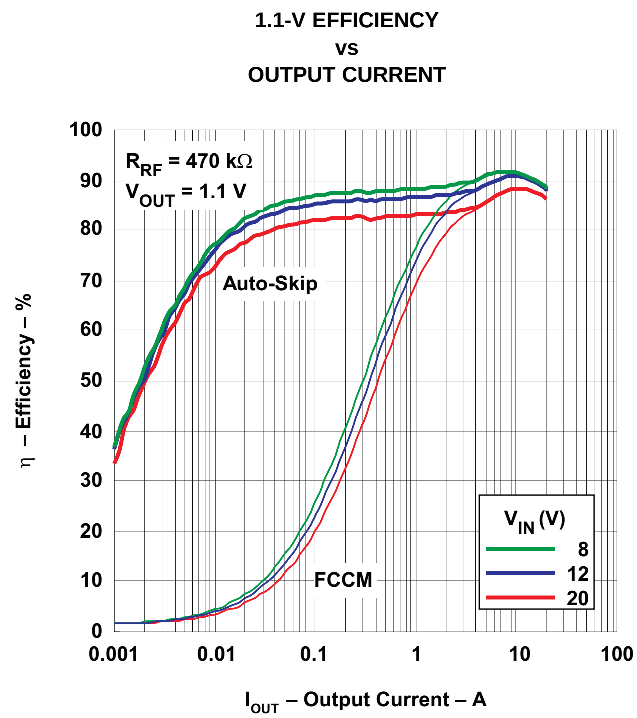


Figure 12.

TYPICAL CHARACTERISTICS (continued)

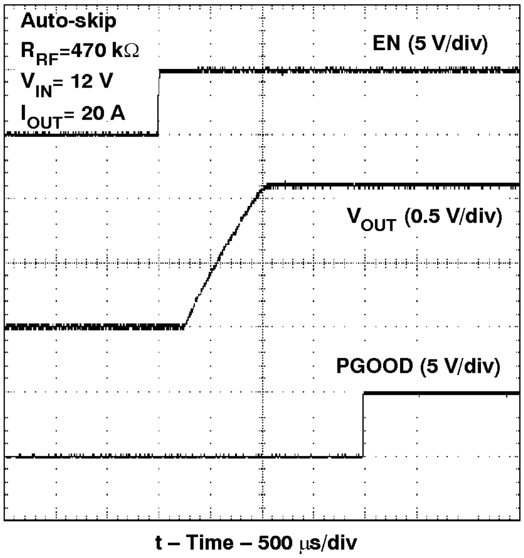


Figure 13. 1.1-V Start-Up Waveform

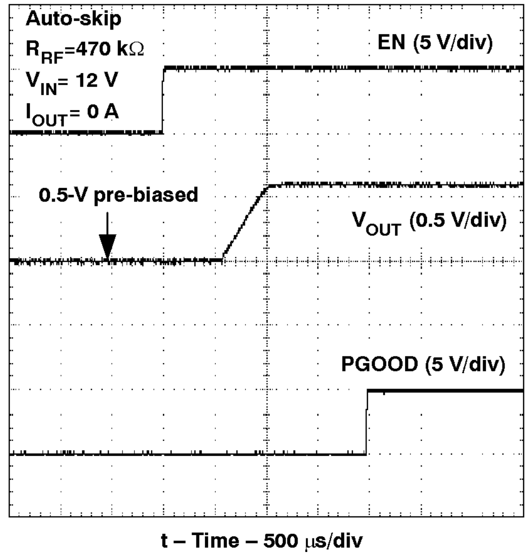


Figure 14. Pre-Biased Start-Up Waveform

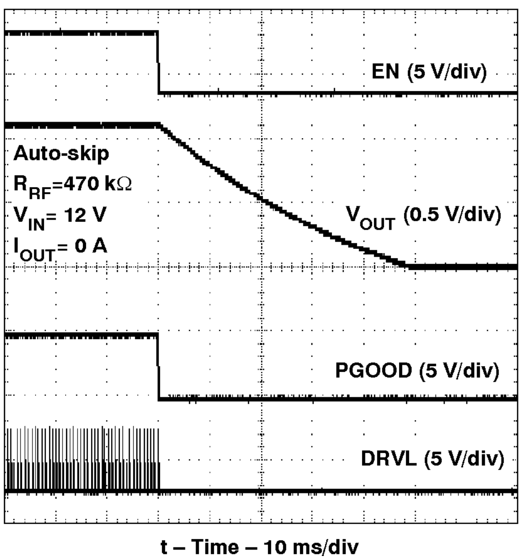


Figure 15. 1.1-V Soft-Stop Waveform

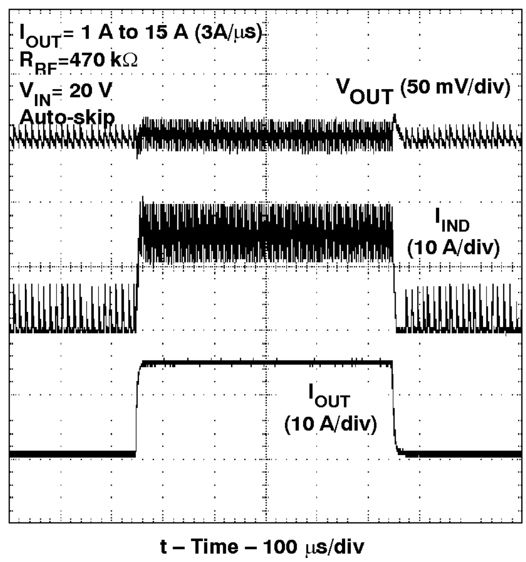


Figure 16. 1.1-V Load Transient Response

APPLICATION INFORMATION

GENERAL DESCRIPTION

The TPS51218 is a high-efficiency, single channel, synchronous buck regulator controller suitable for low output voltage point-of-load applications in notebook computers and similar digital consumer applications. The device features proprietary D-CAP™ mode control combined with adaptive on-time architecture. This combination is ideal for building modern low duty ratio, ultra-fast load step response DC-DC converters. The output voltage ranges from 0.7 V to 2.6 V. The conversion input voltage range is from 3 V to 28 V. The D-CAP™ mode uses the ESR of the output capacitor(s) to sense current information. An advantage of this control scheme is that it does not require an external phase compensation network, helping the designer with ease-of-use and realizing low external component count configuration. The switching frequency is selectable from four preset values using a resistor connected from the RF pin to ground. Adaptive on-time control tracks the preset switching frequency over a wide range of input and output voltages, while it increases the switching frequency at step-up of load.

The RF pin also serves in selecting between auto-skip mode and forced continuous conduction mode for light load conditions. The strong gate drivers of the TPS51218 allow low $R_{DS(on)}$ FETs for high current applications.

ENABLE AND SOFT START

When the EN pin voltage rises above the enable threshold, (typically 1.2 V) the controller enters its start-up sequence. The first 250 μs calibrates the switching frequency setting resistance attached at RF to GND and stores the switching frequency code in internal registers. A voltage of 0.1 V is applied to RF for measurement. Switching is inhibited during this phase. In the second phase, internal DAC starts ramping up the reference voltage from 0 V to 0.7 V. This ramping time is 750 μs. Smooth and constant ramp up of the output voltage is maintained during start up regardless of load current. Connect a 1-kΩ resistor in series with the EN pin to provide protection.

ADAPTIVE ON-TIME D-CAP™ CONTROL

TPS51218 does not have a dedicated oscillator that determines switching frequency. However, the device runs with pseudo-constant frequency by feed-forwarding the input and output voltages into its on-time one-shot timer. The adaptive on-time control adjusts the on-time to be inversely proportional to the input voltage and proportional to the output voltage ($t_{ON} \propto V_{OUT} / V_{IN}$). This makes the switching frequency fairly constant in steady state conditions over wide input voltage range. The switching frequency is selectable from four preset values by a resistor connected to RF as shown in Table 1. (Leaving the resistance open sets the switching frequency to the lowest value, 290 kHz. However, it is recommended to apply one of the resistances on the table in any application designs.)

Table 1. Resistor and Switching Frequency

RESISTANCE (R_{RF}) (kΩ)	SWITCHING FREQUENCY (f_{SW}) (kHz)
470	290
200	340
100	380
39	430

The off-time is modulated by a PWM comparator. The VFB node voltage (the mid point of resistor divider) is compared to the internal 0.7-V reference voltage added with a ramp signal. When both signals match, the PWM comparator asserts the *set* signal to terminate the off-time (turn off the low-side MOSFET and turn on high-side MOSFET). The set signal becomes valid if the inductor current level is below OCP threshold, otherwise the off-time is extended until the current level to become below the threshold.

SMALL SIGNAL MODEL

From small-signal loop analysis, a buck converter using D-CAP™ mode can be simplified as shown in Figure 17.

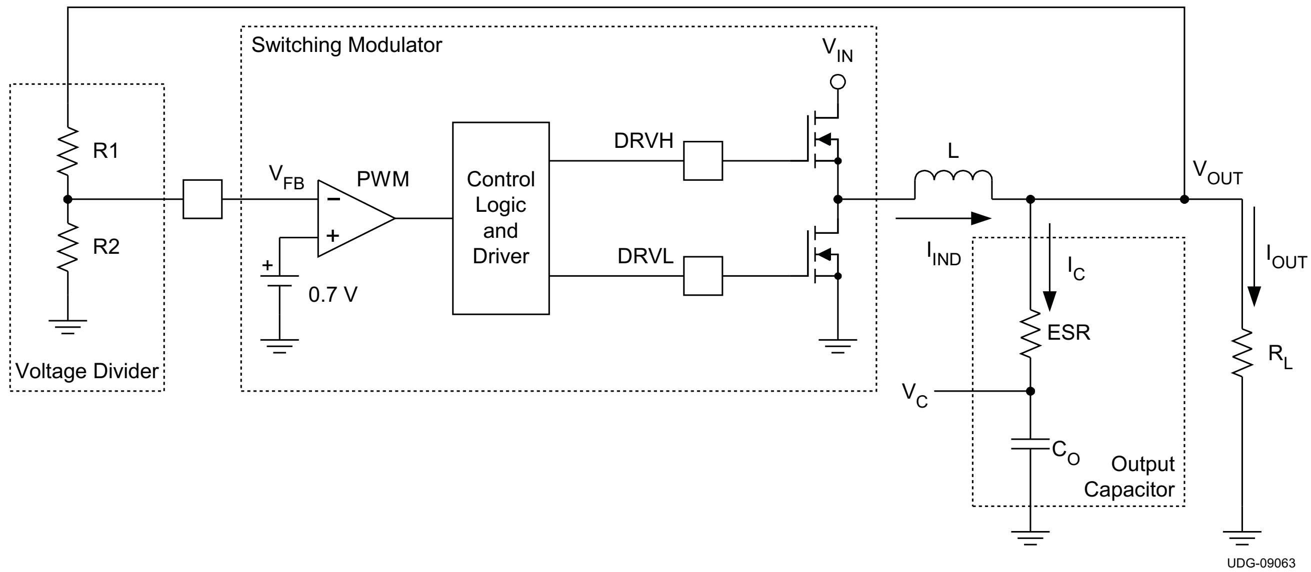


Figure 17. Simplified Modulator Model

The output voltage is compared with internal reference voltage (ramp signal is ignored here for simplicity). The PWM comparator determines the timing to turn on the high-side MOSFET. The gain and speed of the comparator can be assumed high enough to keep the voltage at the beginning of each on cycle substantially constant.

$$H(s) = \frac{1}{s \times ESR \times C_O} \quad (1)$$

For loop stability, the 0-dB frequency, f_0, defined in Equation 2 need to be lower than 1/4 of the switching frequency.

$$f_0 = \frac{1}{2\pi \times ESR \times C_O} \le \frac{f_{SW}}{4} \quad (2)$$

According to Equation 2, the loop stability of D-CAP™ mode modulator is mainly determined by the capacitor's chemistry. For example, specialty polymer capacitors (SP-CAP) have C_O on the order of several 100 µF and ESR in range of 10 mΩ. These makes f_0 on the order of 100 kHz or less and the loop is stable. However, ceramic capacitors have an f_0 of more than 700 kHz, which is not suitable for this modulator.

RAMP SIGNAL

The TPS51218 adds a ramp signal to the 0.7-V reference in order to improve its jitter performance. As described in the previous section, the feedback voltage is compared with the reference information to keep the output voltage in regulation. By adding a small ramp signal to the reference, the S/N ratio at the onset of a new switching cycle is improved. Therefore the operation becomes less jittery and more stable. The ramp signal is controlled to start with –7 mV at the beginning of ON-cycle and becomes 0 mV at the end of OFF-cycle in continuous conduction steady state.

LIGHT LOAD CONDITION IN AUTO-SKIP OPERATION

With RF pin pulled down to low via R_{RF}, the TPS51218 automatically reduces switching frequency at light load conditions to maintain high efficiency. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to the point that its rippled *valley* touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when this zero inductor current is detected. As the load current further decreases, the converter runs in to discontinuous conduction mode. The on-time is kept almost the same as it was in the continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. The transition point to the light load operation $I_{O(LL)}$ (i.e., the threshold between continuous and discontinuous conduction mode) can be calculated in Equation 3.

$$I_{O(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}}$$

where

- f_{SW} is the PWM switching frequency (3)

Switching frequency versus output current in the light load condition is a function of L, V_{IN} and V_{OUT}, but it decreases almost proportional to the output current from the $I_{O(LL)}$ given in Equation 3. For example, it is 58 kHz at $I_{O(LL)}/5$ if the frequency setting is 290 kHz.

ADAPTIVE ZERO CROSSING

The TPS51218 has an adaptive zero crossing circuit which performs optimization of the zero inductor current detection at skip mode operation. This function pursues ideal low-side MOSFET turning off timing and compensates inherent offset voltage of the ZC comparator and delay time of the ZC detection circuit. It prevents SW-node swing-up caused by too late detection and minimizes diode conduction period caused by too early detection. As a result, better light load efficiency is delivered.

FORCED CONTINUOUS CONDUCTION MODE

When the RF pin is tied high, the controller keeps continuous conduction mode (CCM) in light load condition. In this mode, switching frequency is kept almost constant over the entire load range which is suitable for applications need tight control of the switching frequency at a cost of lower efficiency. To set the switching frequency to be the same as Auto-skip mode, it is recommended to connect R_{RF} to PGOOD. In this way, RF is tied low prior to soft-start operation to set frequency and tied high after powergood indicates high.

OUTPUT DISCHARGE CONTROL

When EN is low, the TPS51218 discharges the output capacitor using internal MOSFET connected between SW and GND while high-side and low-side MOSFETs are kept off. The current capability of this MOSFET is limited to discharge slowly.

LOW-SIDE DRIVER

The low-side driver is designed to drive high current low $R_{DS(on)}$ N-channel MOSFET(s). The drive capability is represented by its internal resistance, which are 1.0Ω for V5IN to DRVL and 0.5Ω for DRVL to GND. A dead time to prevent shoot through is internally generated between high-side MOSFET off to low-side MOSFET on, and low-side MOSFET off to high-side MOSFET on. 5-V bias voltage is delivered from V5IN supply. The instantaneous drive current is supplied by an input capacitor connected between V5IN and GND. The average drive current is equal to the gate charge at Vgs=5V times switching frequency. This gate drive current as well as the high-side gate drive current times 5V makes the driving power which need to be dissipated from TPS51218 package.

HIGH-SIDE DRIVER

The high-side driver is designed to drive high current, low $R_{DS(on)}$ N-channel MOSFET(s). When configured as a floating driver, 5 V of bias voltage is delivered from V5IN supply. The average drive current is also equal to the gate charge at V_{GS}=5V times switching frequency. The instantaneous drive current is supplied by the flying capacitor between VBST and SW pins. The drive capability is represented by its internal resistance, which are 1.5 Ω for VBST to DRVH and 0.7 Ω for DRVH to SW.

POWER-GOOD

The TPS51218 has powergood output that indicates high when switcher output is within the target. The powergood function is activated after soft-start has finished. If the output voltage becomes within +10%/–5% of the target value, internal comparators detect power-good state and the power-good signal becomes high after a 1-ms internal delay. If the output voltage goes outside of +15%/–10% of the target value, the powergood signal becomes low after a 2-μs internal delay. The powergood output is an open-drain output and must be pulled up externally.

CURRENT SENSE AND OVER CURRENT PROTECTION

TPS51218 has cycle-by-cycle overcurrent limiting control. The inductor current is monitored during the OFF state and the controller keeps the OFF state during the inductor current is larger than the overcurrent trip level. To provide both good accuracy and cost effective solution, the TPS51218 supports temperature compensated MOSFET $R_{DS(on)}$ sensing. The TRIP pin should be connected to GND through the trip voltage setting resistor, R_{TRIP}. The TRIP terminal sources I_{TRIP} current, which is 10μA typically at room temperature, and the trip level is set to the OCL trip voltage V_{TRIP} as shown in Equation 4. Note that V_{TRIP} is limited up to approximately 3 V internally.

$$V_{TRIP}(mV) = R_{TRIP}(k\Omega) \times I_{TRIP}(\mu A) \tag{4}$$

The inductor current is monitored by the voltage between GND pad and SW pin so that the SW pin should be connected to the drain terminal of the low-side MOSFET properly. I_{TRIP} has 4700ppm/°C temperature slope to compensate the temperature dependency of the $R_{DS(on)}$. GND is used as the positive current sensing node so that GND should be connected to the proper current sensing device, i.e. the source terminal of the low-side MOSFET.

As the comparison is done during the OFF state, V_{TRIP} sets valley level of the inductor current. Thus, the load current at overcurrent threshold, I_{OCP}, can be calculated in Equation 5

$$I_{OCP} = \left(\frac{V_{TRIP}}{8 \times R_{DS(on)}}\right) + \frac{I_{IND(ripple)}}{2} = \frac{V_{TRIP}}{8 \times R_{DS(on)}} + \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \tag{5}$$

In an overcurrent condition, the current to the load exceeds the current to the output capacitor thus the output voltage tends to fall down. Eventually, it crosses the undervoltage protection threshold and shuts down the controller.

When the device is operating in the forced continuous conduction mode, the negative current limit (NCL) protects the external FET from carrying too much current. The NCL detect threshold is set as the same absolute value as positive OCL but negative polarity. Please be noted the threshold still represents the valley value of the inductor current.

OVER/UNDER VOLTAGE PROTECTION

TPS51218 monitors a resistor divided feedback voltage to detect over and undervoltage. When the feedback voltage becomes higher than 120% of the target voltage, the OVP comparator output goes high and the circuit latches as the high-side MOSFET driver OFF and the low-side MOSFET driver ON.

When the feedback voltage becomes lower than 70% of the target voltage, the UVP comparator output goes high and an internal UVP delay counter begins counting. After a 1-ms delay, TPS51218 latches OFF both high-side and low-side MOSFETs drivers. This function is enabled after 1.2 ms following EN has become high.

UVLO PROTECTION

TPS51218 has V5IN undervoltage lockout protection (UVLO). When the V5IN voltage is lower than UVLO threshold voltage, the switch mode power supply shuts off. This is non-latch protection.

THERMAL SHUTDOWN

TPS51218 monitors the die temperature. If the temperature exceeds the threshold value (typically 145°C), the TPS51218 is shut off. This is non-latch protection.

EXTERNAL COMPONENTS SELECTION

Selecting external components is simple in D-CAP™ mode.

1. Choose the inductor.

The inductance value should be determined to give the ripple current of approximately 1/4 to 1/2 of maximum output current. Larger ripple current increases output ripple voltage and improves S/N ratio and helps stable operation.

$$L = \frac{1}{I_{IND(ripple)} \times f_{SW}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} = \frac{3}{I_{OUT(max)} \times f_{SW}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} \quad (6)$$

The inductor also needs to have low DCR to achieve good efficiency, as well as enough room above peak inductor current before saturation. The peak inductor current can be estimated in Equation 7.

$$I_{IND(peak)} = \frac{V_{TRIP}}{8 \times R_{DS(on)}} + \frac{1}{L \times f_{SW}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} \quad (7)$$

2. Choose the output capacitor(s).

Organic semiconductor capacitor(s) or specialty polymer capacitor(s) are recommended. For loop stability, capacitance and ESR should satisfy Equation 2. For jitter performance, Equation 8 is a good starting point to determine ESR.

$$ESR = \frac{V_{OUT} \times 10[mV] \times (1-D)}{0.7[V] \times I_{IND(ripple)}} = \frac{10[mV] \times L \times f_{SW}}{0.7[V]} = \frac{L \times f_{SW}}{70} [\Omega]$$

where

- D is the duty ratio
- the output ripple down slope rate is 10 mV/t_{SW} in terms of VFB terminal voltage as shown in Figure 18
- t_{SW} is the switching period (8)

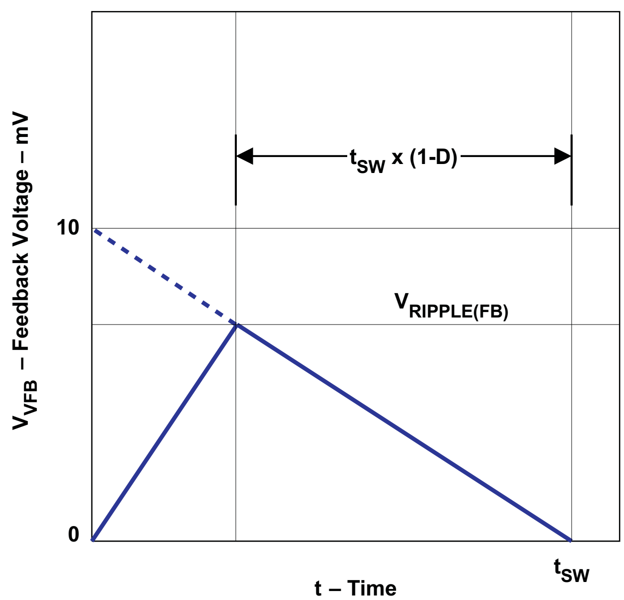


Figure 18. Ripple Voltage Down Slope

3. Determine the value of R1 and R2.

The output voltage is programmed by the voltage-divider resistor, R1 and R2, shown in Figure 17. R1 is connected between the VFB pin and the output, and R2 is connected between the VFB pin and GND. Typical designs begin with the selection of an R2 value between 10 kΩ and 20 kΩ. Determine R1 using Equation 9.

$$R1 = \frac{\left(V_{OUT} - \frac{I_{IND(ripple)} \times ESR}{2}\right) - 0.7}{0.7} \times R2 \quad (9)$$

LAYOUT CONSIDERATIONS

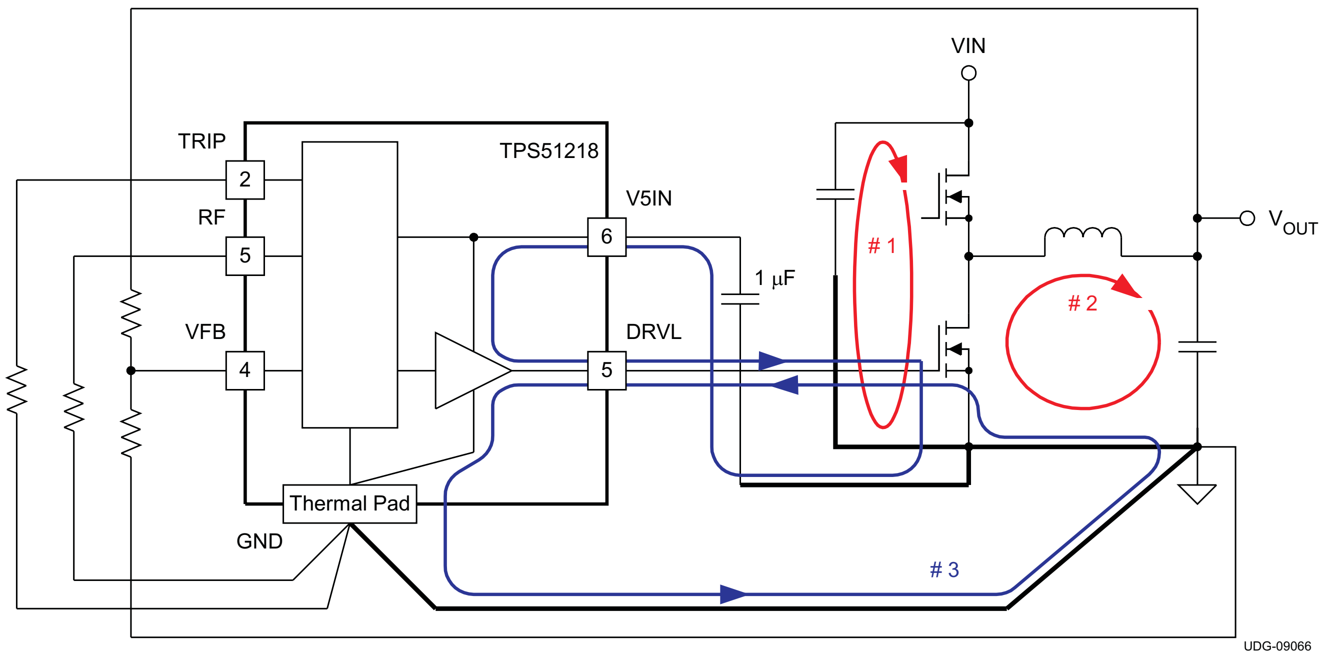


Figure 19. Ground System of DC/DC Converter Using the TPS51218

Certain points must be considered before starting a layout work using the TPS51218.

- Inductor, V_{IN} capacitor(s), V_{OUT} capacitor(s) and MOSFETs are the power components and should be placed on one side of the PCB (solder side). Other small signal components should be placed on another side (component side). At least one inner plane should be inserted, connected to ground, in order to shield and isolate the small signal traces from noisy power lines.
- All sensitive analog traces and components such as VFB, PGOOD, TRIP and RF should be placed away from high-voltage switching nodes such as SW, DRVL, DRVH or VBST to avoid coupling. Use internal layer(s) as ground plane(s) and shield feedback trace from power traces and components.
- The DC/DC converter has several high-current loops. The area of these loops should be minimized in order to suppress generating switching noise.
  - The most important loop to minimize the area of is the path from the V_{IN} capacitor(s) through the high and low-side MOSFETs, and back to the capacitor(s) through ground. Connect the negative node of the V_{IN} capacitor(s) and the source of the low-side MOSFET at ground as close as possible. (Refer to loop #1 of Figure 19)
  - The second important loop is the path from the low-side MOSFET through inductor and V_{OUT} capacitor(s), and back to source of the low-side MOSFET through ground. Connect source of the low-side MOSFET and negative node of V_{OUT} capacitor(s) at ground as close as possible. (Refer to loop #2 of Figure 19)
  - The third important loop is of gate driving system for the low-side MOSFET. To turn on the low-side MOSFET, high current flows from V5IN capacitor through gate driver and the low-side MOSFET, and back to negative node of the capacitor through ground. To turn off the low-side MOSFET, high current flows

from gate of the low-side MOSFET through the gate driver and GND pad of the device, and back to source of the low-side MOSFET through ground. Connect negative node of V5IN capacitor, source of the low-side MOSFET and GND pad of the device at ground as close as possible. (Refer to loop #3 of Figure 19)

- Since the TPS51218 controls output voltage referring to voltage across V_{OUT} capacitor, the top-side resistor of the voltage divider should be connected to the positive node of V_{OUT} capacitor. In a same manner both bottom side resistor and GND pad of the device should be connected to the negative node of V_{OUT} capacitor. The trace from these resistors to the VFB pin should be short and thin. Place on the component side and avoid via(s) between these resistors and the device.
- Connect the overcurrent setting resistors from TRIP pin to ground and make the connections as close as possible to the device. The trace from TRIP pin to resistor and from resistor to ground should avoid coupling to a high-voltage switching node.
- Connect the frequency setting resistor from RF pin to ground, or to the PGOOD pin, and make the connections as close as possible to the device. The trace from the RF pin to the resistor and from the resistor to ground should avoid coupling to a high-voltage switching node.
- Connections from gate drivers to the respective gate of the high-side or the low-side MOSFET should be as short as possible to reduce stray inductance. Use 0.65 mm (25 mils) or wider trace and via(s) of at least 0.5 mm (20 mils) diameter along this trace.
- The PCB trace defined as switch node, which connects to source of high-side MOSFET, drain of low-side MOSFET and high-voltage side of the inductor, should be as short and wide as possible.

LAYOUT CONSIDERATIONS TO REMOTE SENSING

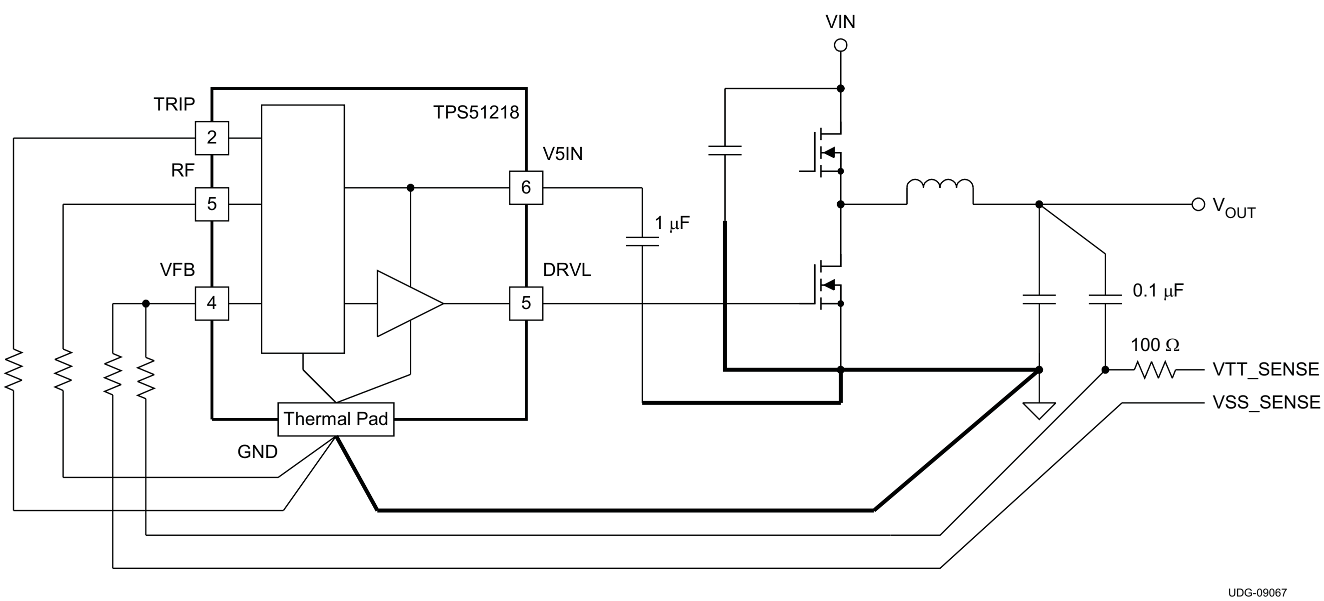


Figure 20. Remote Sensing of Output Voltage Using the TPS51218

- Make a Kelvin connection to the load device.
- Run the feedback signals as a differential pair to the device. The distance of these parallel pair should be as short as possible.
- Run the lines in a quiet layer. Isolate them from noisy signals by a voltage or ground plane.

TPS51218 APPLICATION CIRCUITS

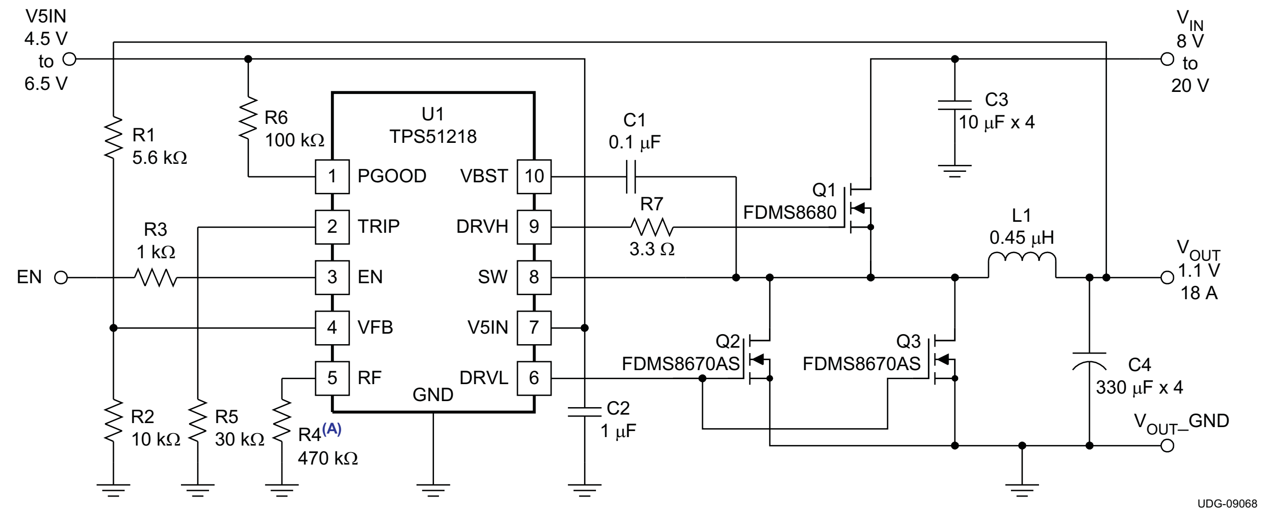
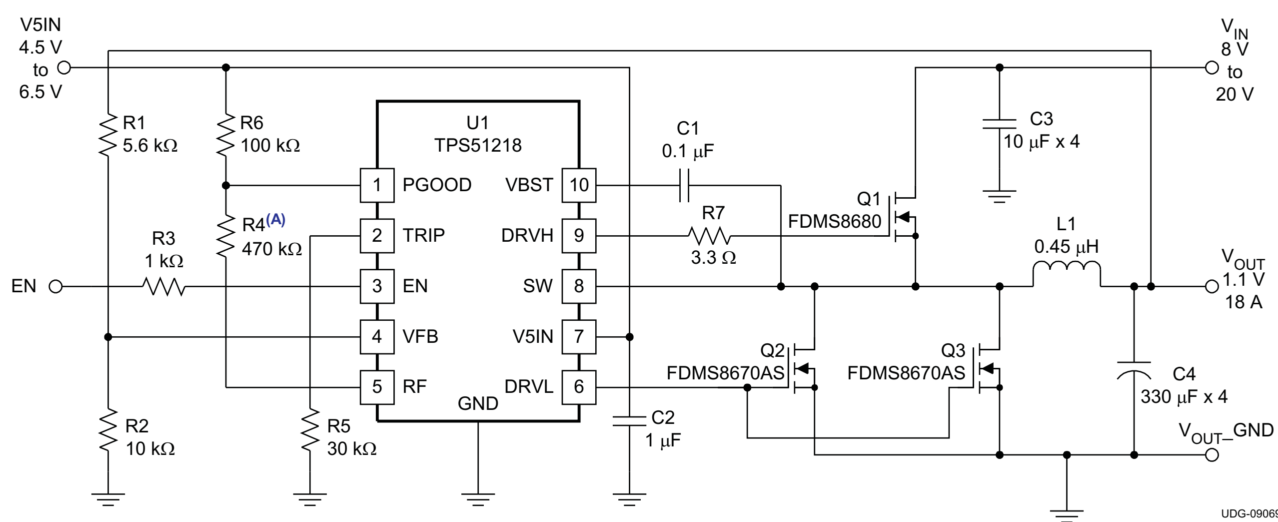


Figure 21. 1.1-V/18-A Auto-Skip Mode



A. See Table 1 for resistor/frequency values.

Figure 22. 1.1-V/18-A Forced Continuous Conduction Mode

Table 2. 1.1-V, 18-A, 290-kHz Application List of Materials

REFERENCE DESIGNATOR	QTY	SPECIFICATION	MANUFACTURER	PART NUMBER
C3	1	4 × 10 μF, 25 V	Taiyo Yuden	TMK325BJ106MM
C4	1	4 × 330 μF, 2 V, 12 mΩ	Panasonic	EEFCX0D331XR
L1	1	0.45 μH, 25 A, 1.1 mΩ	Panasonic	ETQP4LR45XFC
Q1	1	30 V, 35 A, 8.5 mΩ	Fairchild	FDMS8680
Q2, Q3	2	30 V, 42 A, 3.5 mΩ	Fairchild	FDMS8670AS

Changes from Revision A (June 2009) to Revision B	Page
• Added DRVH, pulse width < 20 ns rating in ABSOLUTE MAXIMUM RATINGS table	2
• Added DRVL, pulse width < 20 ns rating in ABSOLUTE MAXIMUM RATINGS table	2

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS51218DSCR	Active	Production	WSON (DSC) | 10	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG | NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PIZI
TPS51218DSCR.A	Active	Production	WSON (DSC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PIZI
TPS51218DSCR.B	Active	Production	WSON (DSC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PIZI
TPS51218DSCRG4.A	Active	Production	WSON (DSC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PIZI
TPS51218DSCRG4.B	Active	Production	WSON (DSC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PIZI
TPS51218DSCT	Active	Production	WSON (DSC) | 10	250 | SMALL T&R	Yes	NIPDAU | NIPDAUAG | NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PIZI
TPS51218DSCT.A	Active	Production	WSON (DSC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PIZI
TPS51218DSCT.B	Active	Production	WSON (DSC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PIZI

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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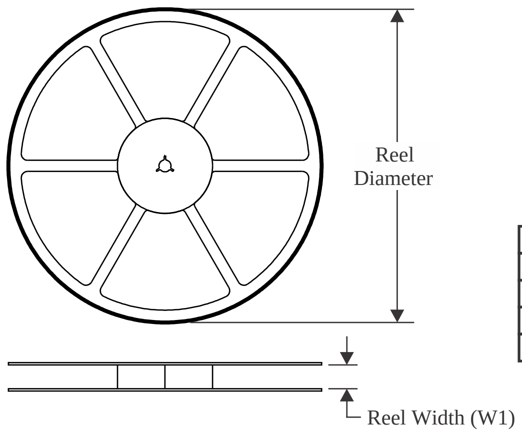
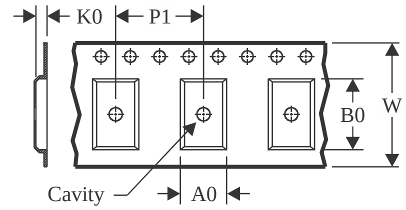
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

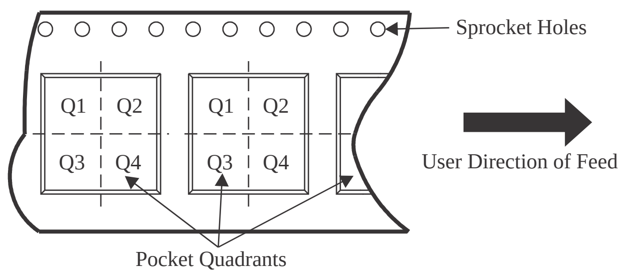


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

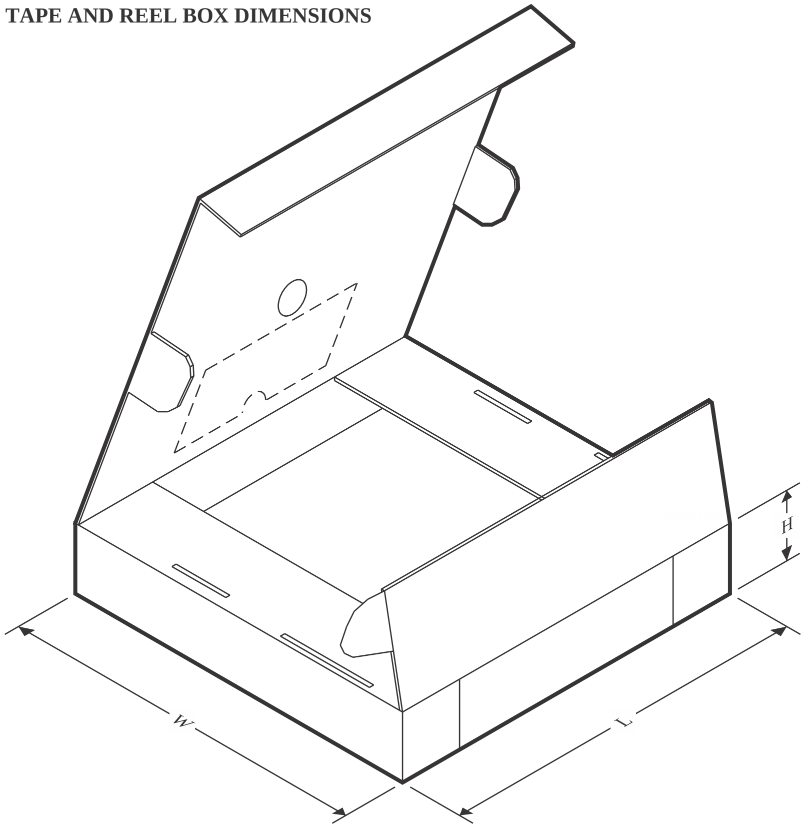
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

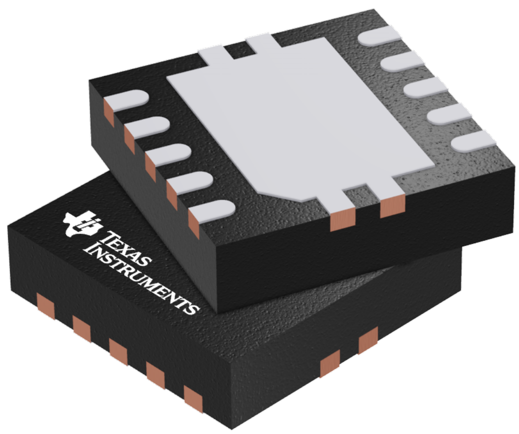
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS51218DSCR	WSON	DSC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS51218DSCR	WSON	DSC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS51218DSCT	WSON	DSC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

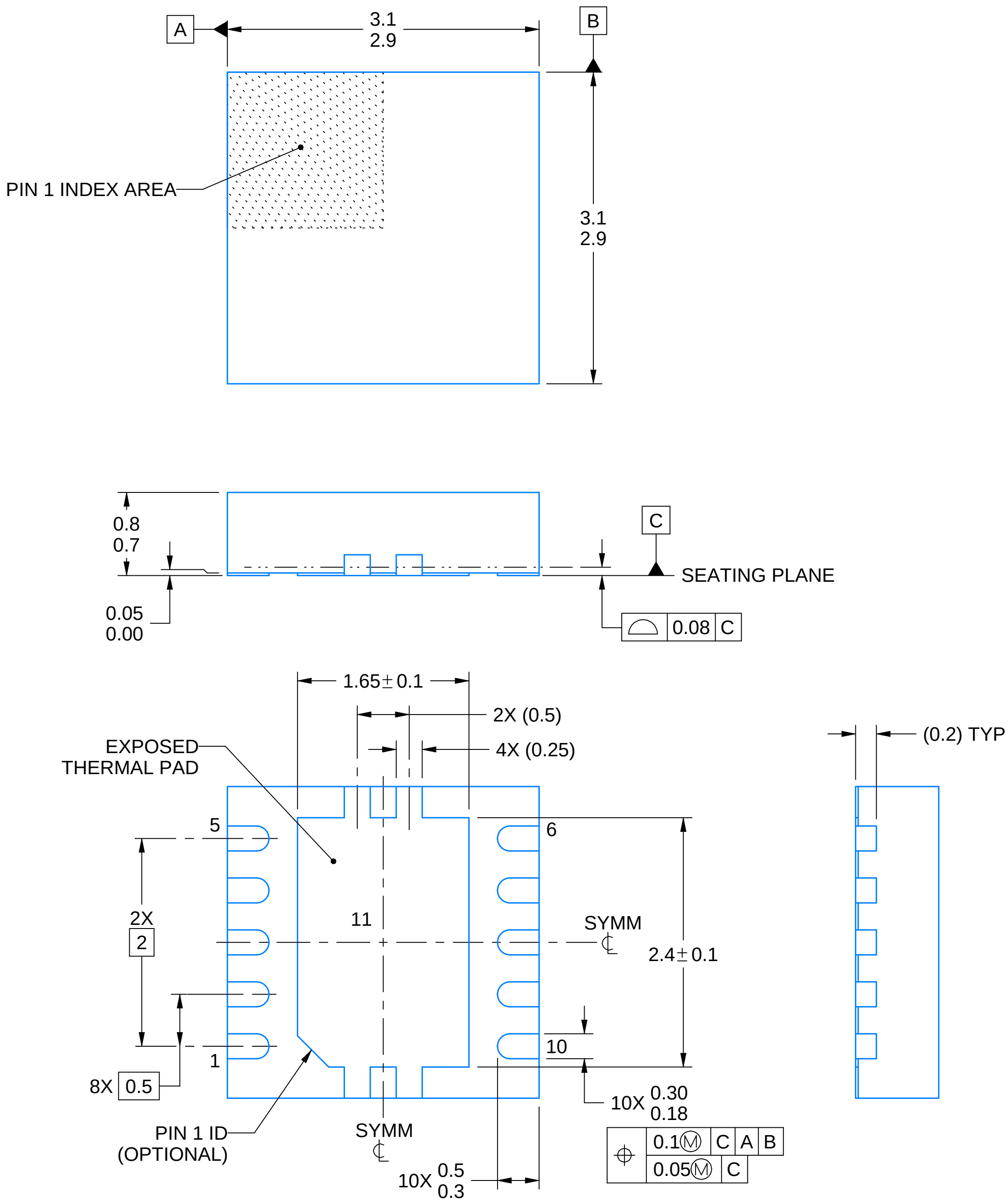


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS51218DSCR	WSON	DSC	10	3000	356.0	356.0	35.0
TPS51218DSCR	WSON	DSC	10	3000	346.0	346.0	33.0
TPS51218DSCT	WSON	DSC	10	250	210.0	185.0	35.0



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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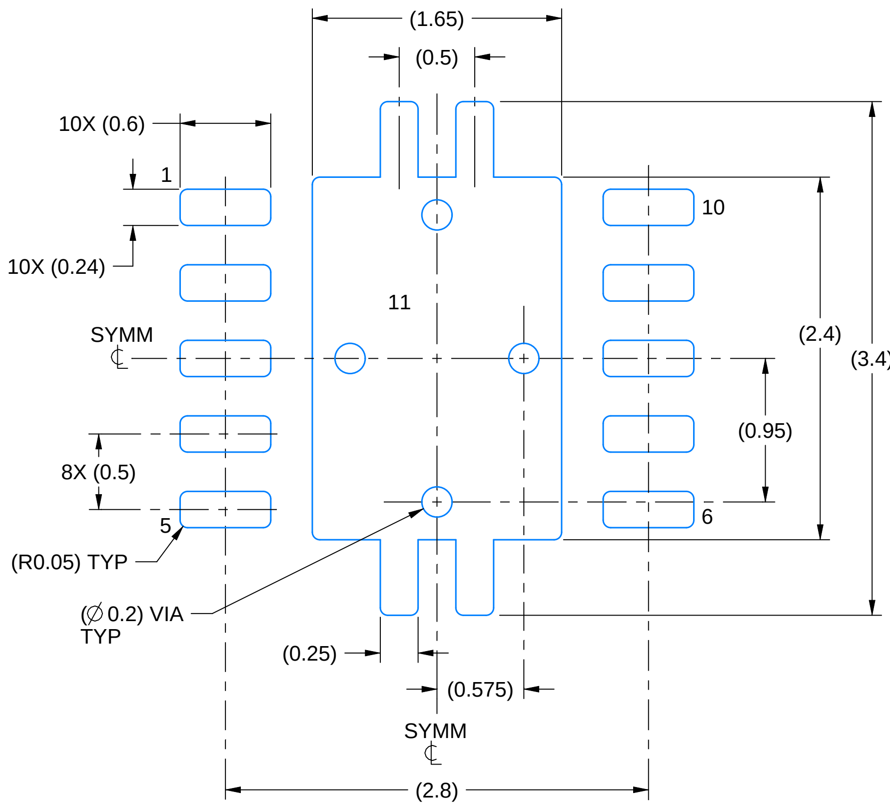
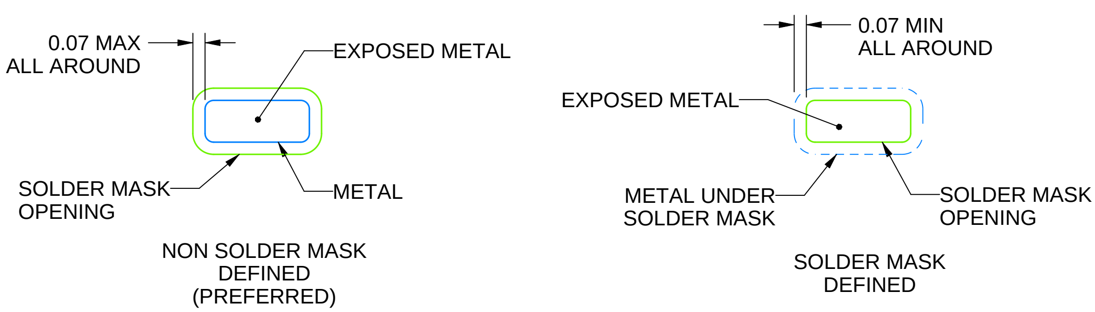
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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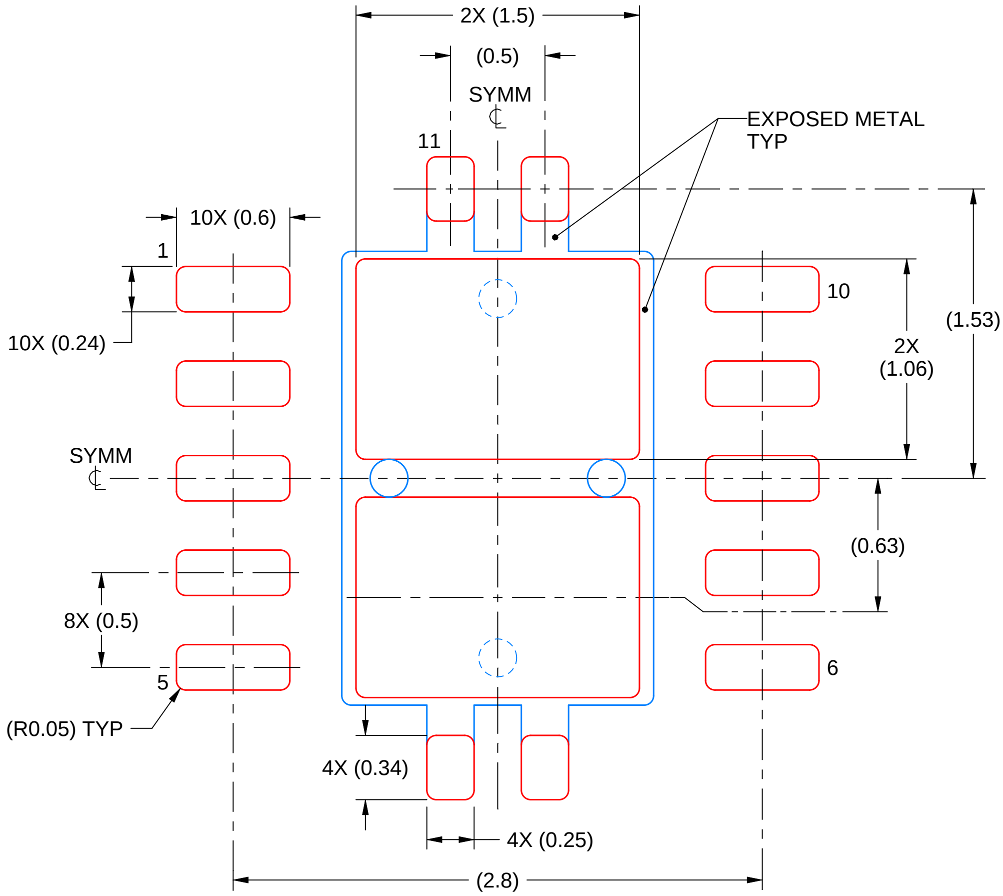
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.