Application Note

UCC28056 System Bring Up Guidelines and Application Debug FAQs

David Huang *High-Voltage Controllers*

ABSTRACT

This application note provides system bring up guidelines for the UCC28056 single-phase CRM controller families.

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1 How to Select the Correct Devices Version of UCC28056 Families?

Table 1-1. Device Comparison Table

Device	UCC28056A	UCC28056B	UCC28056C
Where Used	**PFC Output > 400 V**	**Application With Minimal Audible Noise**	**General Purpose**
Overvoltage Protection Threshold	108% V_{OUT}	110% V_{OUT}	110% V_{OUT}
Second Tier Overvoltage Protection Enabled		✓	✓
Burst Mode Threshold	< 15% Load	< 15% Load	< 10% Load

The UCC28056 families integrate the Zero Current Detection (ZCD) and the Current Sense (CS) feature together at the ZCD/CS pin, to reduce the package size. This makes the devices cost-competitive in of the smallest packages available. The device layout is designed for both precise detection of drain-to-source voltage and OCP signal sampling. The UCC28056A, UCC28056B, and UCC28056C have improved the noise immunity on the ZCD pin making the controller more robust and less sensitive to noise from downstream.

Table 1-1 shows the key differences of each version. The UCC28056A removes the OVP2 feature. Use this device in applications with wider input voltage range and high output voltage. TI also recommends using the device in applications that are not allowed any restart event during surge or lighting test.

The UCC28056C has a lower burst mode threshold compared with the UCC28056A and UCC28056B. Use the UCC28056C in applications that need lower burst mode power.

The minimum frequency for UCC28056C is around 18 kHz to 20 kHz, and UCC28056A, UCC28056B minimum frequency can be higher than 20 kHz. For some applications that detect the audible noise through audible noise test equipment and scan the frequency from 20 Hz to 20 kHz, select the UCC28056A or UCC28056B version.

For more information about the differences of each version, see the *UCC28056 Selection Guide* application brief.

2 How to Complete the Schematic Review of the UCC28056?

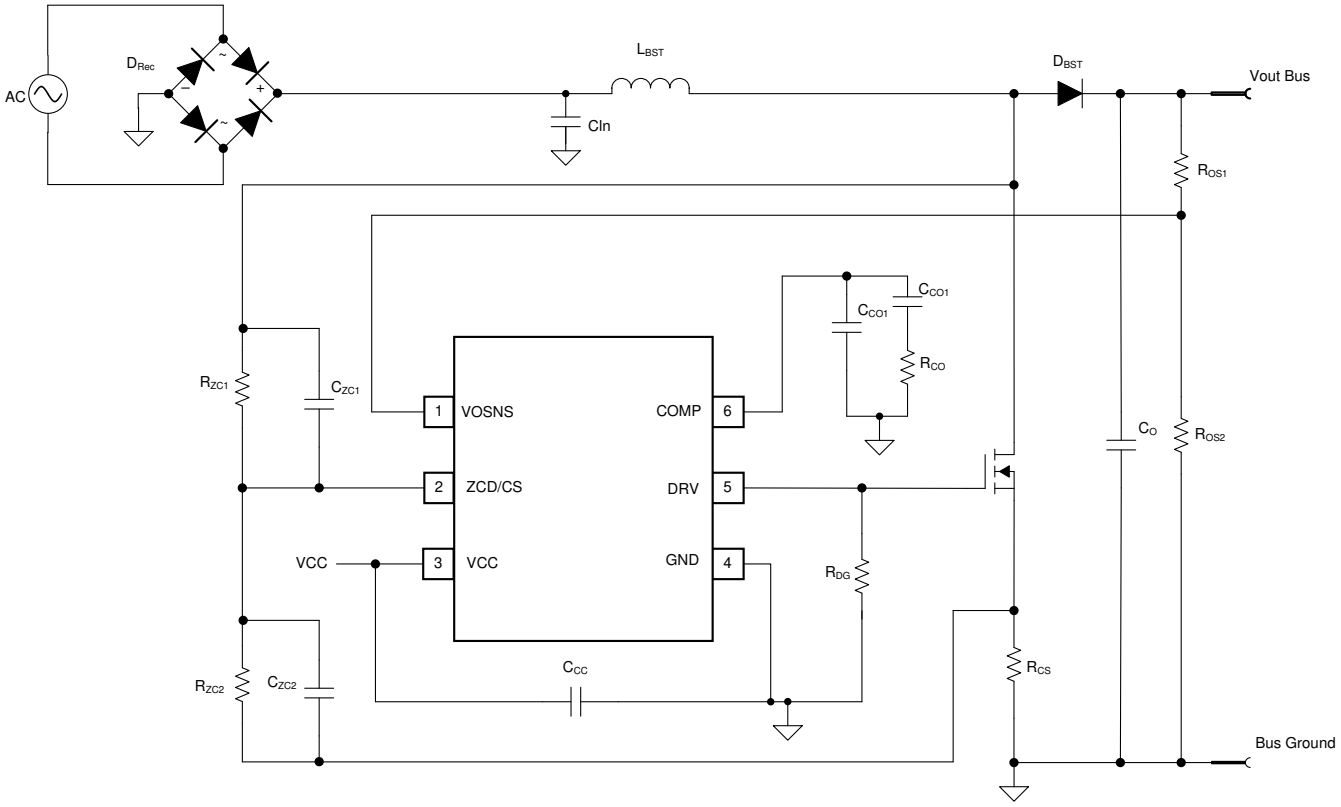


Figure 2-1. UCC28056 Simplified Application

Review the UCC28056 schematic using the simplified application in Figure 2-1 and check each pin of the controller.

2.1 VOSNS Pin

The VOSNS pin voltage is applied to the inverting input of an internal transconductance error amplifier. The output voltage regulation set point (V_{OutReg}) is determined by the external resistor divider network connecting the output voltage to the VOSNS pin. To ensure that the VOSNS pin bias current degrades output voltage regulation by less than 1%, the upper voltage divider resistor value must be less than 39 MΩ. Although it is possible to increase the divider resistance to reduce the standby power, there is some impact on the output voltage regulation accuracy across parts and temperature, so design the total voltage divider resistance to be around 10 MΩ. The capacitance on the VOSNS pin helps to filter the switching noise and use SMD capacitance with a value of less than 3.3 nF. A higher value may increase the PFC output voltage loop response time.

2.2 ZCD/CS Pin

An external divider network attached to the ZCD/CS pin transfers both the attenuated drain-to-source voltage (V_{DS}) waveform and the current sense signal (V_{CS}) into the controller. This transfer is possible because the current sense signal requires observation only when the switch is ON and the V_{DS} signal is close to zero. The drain voltage waveform requires sensing only when the switch is OFF and the current sense signal is close to zero. Both the resistor and capacitor dividers on the ZCD/CS pin are necessary. The resistor divider is for Vinac sampling when the controller still does not output pulses to drive the switching device. Add the capacitor divider in parallel with the resistor divider to use high value resistors without introducing filtering and associated phase shift. In this case, ensure that the reactive divider ratio is equal to the resistor divider ratio.

TI recommends starting with a resistor and capacitor divider ratio of 400:1, then fine-tune the capacitor divider following the *ZCD/CS Pin* section in the *UCC28056 6-Pin Single-Phase Transition-Mode PFC Controller* datasheet.

2.3 DRV Pin

At light load condition when the controller is working at Discontinuous Current Mode (DCM), it is better to turn on the switching MOSFET when drain voltage is at its minimum voltage level to achieve a maximum efficiency. An external resistor connected from DRV to GND adjusts the delay between the drain waveform falling below V_{IN} and the DRV rising edge, allowing the turn on transition to be aligned to the valley minimum accurately over a wide range of idle ring oscillating frequency. Different resistor values of R_{DG} set eight different delay times(T_{ZCDR0} – T_{ZCDR7}).

Fine-tune the R_{DG} value for a given switching MOSFET and PFC inductor. Figure 2-2 and Figure 2-3 list the resistor values and the delay times as shown in the data sheet.

R_{DG0}	DRV to GND resistance value to select T_{ZCDR0} (1)		130	200		kΩ
R_{DG1}	DRV to GND resistance value to select T_{ZCDR1} (1)		81.18	82	82.82	kΩ
R_{DG2}	DRV to GND resistance value to select T_{ZCDR2} (1)		61.38	62	62.62	kΩ
R_{DG3}	DRV to GND resistance value to select T_{ZCDR3} (1)		42.57	43	43.43	kΩ
R_{DG4}	DRV to GND resistance value to select T_{ZCDR4} (1)		26.73	27	27.27	kΩ
R_{DG5}	DRV to GND resistance value to select T_{ZCDR5} (1)		17.82	18	18.18	kΩ
R_{DG6}	DRV to GND resistance value to select T_{ZCDR6} (1)		12.87	13	13.13	kΩ
R_{DG7}	DRV to GND resistance value to select T_{ZCDR7} (1)		9	9.1	9.2	kΩ

Figure 2-2. Eight Different R_{DG} Resistors Settings

T_{ZCDR0}	Minimum ZCD to DRV delay.	From V_{ZC} < $V_{InSynth}$ to DRV = 6V, C_{DR} = 1nF, Fres = 1.2MHz, R_{DG} = R_{DG0}		170	235	ns
ΔT_{ZCDR1}	$T_{ZCDR1} = T_{ZCDR0} + \Delta T_{ZCDR1}$ (1)	$R_{DG} = R_{DG1}$	34.6	45.5	58.5	ns
ΔT_{ZCDR2}	$T_{ZCDR2} = T_{ZCDR0} + \Delta T_{ZCDR2}$ (1)	$R_{DG} = R_{DG2}$	76	90	107	ns
ΔT_{ZCDR3}	$T_{ZCDR3} = T_{ZCDR0} + \Delta T_{ZCDR3}$ (1)	$R_{DG} = R_{DG3}$	114	130	147	ns
ΔT_{ZCDR4}	$T_{ZCDR4} = T_{ZCDR0} + \Delta T_{ZCDR4}$ (1)	$R_{DG} = R_{DG4}$	157	175	193	ns
ΔT_{ZCDR5}	$T_{ZCDR5} = T_{ZCDR0} + \Delta T_{ZCDR5}$ (1)	$R_{DG} = R_{DG5}$	229	255	281	ns
ΔT_{ZCDR6}	$T_{ZCDR6} = T_{ZCDR0} + \Delta T_{ZCDR6}$ (1)	$R_{DG} = R_{DG6}$	301	335	369	ns
ΔT_{ZCDR7}	$T_{ZCDR7} = T_{ZCDR0} + \Delta T_{ZCDR7}$ (1)	$R_{DG} = R_{DG7}$	373	415	457	ns

Figure 2-3. Eight Different T_{ZCDR} Delay Times

2.4 GND Pin

The GND pin is the controller ground reference pin. It is important to connect this pin to the power stage at the lower terminal of the current sense resistor to sample current precisely when the MOSFET is on.

2.5 VCC Pin

Switching operation can start once VCC exceeds $V_{CCStart}$. Switching operation ceases if VCC drops below V_{CCStop} for longer than $T_{UVLOBlk}$. Add at least a 0.47-µF supply and decoupling capacitor on this pin. This capacitor supplies the high current pulses needed to charge the gate capacitance of the power MOSFET. So at higher power applications, you may need to increase the value if a higher gate charge (Qg) MOSFET is selected.

2.6 COMP Pin

To achieve compensation of the voltage loop, add a Type-II compensation network from this pin to GND.

3 How to Test and Confirm the UCC28056 Working Mode?

To better understand the working condition of the controller, it is useful to capture the ZCD/CS, PFC inductor current, and VDS of MOSFET to confirm whether the controller is working as expected. This section shows how to capture the ZCD/CS waveform and normal working mode waveforms.

3.1 How to Capture the ZCD/CS Waveform?

Accurate measurement of the ZCD/CS pin waveform is an important way to fine-tune the robust operation of the UCC28056. To better see what is happening, place the VDS and ZCD/CS pin waveforms on the same scale with the same ground reference, if your oscilloscope allows it. Otherwise, use a 100:1 attenuation probe and a 1:1 probe for the test.

If the VDS waveform is set to 100 V/Div attenuation, click on the ZCD/CS pin channel and select *More* from the menu. Then select the *Fine Scale* menu and adjust this channel to 250 mV/Div. The result is 400:1 difference between the scales of the two channels.

Now if the zero line is set at the same point for each channel, the two traces should have the same amplitude.

Since ZCD/CS is sensitive signal, use a low-capacitance probe (below 10 pF) with the smallest test loop between the ZCD/CS pin and ground. Follow Figure 3-1 when setting up the oscilloscope and probe.

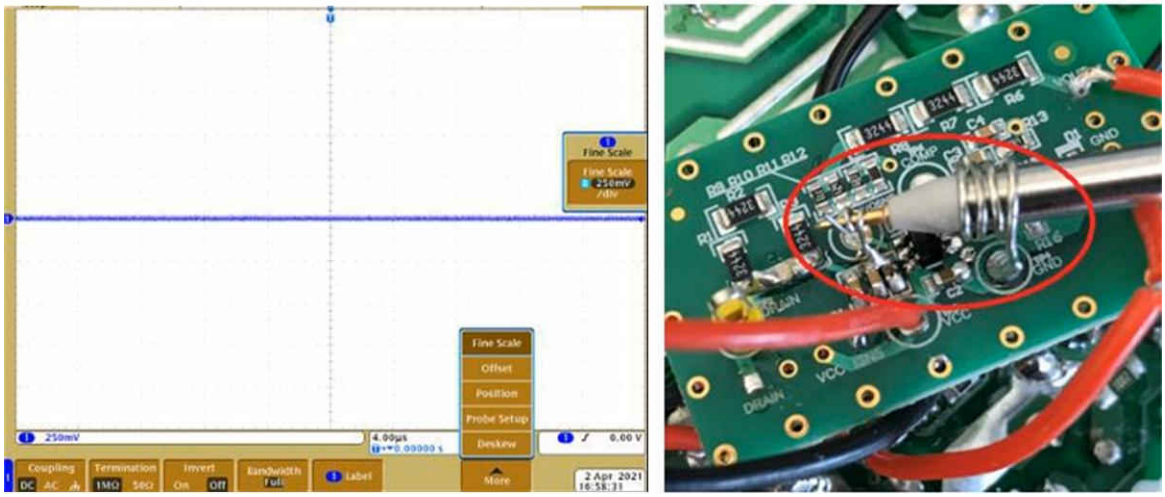


Figure 3-1. Fine Scale Menu of the Oscilloscope and Probe Connecting

This method allows a clear check of how well these two waveforms are following each other. The waveform in Figure 3-2 shows the VDS and ZCD/CS together.

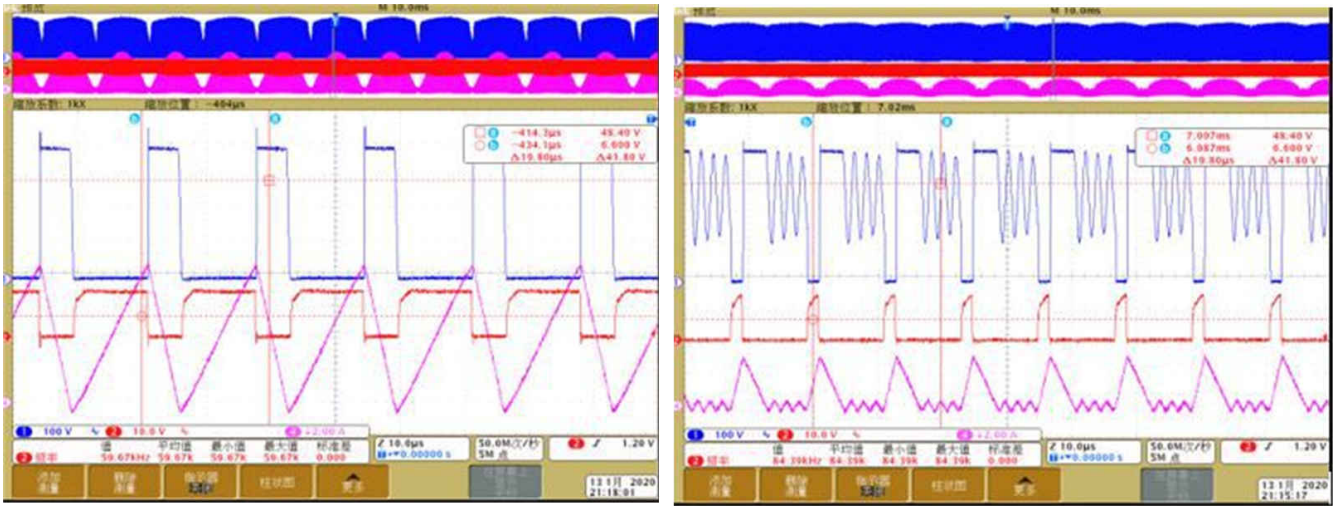
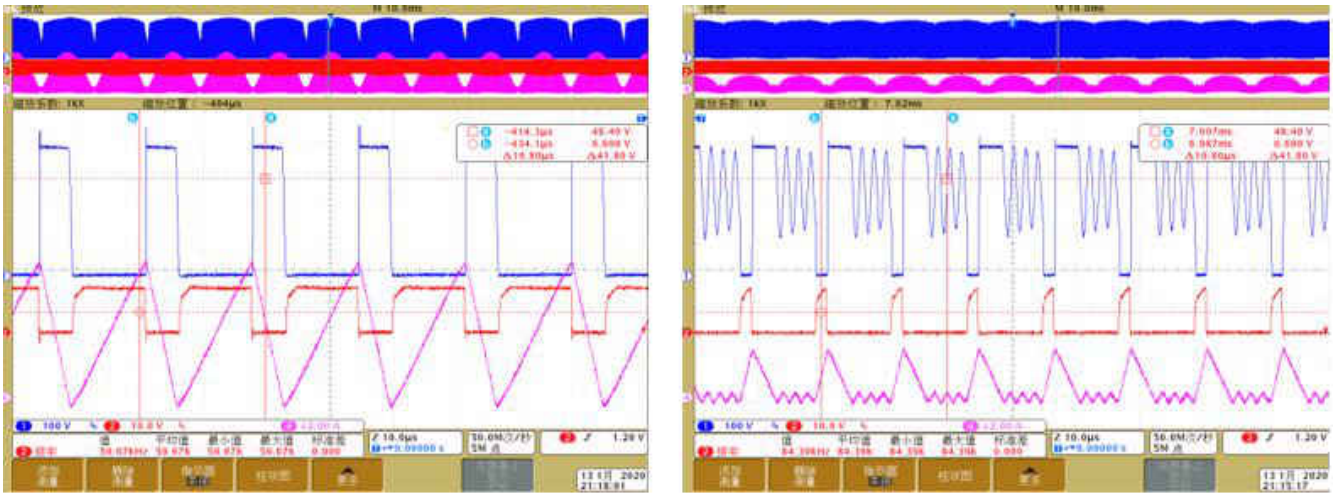


Figure 3-2. VDS vs ZCD/CS

To achieve a precise sampling of VDS from the ZCD/CS pin, follow the *ZCD/CS Pin* section in the *UCC28056 6-Pin Single-Phase Transition-Mode PFC Controller* data sheet to fine tune the amplitude of ZCD/CS to meet VDS.

3.2 How to Evaluate UCC28056 Normal Operation Mode Waveform?

The waveforms in Figure 3-3 show references for Critical Conduction Mode (CRM) and DCM.



Pink: PFC inductor current, Red: VGS of MOSFET, Blue: VDS of MOSFET

Figure 3-3. Normal Working Mode: CRM vs DCM

For a normal design, the controller works at CRM at low line input with heavy load condition, and working at DCM at high line input with light load condition.

4 Protections and how to Identify Them?

The UCC28056 controller includes a comprehensive list of fault-protection features such as cycle-by-cycle current limit, overcurrent protection, dual independent output overvoltage protection, line Brown-in, overtemperature protection, and bias-supply undervoltage lockout (UVLO).

Figure 4-1 shows all the protection features with the accompanying pin information.

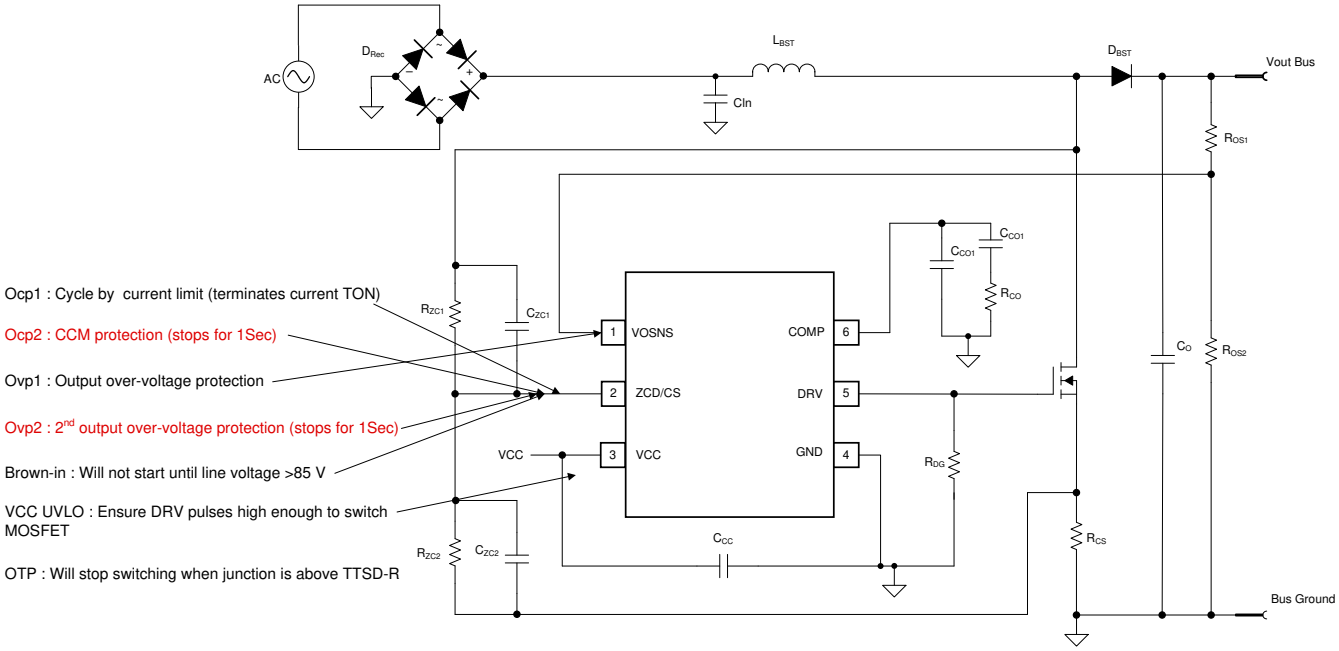


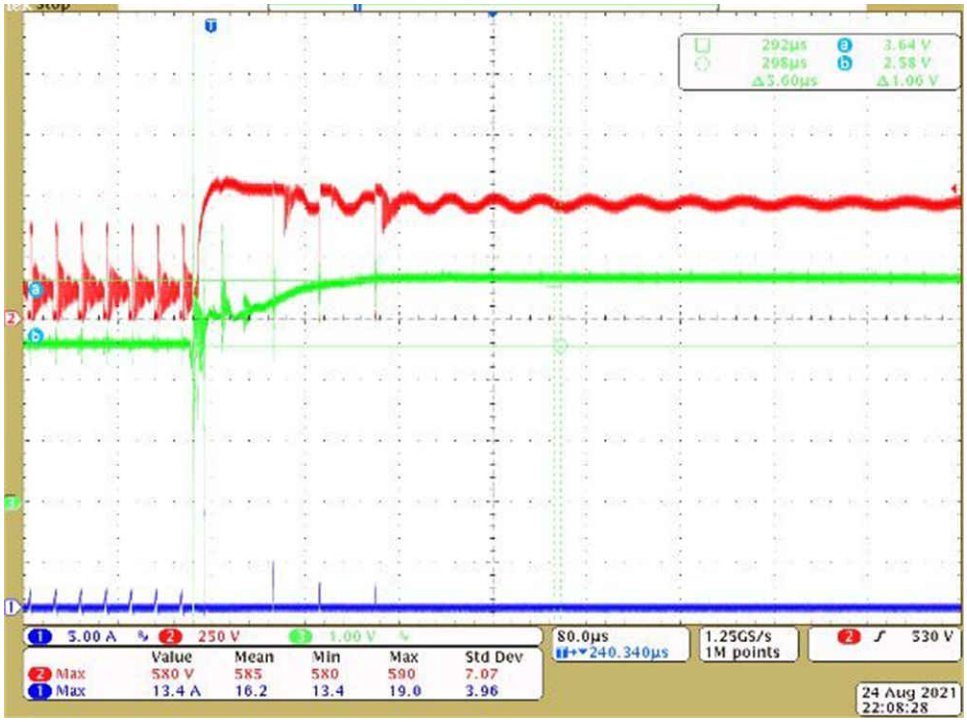
Figure 4-1. Protection Features

The following sections show the four most important protections in the controller, including O_{VP1}, O_{VP2}, O_{CP1}, and O_{CP2}.

4.1 O_{VP1}

The VOSNS pin monitors output capacitor voltage via an external resistor divider. An internal comparator (O_{VP1}) monitors the VOSNS pin voltage (V_{OS}). If the voltage on this pin rises above $V_{Ovp1Rise}$, indicating excessive output capacitor voltage, then the controller transitions to its BstOffb state. In this state switching halts to prevent further increase in the output voltage. The controller returns to the Runb state, and resumes switching operation, only after VOS falls below $V_{Ovp1Fall}$, indicating that the output voltage has returned to normal range.

The UCC28056A has 108% $V_{Ovp1Rise}$ which is less than the UCC28056B (110%) and UCC28056C (110%). The overshoot performance is better when using the UCC28056A, especially during start-up condition. The waveform in Figure 4-2 shows where the controller enters into O_{VP1}.



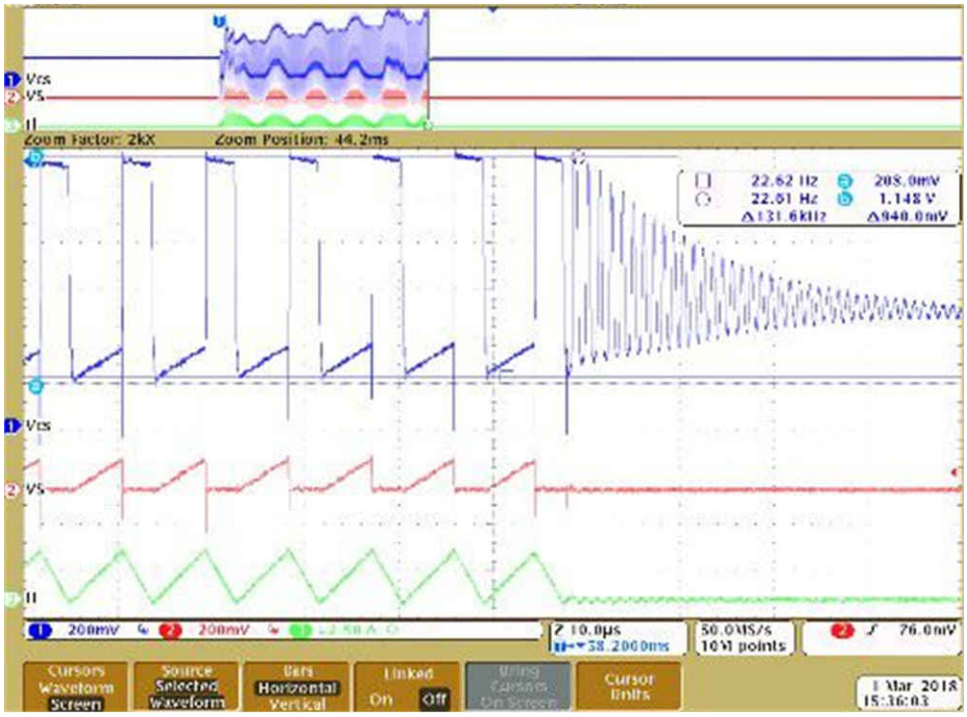
Green: V_{OSNS}, Blue: MOSFET Id

Figure 4-2. UCC28056 Triggers O_{VP1} Protection

4.2 O_{VP2}

An O_{VP2} comparator with a fixed threshold (V_{Ovp2Th}) monitors the ZCD/CS pin voltage during the TDCH period. A fixed blanking period ($T_{Ovp2Blk}$) is applied after the falling edge of the DRV waveform to ensure that the O_{VP2} comparator is not tripped by inductive spikes on the leading edge of the drain waveform.

The waveform in Figure 4-3 shows the controller entering into O_{VP2}.

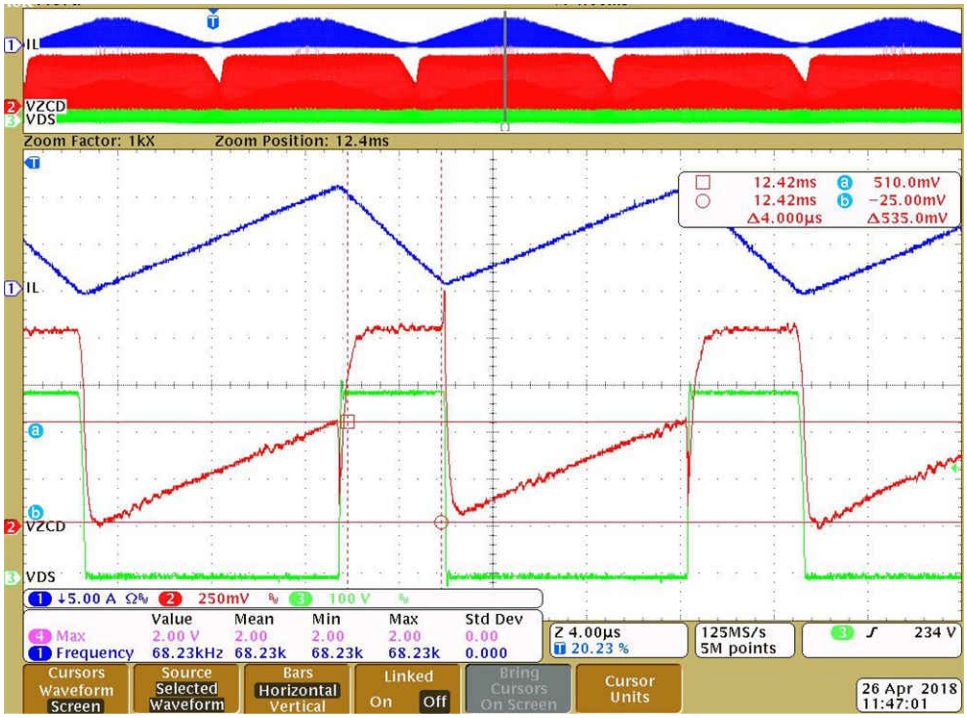


Green: PFC inductor current, Blue: ZCD/CS, Red: Voltage on current sense resistor

Figure 4-3. UCC28056 Triggers O_{VP2} Protection

4.3 O_{CP1}

Cycle-by-cycle peak current protection (O_{CP1}) terminates the on-time (T_{ON}) duration early if the current sense voltage rises above 0.5 V. This current protection method limits the peak inductor current, thus avoiding inductor saturation or damage to the power stage. The waveform in Figure 4-4 shows the controller enters into O_{CP1}. The O_{CP1} comparator is enabled from the DRV rising edge with a 450-ns blanking time.



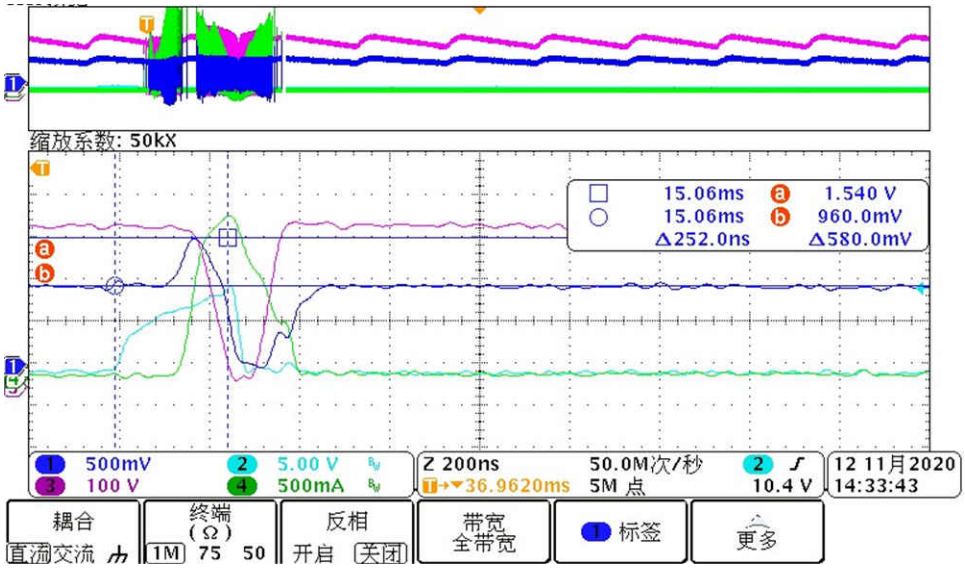
Red: ZCD/CS

Figure 4-4. UCC28056 Triggers O_{CP1} Protection

4.4 O_{CP2}

A second comparator (O_{CP2}) with a higher threshold, and shorter blanking time, also monitors the current sense voltage signal. If triggered, this second O_{CP2} comparator also terminates the current on-time (T_{ON}) duration early. In addition, if the controller triggers the O_{CP2} comparator on three consecutive switching cycles, it also triggers a long fault. The long fault halts switching operation and prevents restart for a period of $T_{LongFlt}$.

The ZCD/CS blanking time from DRV rising edge to Enable O_{CP2} Comparator Output is 250 ns. The waveform in Figure 4-5 shows where the controller enters into O_{CP2}.



Dark Blue: ZCD/CS; Light Blue: DRV

Figure 4-5. UCC28056 Triggers O_{CP2} Protection

The resistor between the controller DRV pin and MOSFET gate pin influences the turning on and off speed of the MOSFET. A higher value resistor can lower the turning on speed of the MOSFET and also helps on EMC performance. If the resistor value is too high, it may delay the VDS falling edge; therefore causing a delay on the ZCD/CS pin. If 250-ns blanking time is not enough for ZCD/CS falling down to correctly sampling current through the MOSFET, there may be a mis-triggering of O_{CP2}.

5 Application Debug Frequently Asked Questions (FAQs).

5.1 How is the UCC28056 GND Pin Connected?

TI recommends connecting the UCC28056 GND pin to the negative terminal of the RCS resistor. This is important because it provides good detection of the RCS current. Always try to connect the controller GND to the power circuit GND at only one point.

5.2 There is CCM Inductor Current During Start-Up, is This a Normal Phenomenon?

The CCM phenomenon is expected at the beginning of the start-up process. During this period, the peak output voltage is approximately equal to the line voltage; hence there is no different voltage to discharge the inductor current. In this region it is very difficult for the controller to detect the ZCD event; hence there is a very long OFF time. The strange switching operation is rapidly corrected once the output voltage has charged above the peak line voltage by a few volts.

5.3 How to Fine-Tune the RC Parameter on the ZCD/CS Pin?

TI recommends the RC constant time on the ZCD pin be no bigger than 100 ns. A longer RC time delay may result in an incorrect detection of MOSFET VDS and cause abnormal behavior from controller.

5.4 Is it Possible to Increase the High Voltage Cap Value on the ZCD Cap Divider?

It is possible to increase C_{ZC1} capacitor from 10pF to 30 pF, or even 100 pF to reduce the impedance of the ZCD/CS pin and make its resistive capacitive pickup better. In this case, the customer must also increase the C_{ZC2} capacitor by the same factor so that C_{ZC2} / C_{ZC1} = R_{ZC1} / R_{ZC2}. Since the C_{ZC1} capacitor does have some loss impact especially at high line operation, TI recommends the C_{ZC1} be no higher than 100 pF. For C_{ZC1} and C_{ZC2}, see UCC28056 Simplified Application.

5.5 How to Separate the T_{ONMAX} Limit or O_{CP} Protection When the PFC Output Voltage Cannot Follow the Regulated Voltage?

If O_{CP1} is limiting, it is easy to see that the peak PFC inductor current has a *flat* top around the peak of the line cycle. In this case T_{ON} < T_{ONMAX} around the peak of the line cycle but should still be T_{ONMAX} at the zero-crossing.

If T_{ONMAX} is limiting, you should see that the T_{ON} period is 12.8 µs and V_{COMP} is > 5 V.

5.6 Does UCC28056 Support DC Input Application?

DC operation of the UCC28056 is allowed, depending upon the application requirements. There will be some impact on the V_{FF} and Brown-in levels You may need to adjust the ZCD pin divide ratio to correct for this, and this will also affect the O_{VP2} level.

5.7 How Does RDG Change the Delay Time for Valley Switching Detection of the MOSFET?

During start-up, the UCC28056 will source a current I_{DG} from the DRV pin. After a delay (T_{DGSmpl}), it will detect the voltage on the DRV pin. This voltage level is used to set the valley delay. Only the effective resistance between DRV and GND is important.

5.8 Can UCC28056 Meet Harmonic Performance?

There are different requirements for IEC6100-3-2 from CLASS A to CLASS D. The UCC28056 is able to meet all CLASS A-D from this standard with a well-designed input filter circuit.

5.9 Does UCC28056 Have Soft Start?

There is no soft-start in the UCC28056. Only the COMP pin voltage is pulled down to GND via an internal 5-kΩ resistor to ensure it is discharged before start-up. The time required to boost up the VBUS should therefore depend mainly on the size of the bulk capacitor and the power capability of the PFC stage (PFC inductor value and RCS value) and if there is or is not a load on the output at start up process.

5.10 Does the UCC28056 Support Auxiliary-Winding PFC Inductor Input on the ZCD Pin?

Yes, the UCC28056 supports auxiliary-winding PFC inductor input on the ZCD Pin. Follow the *UCC28056x, Using Auxiliary Winding Voltage for Driving ZCD/CS Pin* application note .

6 References

- Texas Instruments, *UCC28056 6-Pin Single-Phase Transition-Mode PFC Controller* data sheet
- Texas Instruments, *UCC28056X Selection Guide*
- Texas Instruments, *UCC28056x, Using Auxiliary Winding Voltage for Driving ZCD/CS Pin* application report

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