Application Report

Large Duty Cycle Operation On the TPS563211

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ABSTRACT

The TPS563211 is a 3-A synchronous buck converter that operates from 4.2-V to 18-V input voltage, and 0.6-V to 7-V output voltage. The device employs AECM control, an emulated current control topology that combines the advantages of peak current mode control and D-CAP2 control, providing fast transient response with true fixed switching frequency.

With an on-time extension function, the device supports a maximum duty cycle of 98%. This application report introduces how the TPS563211 device is designed to implement large duty cycle operation.

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1 TPS563211 Introduction

The TPS563211 is a cost effective and highly flexible synchronous buck converter that provides selectable Eco-mode operation or FCCM (Force Continuous Conduction Mode) operation. Selectable Power-Good indicator or external Soft-Start is also configurable through the MODE pin. Power sequencing is possible by correctly configuring the Enable, Power-Good indicator or external Soft-Start. A wide input voltage range of 4.2 V to 18 V supports a wide variety of common input rails like 12 V and 15 V. It supports up to 3 A continuous output current at output voltages between 0.6 V and 7 V.

The device provides fast transient response with true fixed switching frequency through the use of the Advanced Emulated Current Mode (AECM) control topology. With internal smart loop bandwidth control, the device provides fast transient response over a wide output voltage range without the need for external compensation.

2 TPS563211 Control Architecture

2.1 AECM Control on TPS563211

AECM is a new topology based on a fixed-frequency modulator with emulated current information for the loop control, combing the fixed frequency of PCM control and the fast load-transient response of the D-CAP2 control topology. The key features and benefits of AECM include:

- True fixed-frequency modulation that can simplify EMI filter design and make it easy to achieve high-frequency modulation such as 2.1 MHz.
- An emulated ramp-generator circuit with smart loop-bandwidth control that can adjust the DC gain smartly, supporting wide-output and large-duty-cycle applications with good load-transient performance.

Figure 2-1 shows the detailed control block diagram in the TPS563211 design.

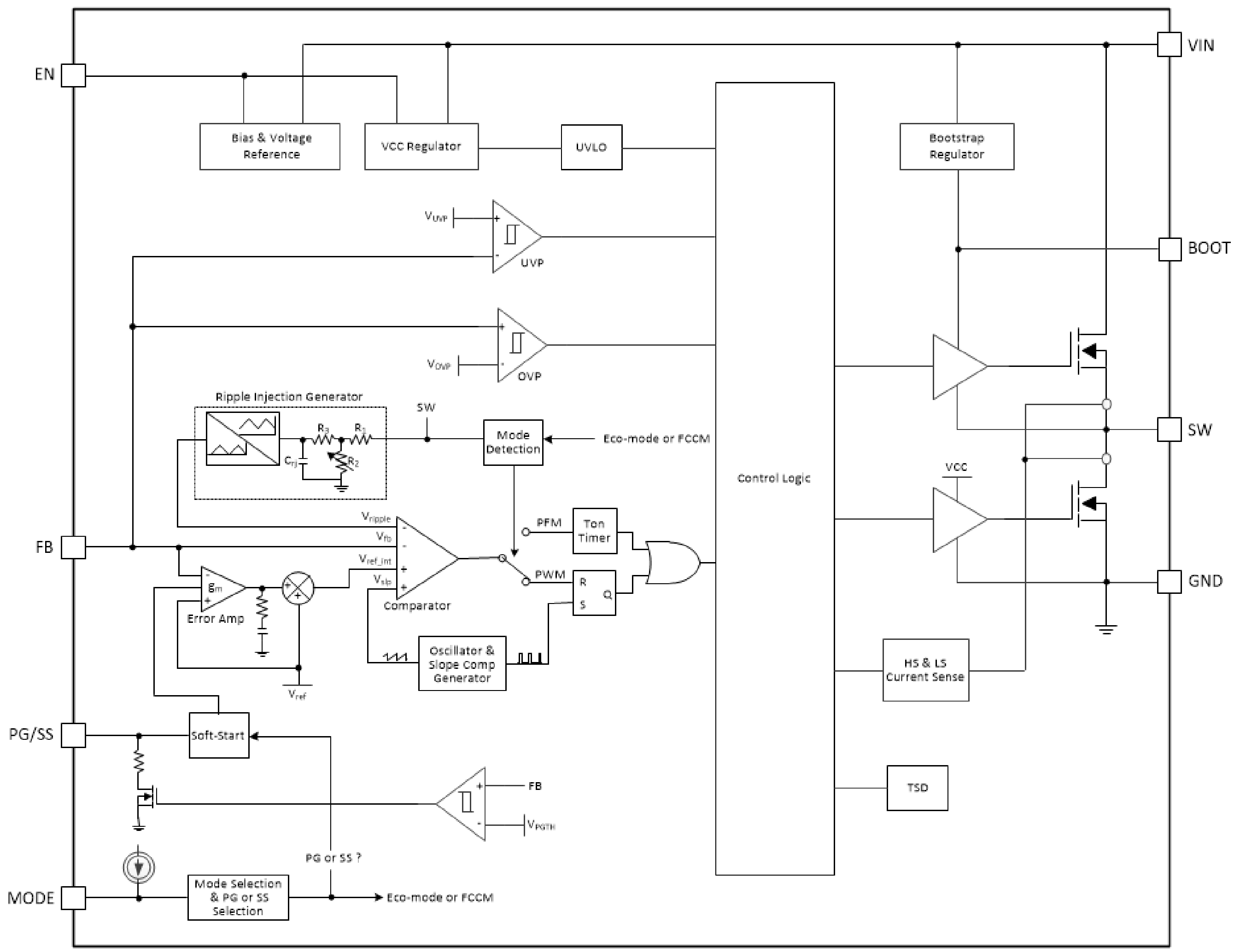

Figure 2-1. TPS563211 Functional Block Diagram

To improve noise immunity with virtually no ripple on the output voltage, an additional RAMP is added. An included error amplifier makes the output voltage very accurate.

In the control block of the TPS563211 device, the inductor valley current is monitored by measuring the SW node voltage during low-side MOSFET ON-time, which leads a minimum off time requirement for the high-side MOSFET. When the ON timer is expired, the high-side MOSFET is turned off and the low-side MOSFET is turned on. The turning off of the high-side MOSFET causes the SW ringing. When measuring the SW node voltage, a time delay needs to be included to let the internal SW node ringing dissipate. This time delay results in the minimum off time for the high-side MOSFET.

$$D = \frac{T_{ON}}{T_{SW}} = 1 - \frac{T_{OFF}}{T_{SW}} = 1 - F_{SW} \times T_{OFF} \tag{1}$$

Based on Equation 1, since Toff has a minimum value, it follows that the duty cycle, D, has a maximum value. If the F_{SW} is fixed, a smaller $T_{OFF(min)}$, means a larger duty cycle can be supported. Alternatively, if the $T_{OFF(min)}$ is fixed, a larger duty cycle can be supported with a smaller F_{SW}.

In the TPS563211 device, the minimum off time of low-side MOSFET is 105 ns and the maximum on time is 6 μs which result in a maximum duty cycle of about 98% during normal operation.

2.2 AECM Control Principle

There are two basic operation modes, PWM mode and PFM mode, selectable by the mode detection block. The integrator in the voltage loop can improve output-voltage accuracy issues. The integrated oscillator generates the fixed clock. Implementing slope compensation in the modulator avoids subharmonic oscillation when the duty cycle is higher than 50% in PWM mode. The emulated ramp generator with the smart loop-bandwidth control circuit can adjust the DC gain to achieve high bandwidth over all output rails. And even though there is an integrator, unlike PCM control, the integrator in AECM control can improve output-voltage accuracy with no direct impact on loop response speed.

The PWM mode control scheme is similar to PCM control. As shown in Figure 2-2 on the following page, the internal clock initials one on-pulse; the high-side FET then turns on, with current increasing in the inductor. When the emulated ramp voltage, feedback voltage and slope compensation voltage reach the integrated reference voltage, the high-side FET turns off and the low-side FET turns on until the next clock cycle. Therefore, in PWM mode, the switching frequency is truly fixed.

AECM control implements PFM mode to achieve high efficiency under light loads. With a load current decrease, the device enters into discontinuous conduction mode (DCM) from continuous conduction mode (CCM). In both modes, the switching frequency is fixed; the width of the on-pulse (Ton) depends on the load current. Lighter loads have a shorter Ton. AECM has an on-time generator like the D-CAP2 control topology, but that generator is disabled in PWM mode. With the load current further decreasing, the Ton decreases down to the internal clamped on-time, while the AECM device steps into PFM mode with the internal clock blocked and the on-time generator enabled. As shown in Figure 2-2, the control scheme of PFM mode is similar to the D-CAP2 control scheme.

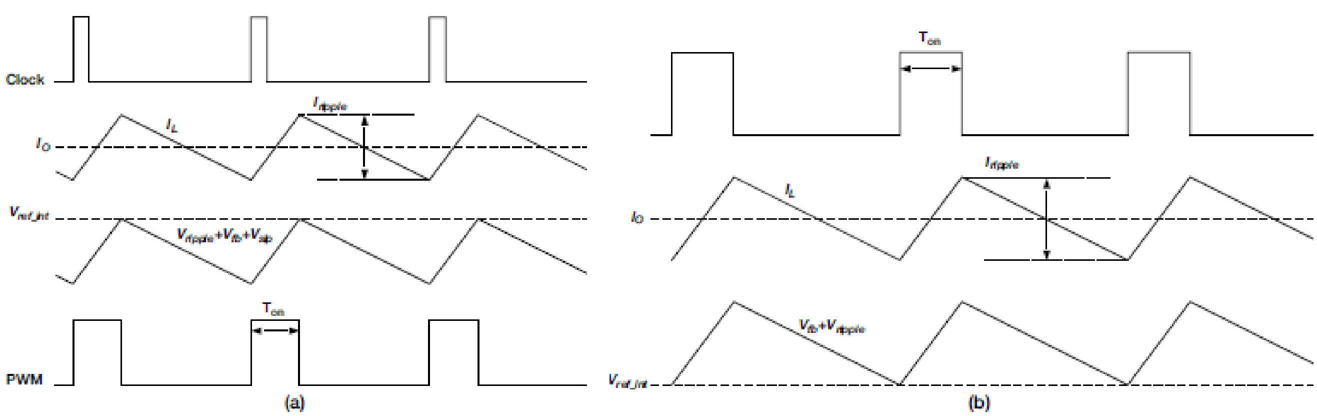

Figure 2-2. AECM Control Scheme Waveform: PWM Operation Mode (a); PFM Operation Mode (b)

3 Large Duty Cycle Operation in the TPS563211

3.1 On-Time Extension Function

To support higher duty cycle operation when V_{IN} close to V_{OUT}, the TPS563211 includes an On-Time Extension function. This function operates by increasing the HSFET On-Time beyond that during normal operation, thus lowering the operating frequency and allowing large duty cycles to be maintained.

Minimum on-time, T_{ON_MIN}, is the smallest duration of time that the high-side MOSFET can be on. T_{ON_MIN} is typically 45 ns in the device. Minimum off-time, T_{OFF_MIN}, is the smallest duration that the high-side MOSFET can be off. T_{OFF_MIN} is typically 105 ns in the device. In CCM operation, T_{ON_MIN} and T_{OFF_MIN} limit the voltage conversion range given a fixed switching frequency.

The minimum duty cycle allowed is:

$$D_{MIN} = T_{ON\_MIN} \times f_{SW} \tag{2}$$

The maximum duty cycle allowed is:

$$D_{MAX} = 1 - T_{OFF\_MIN} \times f_{SW} \tag{3}$$

In the device, a frequency foldback scheme is employed to extend the maximum duty cycle when T_{OFF_MIN} is reached. The switching frequency decreases once longer duty cycle is needed under low VIN conditions. With the duty increased, the on-time is extended until up to the maximum on-time, 6 µs. Wide range of frequency foldback allows the device output voltage stay in regulation with a much lower supply voltage VIN. This leads to a lower effective dropout voltage.

Given an output voltage, the maximum operation supply voltage can be found by:

$$V_{IN\_MAX} = \frac{V_{OUT}}{f_{SW} \cdot T_{ON\_MIN}} \tag{4}$$

At lower supply voltage, the switching frequency decreases once T_{OFF_MIN} is triggered. The minimum VIN without frequency foldback can be approximated by:

$$V_{IN\_MIN} = \frac{V_{OUT}}{(1\text{-}f_{SW} \cdot T_{OFF\_MIN})} \tag{5}$$

Taking considerations of power losses in the system with heavy load operation, V_{IN_MAX} is higher than the result calculated in Equation 4.

If decrease this V_{IN_MIN} voltage, The device would allow periodic switching after trigger min off time. And the on-time is extended until up to the maximum on-time, 6 µs typical, with the duty increased.

Based on 6 us maximum on-time and 105 ns minimum off-time, we can get a real maximum duty, 98%, thanks to this frequency foldback scheme.

3.2 TPS563211 EVM Bench Test

The bench tests are done on the TPS563211EVM. For details, see the *TPS563211EVM Evaluation Module User's Guide*. The bench test setup and configuration is listed inTable 3-1 .

Table 3-1. Bench Setup for TPS563211

V_{OUT}(V)	L (µH)	Cout (µF)	Rtop (kΩ) / R9	Rbot (kΩ) / R8	Mode
5	4.7	2× 22 µF (0805, 10 V)	73.2	10	FCCM / 600 kHz

The waveforms in Figure 3-1 to Figure 3-4 show the behaviors with and without the ON-time extension function triggered. Table 3-2 lists the summary for the figures.

Table 3-2. Summary for TPS563211 On-Time Extension Bench Test

V_{OUT} (V)	Figure	I_{OUT} (A)	V_{IN} (V)	V_{OUT} / V_{IN} Condition	T_{ON} Condition	F_{SW} (kHz)
5.09	Figure 3-1	0	6	84%	Without ON-time extension, T_{ON}=1.38uS	601
5.08	Figure 3-2	3	5.79	87.7%	With ON-time extension, T_{ON}=1.9uS	329
5.09	Figure 3-3	0	5.18	98.3%	With ON-time extension,T_{ON}=6uS	166
5.07	Figure 3-4	3	5.55	91.4%	With ON-time extension,T_{ON}=6.5uS	153

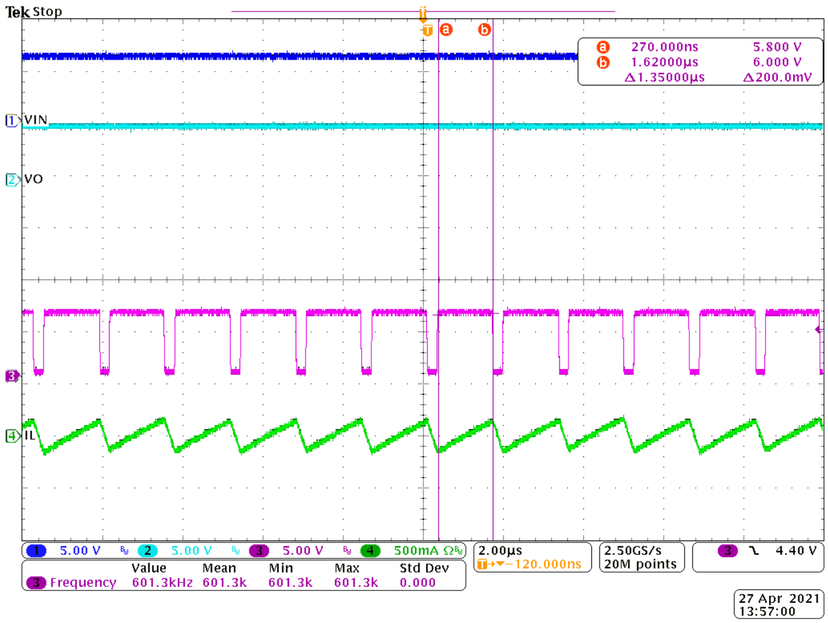

Figure 3-1. 6Vin-5Vout-0A

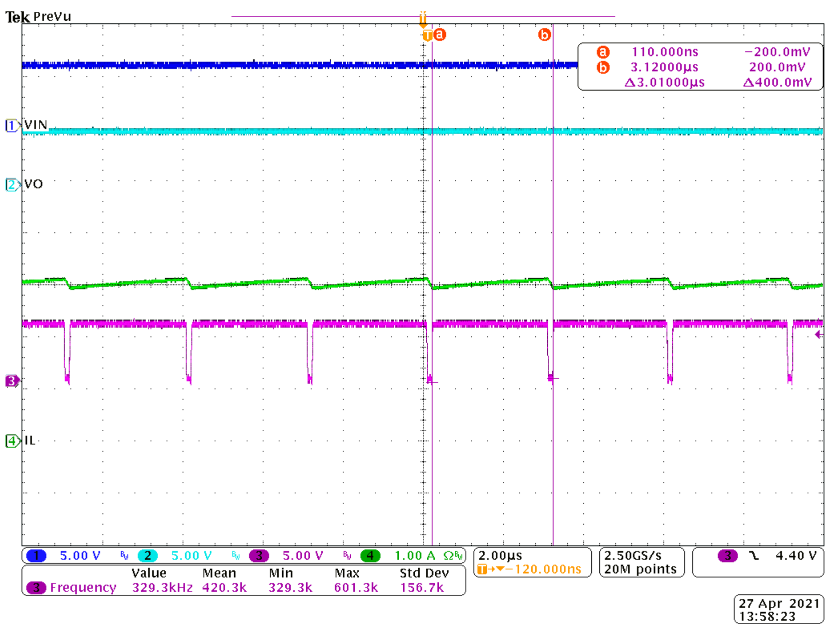

Figure 3-2. 6Vin-5Vout-3A

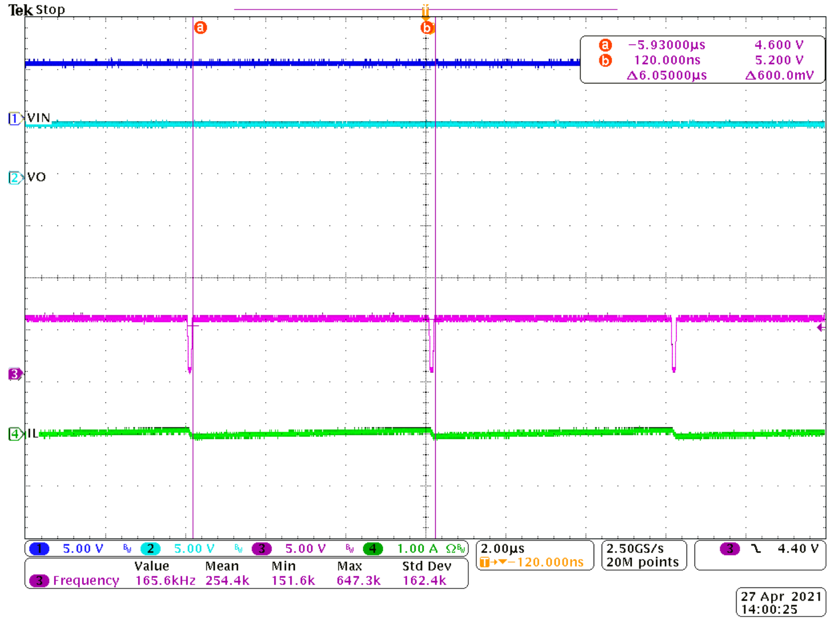

Figure 3-3. 5.1Vin-5Vout-0A

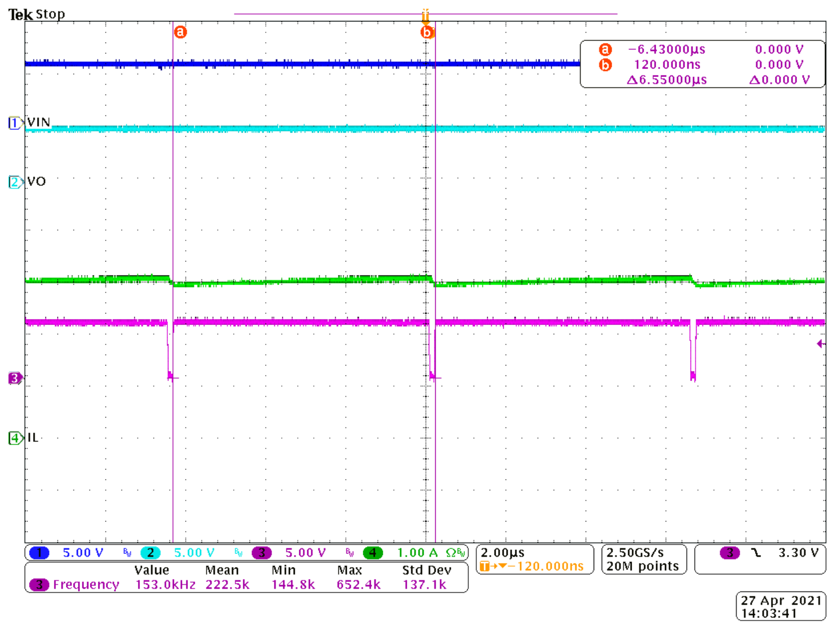

Figure 3-4. 5.5Vin-5vout-3A

3.3 Summary for Bench Test Results

With On-Time Extension triggered, when loading is added to 3 A, the maximum duty cycle drops. This is caused mainly by the power loss of the $R_{DS(ON)}$ of the HSFET and LSFET, and the power loss of the DCR of the external inductor.

With frequency foldback, V_{IN_VIN} is lowered by decreased f_{SW}, as shown in Figure 3-5.

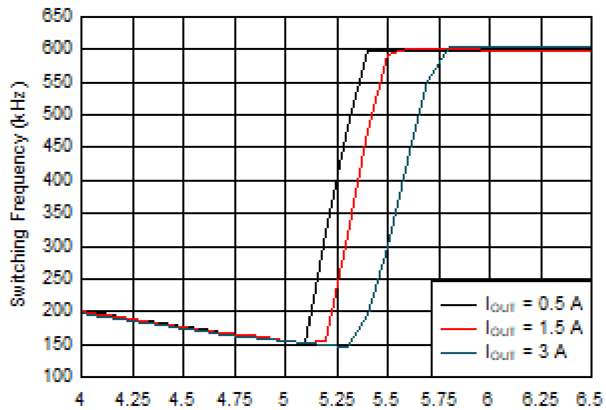

Figure 3-5. Frequency Foldback at Dropout (V_{OUT} = 5 V)

4 Summary

The TPS563211 device employs AECM control, an emulated current control based topology that combines the advantages of peak current-mode control and D-CAP2 control, providing fast transient response with true fixed switching frequency. AECM builds in the On-Time Extension function to support large duty cycle operation up to 98%.

5 References

1. Texas Instruments, *TPS563211 4.2-V to 18-V Input, 3-A Synchronous Buck Convertor in SOT583 Data Sheet*.
2. Texas Instruments, *TPS562211 4.2-V to 18-V Input, 2-A Synchronous Buck Convertor in SOT583 Data Sheet*.
3. Texas Instruments, *Achieving Fast Load-Transient Response and Low EMI with the AECM DC/DC Control Topology*.
4. Texas Instruments, *TPS563211EVM Evaluation Module User's Guide*.
5. Texas Instruments, *TPS562211EVM Evaluation Module User's Guide*.

6 Also From TI

The TPS562211 device is a 4.2-V to 18-V input voltage range, 2-A synchronous buck converter, and 0.6-V to 7-V output voltage. This device also employs AECM control with the same ON-time extension function to support large duty cycle operation up to 98%.

The TPS56339 devices is a 4.5-V to 24-V input voltage range, 3-A synchronous buck converter, and 0.8-V to 16-V output voltage. This device also employs AECM control with the same ON-time extension function to support large duty cycle operation up to 97%.