Application Report
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UCC2806x PCB Layout Guideline for PFC

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ABSTRACT

This application report describes the optimized layout for the UCC2806x family (such as UCC28064A and UCC28063A) of interleaved transition mode PFC controllers for AC/DC power design. The purpose of a good layout is to minimize parasitic effects which can degrade and potentially prevent proper operation. This guide shows how to properly place external components and route PCB traces around UCC2806x to achieve best performance. Though not covered by this layout guide, similar principles can be applied to the PCB layout for other PFC controllers, such as UCC28070A, UCC28180, UCC28056, and so forth.

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1 Typical Application Circuit

Figure 1 and Figure 2 show a typical application circuit for the UCC2806x with the component names used in this layout guideline.

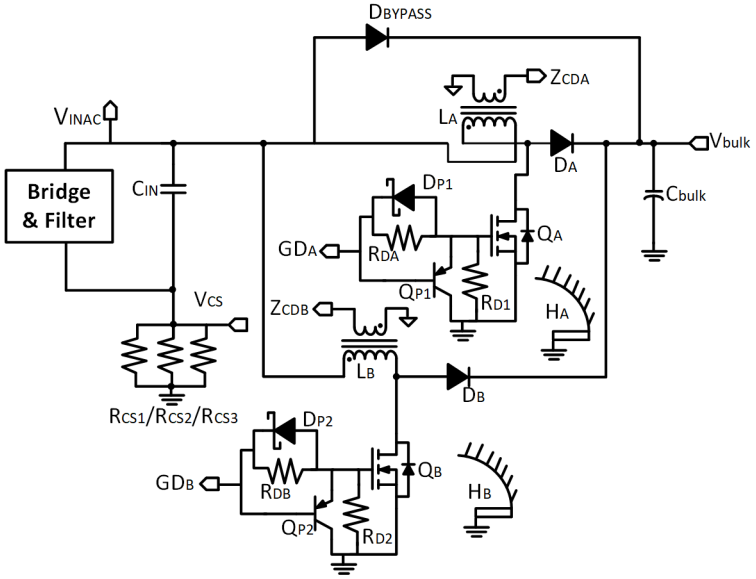

Figure 1. PFC Power Stage

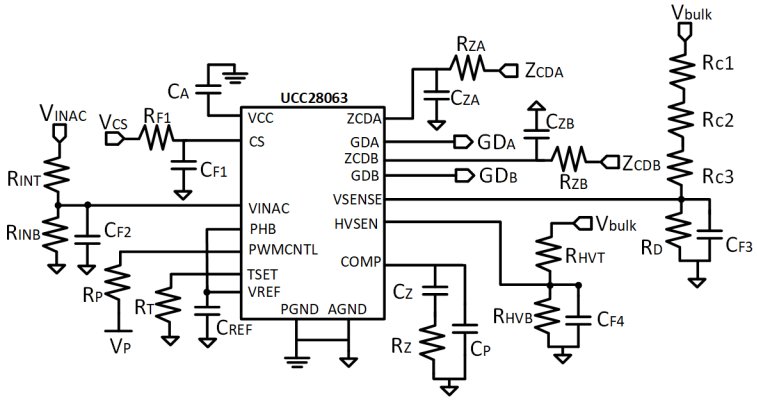

Figure 2. PFC Device Shematic

2 Layout Procedure

2.1 RTSET and VSENSE

The most sensitive external component is the TSET resistor. TSET is used to set maximum on-time to limit maximum power that can be delivered by the input for a given boost inductance. Minimize TSET stray capacitance to any other node that can have high voltage dv/dt on it. Place the resistor as close to device as possible and terminate to AGND.

The VSENSE path is used to feedback bulk voltage. It should be placed close to the device and terminate to AGND as shown in Figure 3. Choose the VSENSE resistance to keep standby power low. Choose CF3 to get RC ≤ 100 µs for good filtering. Too much filtering on VSENSE delays the feedback, slows reaction to transient conditions, and may amplify ripple on the output voltage (V_{out}).

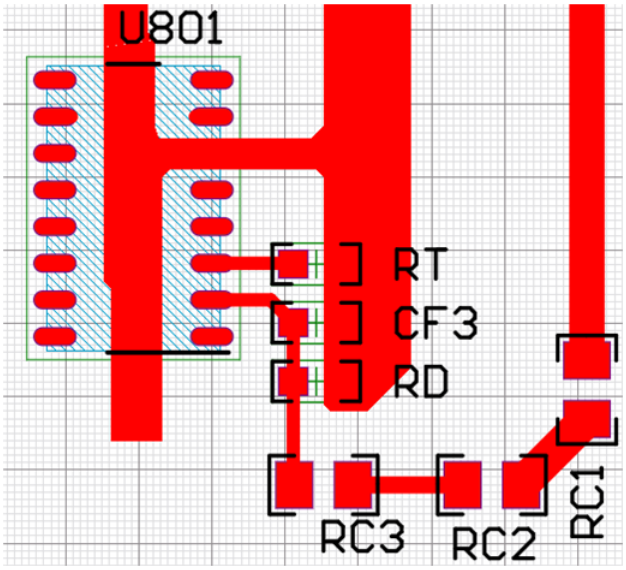

Figure 3. TSET and VSENSE Layout

2.2 ZCD Filter

RZx is chosen to limit max negative current (out of the ZCDx pin) per the datasheet ABS MAX specification. CZx is chosen to tune the turnon timing to achieve optimal valley switching. It is not recommended to connect the filter GND to the convenient local GND since high di/dt and surge through inductance injects noise to ZCD signal. Locate the ZCDx filter capacitor and resistor close to device and terminate to AGND. Minimize the loop area of ZCDx signal tracks by keeping the ZCD-winding tracks very close and parallel to each other and bringing the GND return track all the way back to the IC along with ZCDx track.

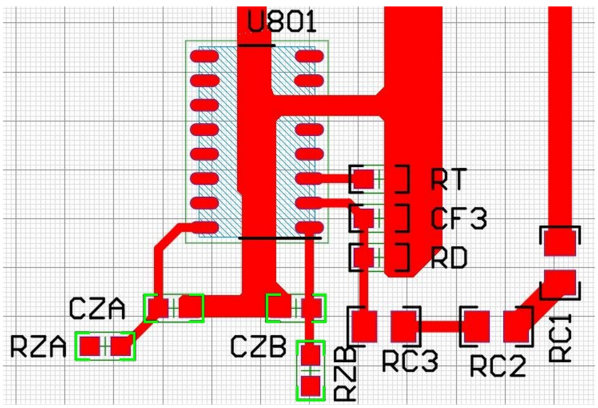

Figure 4. ZCD Filter Layout

2.3 VREF

VREF is the output that supplies internal circuits and provides a well-regulated reference voltage to the circuit. The output is suggested to be bypassed to PGND with a low impedance 0.1 µF capacitor or place a larger capacitor close to VREF pin. This provides the shortest path to bypass noise on the internal circuit and goes to the VCC capacitor.

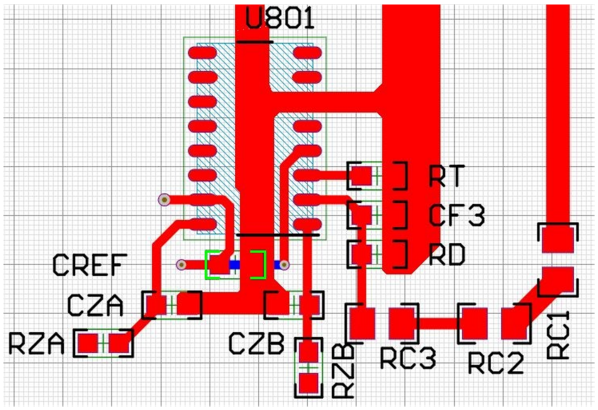

Figure 5. VREF Layout

2.4 COMP and PHB

Compensation components RZ, CZ, and CP are noise sensitive. Minimize the distance between RZ, CZ, and CP and keep them as close as possible to the UCC2806x controller. These components must terminate to AGND.

The PHB can directly connect to VREF if it is required to have both phases always on. The PHB input can be connected to COMP to implement automatic phase-shedding, or it can connect to the external circuit for specialized phase control.

If a wire jumper is undesirable, use the 0805 or 1206 package for RZ to use as a jumper over the GND copper, or use a 0-Ω resistor as a jumper.

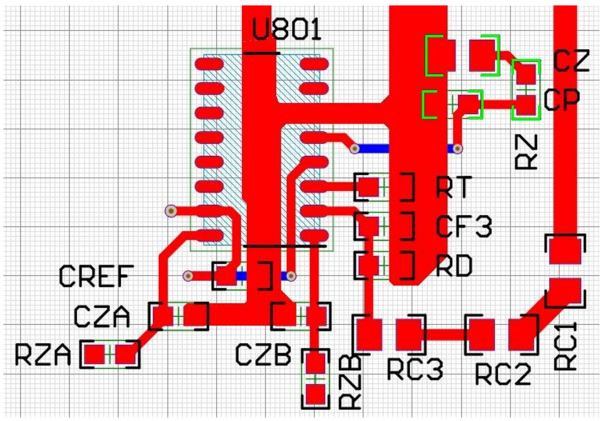

Figure 6. COMP and PHB Layout

2.5 VINAC and HVSEN

Input power line voltage sensing at VINAC determines when the system PFC is in setup and shutdown mode. The VINAC pin also implements dropout detection. It is often the case that the ac-line voltage momentarily drops to zero or nearly zero, due to transient abnormal events affecting the local ac power distribution network. It is recommended to filter the VINAC by the RC, but avoid excessive filtering of the VINAC signal, or dropout detection may be delayed or defeated. An RC time-constant of ≤ 100 µs should provide good performance. Place the VINAC filter as close to the device as possible and terminate to AGND.

HVSENS is the second order OVP. HVSEN can be filtered more than VSENSE and VINAC, but not so much filtering as to result in significant overvoltage stress to the buck capacitor before shutdown. In order to maintain low power consumption, the impedance of the sense path is high. VINAC and HVSEN can be sensitive to noise. The traces connecting to VINAC and HVSEN should not cross the high dv/dt area. To avoid picking up switching noise, bring raw high voltage (HV) signal sources toward the control area and then divide down. Do not place divider resistors in the HV area and route low voltage (LV) signal a long distance through the HV areas.

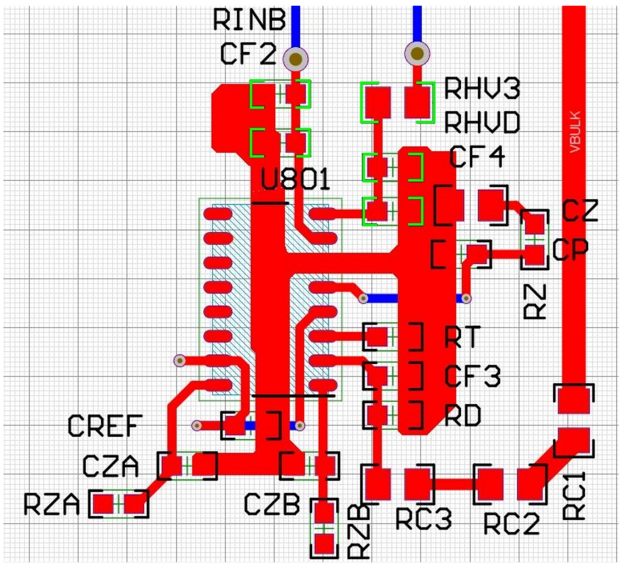

Figure 7. VINAC and HVSEN Layout

2.6 Current Sense Filter, Vcc Cap, and PWMCTL

UCC2806x uses a resistor to continuously sense the combined total inductor (input) current. As the input current increase, the voltage on CS goes more negative. This cycle-by-cycle overcurrent limits input current by turning off both gate drive output (GDx) when CS is more negative than -200 mV in two-phase operation and -167 mV in single-phase operation. RF1 is used to limit the magnitude of negative current out of the CS pin when the power-on inrush surge current develops a high voltage across the sense resistor. CF1 forms an RC filter with RF1 and is chosen to suppress switching noise at the CS pin.

Heavy filtering of CS delays sensing of current peaks and may result in excess output power before OCP, or even saturation of the boost inductor (Lx) if there is an insufficient design margin. It is recommended to have an RC time constant at the CS input of 100 ns to 200 ns.

The current sense filter, RF1 and CF1, should be as close to the device as possible. Connect all control and sense signal parts to AGND. If possible, run the VCS signal and GND in parallel from Rcs to IC (like ZCDx signal). Nearby filtering of CS delays peak. The VCC capacitor, CA, should be placed close by the VCC pin and PNG. Connect the analog and power grounds at a single point to isolate high current noise signal of the power components from interference with low current circuits.

PWMCTL is used to enable PHB. Pull up RP with VCC by 100 kΩ if always enabled or external circuit for custom phase management.

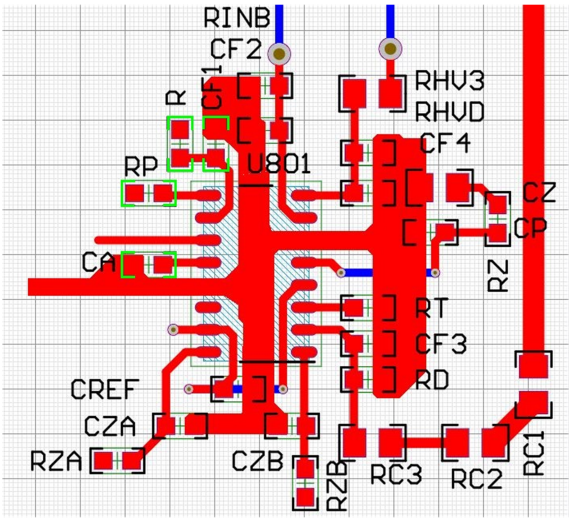

Figure 8. Current Sense Layout

2.7 Power Loop

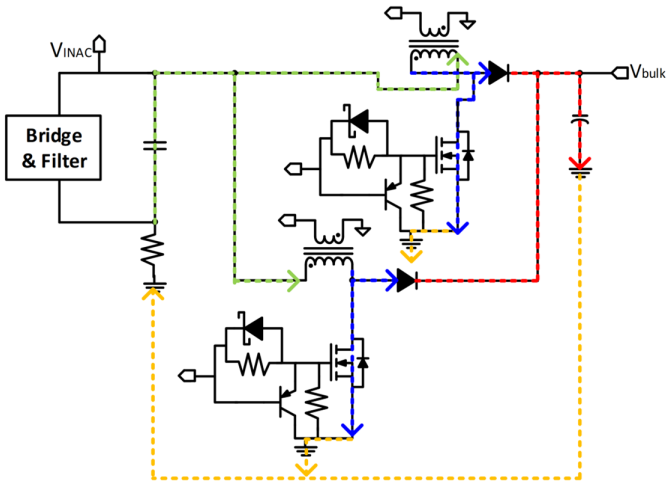

Figure 9. Power Loops of PFC

As shown in Figure 9, there are four loops in PFC design. The green line is the input current loop, the blue line is the switching loop, the red line is the output current loop, and the orange line is the power ground return loop. The following suggestions are general layout concepts and considerations for PFC, especially single layer design.

In order to make layout easier, the PFC choke polarities are different. To minimize the interference caused by inductive coupling from the boost inductors, the UCC2806x controller should be located at least 1 inch (25.4 mm) away from the boost inductors.

- **Input current loop:**
  - To maximize the benefits of interleaving, the input and output capacitors should be located before and after the two phase currents depart and are combined together.
- **Switching loop:**
  - Minimize the switching loop area to achieve better EMI and reduce noise.
- **Output current loop:**
  - Since the current flowing through the bulk capacitor is pulse type, minimize the trace between the diode to the bulk capacitor.
- **Power ground return loop:**
  - The AGND and PGND should be connected somewhere. TI recommends connecting it underneath the IC from pin 6 (AGND) across to pin 13 (PGND). In order to keep high current signal out of AGND, terminate current sense RCS ground and bulk capacitor ground to pin 13.
  - The gate drive ground return path should be minimized.

3 Layout Example

Figure 10 shows the combined layout example based on rules described in Section 2.

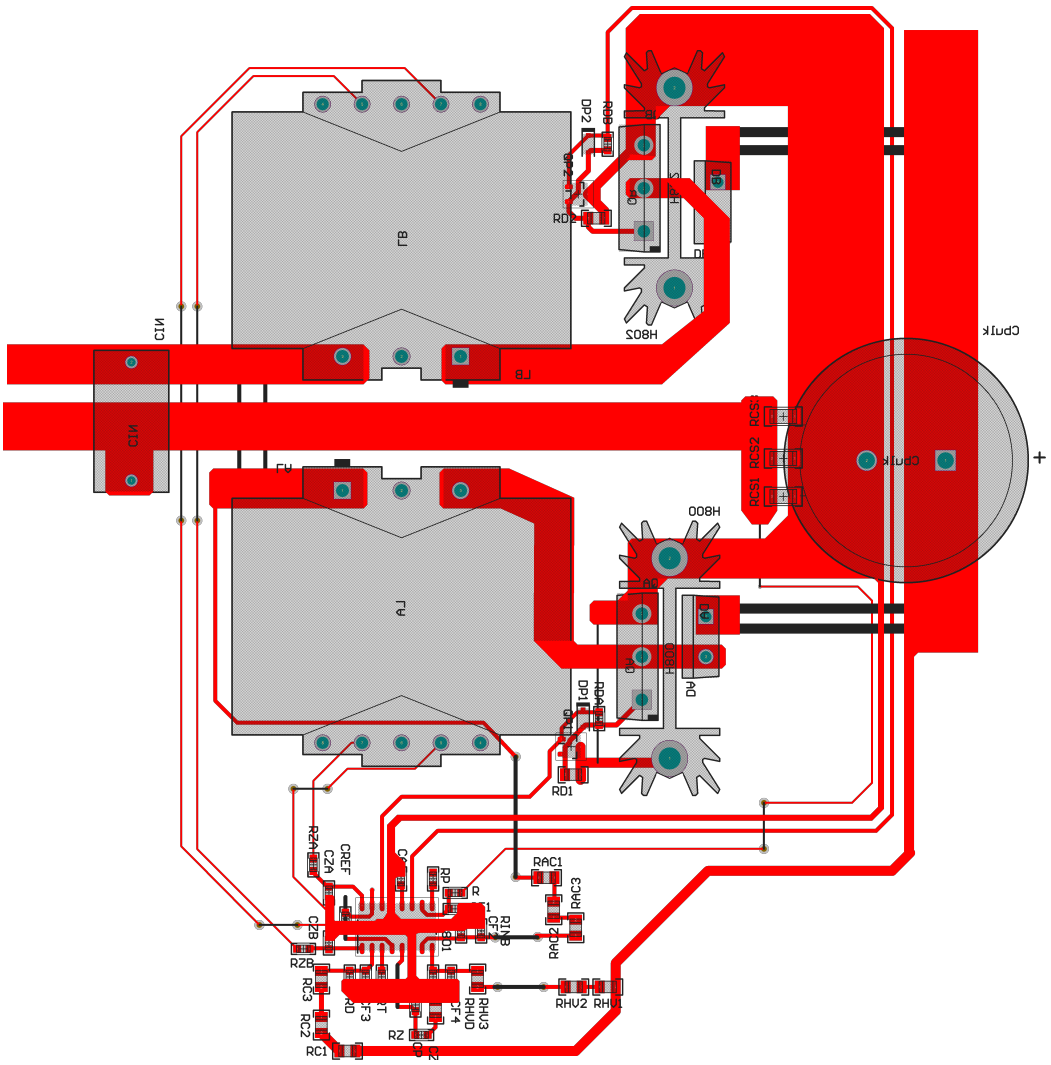

Figure 10. Layout Example with UCC28063

4 References

- Texas Instruments, *UCC28063A Natural Interleaving™ Transition-Mode PFC Controller With Improved Audible and Input Surge Noise Immunity Data Sheet* (SNVSA88)
- Texas Instruments, *UCC28064A Natural Interleaving™ Transition-Mode PFC Controller with High Light-Load Efficiency Data Sheet* (SLUSC60)
- Texas Instruments, *UCC28070A Extended Frequency Range (10 kHz to 300 kHz), Interleaving Continuous Conduction Mode PFC Controller Data Sheet* (SLUSAW0)

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