Application Report
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Common-Mode-Chokeless Bias Supply Reference Design Example

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ABSTRACT

This document aims to educate the reader on the design procedure of the PMP21022 reference design so that the reader can design using TI's UCC28722 for his or her own applications.

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Trademarks

1 Introduction

The PMP21022 is a TI bias supply reference design with an output rated for 12 V, 0.85 A that supports an input range of 102–138 V_{RMS}. The design features TI's UCC28722 – a constant-voltage, constant-current BJT drive flyback controller that features primary-side regulation, eliminating the need for a feedback optocoupler. Rather, an auxiliary winding on the transformer and information from the power switch are used to provide control of output voltage and current. The PMP21022 design passes class B conducted EMI without a common mode choke, reducing the cost of the design, although a shielded transformer would be recommended to reduce noise. Cable compensation is not utilized in this design.

2 Simplified Application Circuit

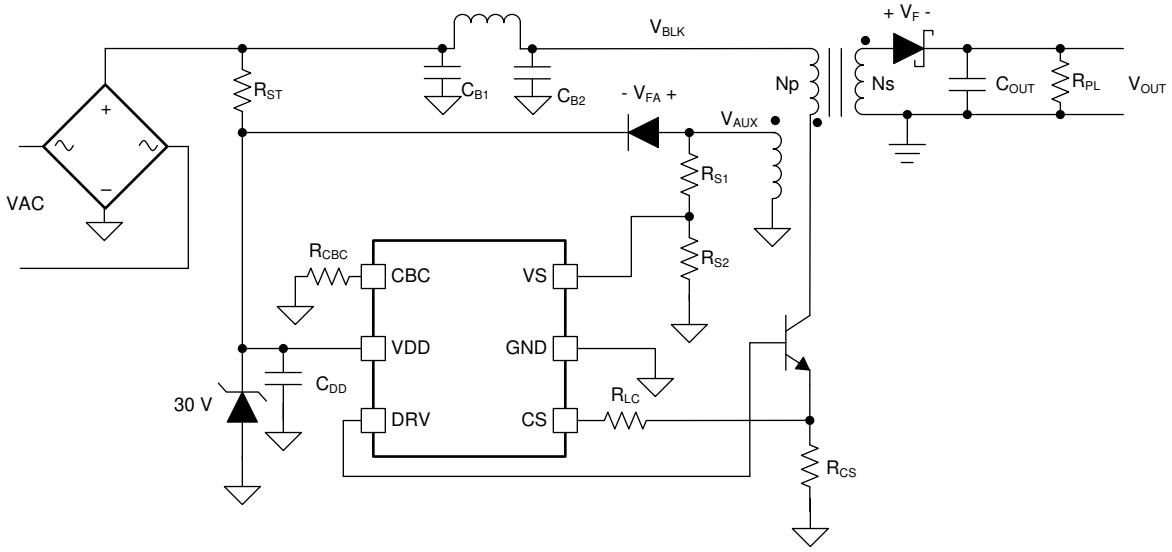

Figure 1. Simplified Application Circuit

Figure 1 is a simplified application circuit that presents the naming convention used throughout the rest of the document. The labels of the various values here refer to the corresponding values on the PMP21022 schematic in Figure 2.

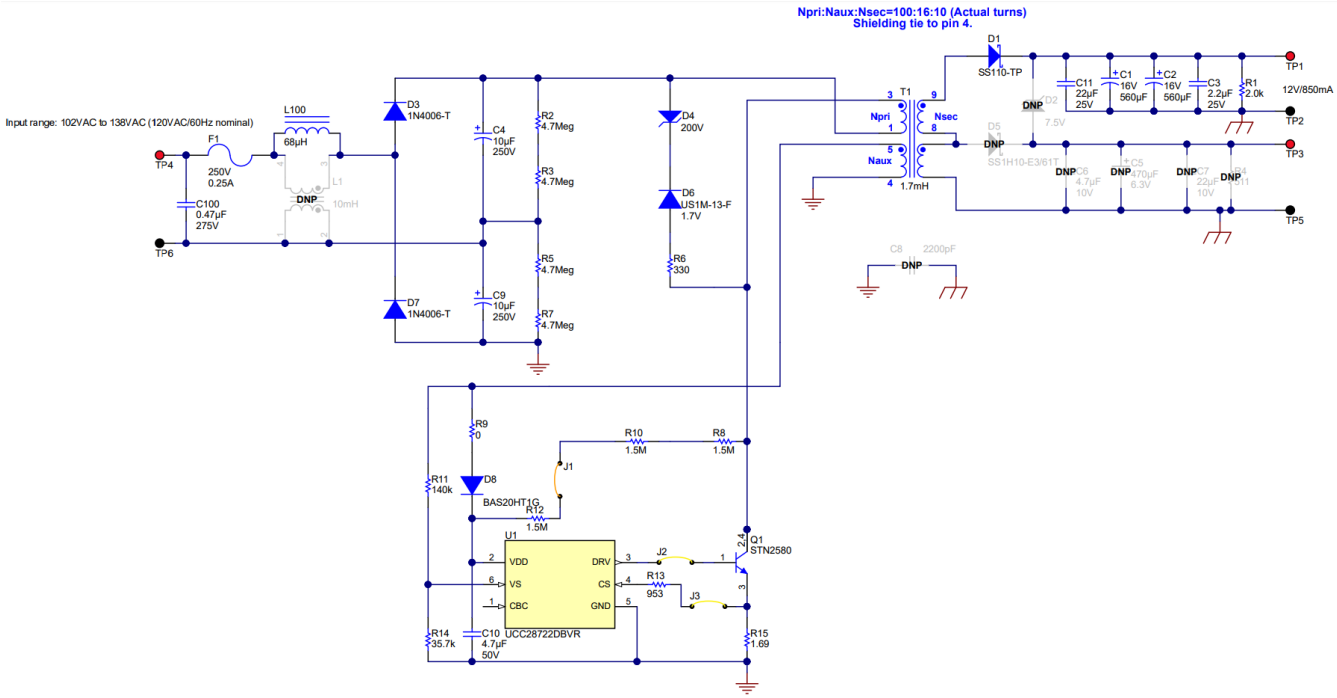

Figure 2. PMP21022 Schematic

3 Design

3.1 Input EMI Filter and Voltage Doubler

The input LC filter is used to attenuate the differential mode noise generated by the flyback converter. There are two methods of determining the necessary L and C values. The first is to utilize a simulation model including the parasitics to evaluate noise performance. The other is to measure the EMI and iterate the LC values until the desired performance is reached. The PMP21022 reference design was designed with the latter approach, as it was designed without a simulation model.

The voltage doubler at the input can reduce the primary RMS current of the converter, allowing a reduction in the size of the transformer.

3.2 Transformer Turns Ratio

The maximum primary-to-secondary turns ratio is dependent upon the maximum switching frequency at full load, the minimum input voltage, and the estimated DCM quasi-resonant time. The quasi-resonant time is the time from the end of the transformer demagnetization period to the first valley of the V_{CE} voltage. The DCM resonant time can be assumed to be 500 kHz if there is no estimate from previous designs.

First, determine the maximum available duty cycle of the on time and secondary conduction time. Here, D_{MAGCC} is defined as the secondary diode conduction duty cycle during constant-current operation. It is internally set to 0.425 by UCC28722.

- From the data sheet, t_r = 2 µs
- f_{max} = 60 kHz
- From data sheet, D_{MAGCC} = 0.425

$$D_{max} = 1 - \left(\frac{t_R}{2} \times f_{max}\right) - D_{MAGCC} = 1 - \left(\frac{60 \times 10^3}{2 \times 500 \times 10^3}\right) - 0.425 = 0.515 \quad (1)$$

The maximum primary-to-secondary turns ratio is limited by D_{max}. Here, V_F is the forward voltage drop of the secondary rectifier (SS110-TP). $V_{in,min}$ is the minimum input voltage to the converter.

- $V_{in,min}$ = 200 V
- V_F = 0.85 V

$$N_{ps,max} = \frac{V_{in,min} D_{max}}{\left(V_{out} + V_F\right)\left(1 - D_{max}\right)} = \frac{200 \times 0.515}{\left(12 + 0.85\right)\left(0.485\right)} = 16.527 \quad (2)$$

For PMP21022, N_p = 100, and N_s = 10.

The auxiliary-to-secondary turns ratio is determined by the lowest target operating voltage in constant-current regulation and the UVLO turnoff threshold, $V_{DD,off}$, of the UCC28722. Here, V_{FA} is the auxiliary rectifier forward voltage drop (BAS20HT1G).

- From the data sheet, $V_{DD,off}$ = 7.7 V
- V_{FA} = 1.25 V
- V_{OCC} = 3.2 V
- V_F = 0.85 V

$$N_a = N_s \times \frac{V_{DD,off} + V_{FA}}{V_{OCC} + V_F}$$
$$= 10 \times \frac{7.7 + 1.25}{3.2 + 0.85} = 22.1 \text{ turns} \quad (3)$$

For PMP21022, the number of auxiliary turns was chosen to be 16.

3.3 Current Sense Resistance

From UCC28722's data sheet, the constant current regulating level, V_{CCR} = 330 mV . The output overcurrent protection level, I_{OCC} = 0.95 A. For design calculations, the estimated transformer efficiency, η_{XFMR}, is 0.9, accommodating for a 3.5% loss in the leakage inductance, 5% core and winding loss, and 1.5% loss in bias power. The current sense resistance is determined as the following shows.

- From the data sheet, V_{CCR} = 330 mV
- N_p = 100, N_s = 10
- I_{OCC} = 0.95 A
- η_{XFMR} = 0.9

$$R_{CS} = \frac{V_{CCR} \frac{N_p}{N_s}}{2I_{OCC}} \times \sqrt{\eta_{XFMR}}$$
$$= \frac{0.33 \times 10}{2 \times 0.95} \times \sqrt{0.9} = 1.648\ \Omega \approx 1.69\ \Omega \quad (4)$$

For PMP21022, R_{CS} = 1.69 Ω.

3.4 Transformer Primary Inductance

With the current sense resistance value, the maximum primary current can be determined as the maximum current sense threshold voltage found in the data sheet divided by the current sense resistance.

- From the data sheet, $V_{CST,max}$ = 0.78 V

$$I_{pp,max} = \frac{V_{CST,max}}{R_{CS}} = \frac{0.78}{1.69} = 0.462 \quad (5)$$

From here, the primary inductance can be found.

- V_F = 0.85 V
- I_{OCC} = 0.95 A
- f_{sw} = 60 kHz

$$L_p = \frac{2\left(V_{out} + V_F\right) \times I_{OCC}}{\eta_{XFMR} \times I_{pp,max}^2 \times f_{sw}}$$
$$= \frac{2\left(2 + 0.85\right) \times 0.95}{0.9 \times 0.452^2 \times 60 \times 10^3} = 2.118 \text{ mH} \quad (6)$$

The actual inductance of the transformer on the PMP21022 design, L_p = 1.7 mH.

3.5 Transformer Parameter Verification

The UCC28722 requires a minimum on time of the transistor (t_{on}) and minimum secondary rectifier conduction time (t_{DMAG}). The following equations can be used to determine if the minimum t_{on} target of 300 ns and the minimum t_{DMAG} target of 1.2 µs are achieved. V_{OCV} is the regulated output voltage of the converter, and V_F is the secondary rectifier voltage drop.

- From the data sheet, $V_{CST,min}$ = 190 mV
- From the data sheet, $V_{CST,max}$ = 780 mV
- V_{OCV} = 12 V
- V_F = 0.85 V

$$t_{on} = \frac{L_p}{V_{in,max}} \times \frac{I_{pp,max} \times V_{CST,min}}{V_{CST,max}} = \frac{1.7 \times 10^{-3}}{390} \times \frac{0.462 \times 190 \times 10^{-3}}{780 \times 10^{-3}} = 491\,\text{ns} > 300\,\text{ns} \quad (7)$$

$$t_{DMAG} = \frac{t_{on} \times V_{in,max}}{N_{ps} \times \left(V_{OCV} + V_F\right)} = \frac{491 \times 10^{-9} \times 390}{10 \times \left(12 + 0.85\right)} = 1.49\,\mu\text{s} > 1.2\,\mu\text{s} \quad (8)$$

With the chosen component values, both the minimum transistor on time and minimum secondary rectifier conduction time requirements are met. This means that the selected maximum switching frequency, transformer primary inductance, and current-sense resistor are valid for designs with UCC28722.

3.6 Output Capacitance

One consideration required while choosing the output capacitor is the ripple voltage requirement, which depends on secondary peak current and ESR. A 20% margin is added to the capacitor ESR requirement.

$$R_{ESR} = \frac{V_{ripple} \times 0.8}{I_{pp,max} \times N_{ps}} \quad (9)$$

The chosen bulk output capacitor has a dissipation factor of 0.16. From this, we can derive the ESR of the capacitor.

$$R_{ESR} = D_F \times X_C = \frac{0.16}{2\pi \times 60 \times 10^3 \times 560 \times 10^{-6}} = 0.758\,\text{m}\Omega \quad (10)$$

For this design, two 560 µF capacitors were placed in parallel at the output, so the equivalent ESR is half of the ESR of one capacitor. From here, we can derive the output voltage ripple.

$$V_{ripple} = \frac{\frac{R_{ESR}}{R} \times I_{pp,max} \times N_{ps}}{0.8} = \frac{0.379 \times 10^{-3} \times 0.462 \times 10}{0.8} = 2.188\,\text{mV} \quad (11)$$

The output capacitance value is typically determined by the transient response requirement from no load. The V_{DD} capacitance is dependent upon a couple user-defined parameters: I_{TRAN}, the required positive load-step current, and $V_{O\Delta}$, the output voltage drop allowed during the load-step transient. The desired minimum switching frequency was chosen to be 30 kHz.

- I_{TRAN} = 0.85
- $V_{O\Delta}$ = 0.36 V
- f_{min} = 30 kHz

$$C_{OUT} = \frac{I_{TRAN}\left(\frac{1}{f_{min}} + 150 \times 10^{-6}\right)}{V_{O\Delta}}$$
$$= \frac{0.85\left(\frac{1}{30 \times 10^{3}} + 150 \times 10^{-6}\right)}{0.36} = 432.9\ \mu F \quad (12)$$

3.7 V_{DD} Capacitance

Once the output capacitance is determined, the size of the V_{DD} capacitance can be found. The capacitance on V_{DD} needs to supply the device operating current until the output of the converter reaches the target minimum operating voltage in constant-current regulation.

- V_{OCC} = 3.2 V
- I_{OCC} = 0.95 A
- From the data sheet, I_{RUN} = 2 mA
- From the data sheet, $I_{DRS,max}$ = 37 mA, $I_{DRS,min}$ = 19 mA
- From the data sheet, D_{MAGCC} = 0.425
- From the data sheet, $V_{DD,on}$ = 21 V, $V_{DD,off}$ = 7.7 V

$$C_{DD} = \frac{\left(I_{RUN} + I_{DRS,max}\left(1 - D_{MAGCC}\right)\right)\frac{C_{OUT}V_{OCC}}{I_{OCC}}}{V_{DD,on} - V_{DD,off} - 1}$$
$$= \frac{\left(2 \times 10^{-3} + 37 \times 10^{-3} \times 0.575\right)\frac{1142.2 \times 10^{-6} \times 3.2}{0.95}}{21 - 7.7 - 1} = 7.3\ \mu F \quad (13)$$

The value of C_{DD} on the PMP21022 design was chosen to be a standard capacitance value, 4.7 µF.

3.8 Voltage Sense Divider

From here, the voltage sense divider resistor values can be determined. With the turn-on voltage chosen to be 200 V and the VS-line sense run current specified in the data sheet to be 225 µA, the high-side divider resistor value can be found.

- V_{en} = 200 V
- From the data sheet, $I_{VSL,run}$ = 225 µA

$$R_{S1} = \frac{N_a}{N_p} \times \frac{V_{en}}{I_{VSL,run}}$$
$$= \frac{16}{100} \times \frac{200}{225 \times 10^{-6}} = 142.22 k\Omega \approx 140\ k\Omega \quad (14)$$

For PMP21022, a 140-kΩ resistor was selected. With the typical specification for the constant voltage regulation level at the VS input to be 4.05 V, the low-side divider resistor value can be determined.

- From the data sheet, V_{VSR} = 4.05 V

$$R_{S2} = \frac{V_{VSR}R_{S1}}{\left(V_{out} + V_F\right) \times \frac{N_a}{N_s} - V_{VSR}}$$
$$= \frac{4.05 \times 140 \times 10^{3}}{\left(12 + 0.85\right) \times \frac{16}{10} - 4.05} = 34.34\ k\Omega \approx 35.7\ k\Omega \quad (15)$$

A 35.7-kΩ resistor was chosen the design. Here, V_{out} can be re-verified.

$$V_{out,verify} = \left(1 + \frac{R_{S1}}{R_{S2}}\right) \times V_{VSR} \times \frac{N_s}{N_a} - V_F$$
$$= \left(1 + \frac{140 \times 10^3}{35.7 \times 10^3}\right) \times 4.05 \times \frac{10}{16} - 0.85 = 11.608 \text{ V} \quad (16)$$

3.9 Line Compensation Resistance

The series resistor to the CS pin, R_{LC}, provides the function of feed-forward line compensation to eliminate changes in I_{pp} due to change in di/dt, the propagation delay of the internal comparator, and NPN transistor turn-off time. The line compensation resistance is calculated by Equation 17. The constant K_{LC} represents the line compensation current ratio found in the data sheet. t_d is the transistor turnoff delay with an additional 50 ns added to account for the internal UCC28722 delay, but the line compensation resistance value for the PMP21022 design was calculated with just the internal UCC28722 delay in mind.

- From the data sheet, K_{LC} = 25 A/A
- R_{S1} = 140 kΩ
- R_{CS} = 1.69 Ω
- N_p = 100, N_a = 16
- From the data sheet, t_d = 50 ns
- L_p = 1.7 mH

$$R_{LC} = \frac{K_{LC} \times R_{S1} \times R_{CS} \times t_d \times \frac{N_p}{N_a}}{L_p}$$
$$= \frac{25 \times 140 \times 10^3 \times 1.69 \times 50 \times 10^{-9} \times \frac{100}{16}}{1.7 \times 10^{-3}} = 1.087 \text{ k}\Omega \quad (17)$$

For PMP21022, R_{LC} was selected to be 953 Ω.

3.10 Startup Resistance

There is a tradeoff to be made between startup time and standby input power. For the design of the PMP21022, a startup time of 2 seconds was assumed.

- From the data sheet, I_{START} = 1 µA
- T_{STR} = 2 sec
- $V_{in,min}$ = 200 V
- From the data sheet, $V_{DD,on}$ = 21 V
- C_{DD} = 4.7 µF

$$R_{STR} = \frac{V_{in,min}}{I_{START} + \frac{V_{DD,on} C_{DD}}{T_{STR}}}$$
$$= \frac{200}{10^{-6} + \frac{21 \times 4.7 \times 10^{-6}}{2}} = 3.97 \text{ M}\Omega \quad (18)$$

For PMP21022, R_{STR} = 4.5 MΩ.

3.11 BJT Selection

The selected BJT needs to have enough current gain to source the peak primary current based off of the worst-case maximum DRV source current of UCC28722. The minimum specification for $I_{DRS,max}$ = 31 mA.

- $I_{pp,max}$ = 0.462 A
- From the data sheet, minimum $I_{DRS,max}$ = 31 mA

$$\beta_{min} = \frac{0.462}{31 \times 10^{-3}} = 14.9 \tag{19}$$

The minimum specified DC current gain of the selected BJT, STN2580, is 60, which is more than enough to support the primary current during operation.

Apart from this, the BJT must have a collector current rating high enough to support the maximum primary current, which the 1 A rating on the STN2580 covers. Other things to look out for are a low collector-emitter saturation voltage and quick rise/fall times. These help to minimize conduction and switching losses, respectively.

3.12 Zener Clamp

To limit the voltage stress on the BJT due to the leakage inductance while switching off, a Zener clamp is used. A 200 V Zener diode (1SMB5956BT3G) and a US1M-13-F (V_d = 1.7 V) diode were selected. STN2580 has a maximum collector to emitter voltage of 800 V. From here, the available clamp voltage to protect the BJT can be calculated.

$$\begin{aligned} V_{CLAMP} &= V_{CE,max} \times 0.9 - V_{in,max} \\ &= 800 \times 0.9 - 390 = 330 \text{ V} \end{aligned} \tag{20}$$

Now the series resistance can be determined.

$$\begin{aligned} R_S &= \frac{V_{CLAMP} - V_d - V_Z}{I_{pp,max}} \\ &= \frac{330 - 1.7 - 200}{0.462} = 407.6\ \Omega \end{aligned} \tag{21}$$

A standard resistor value of 330 Ω was chosen as the series resistance.

4 Layout Guidelines

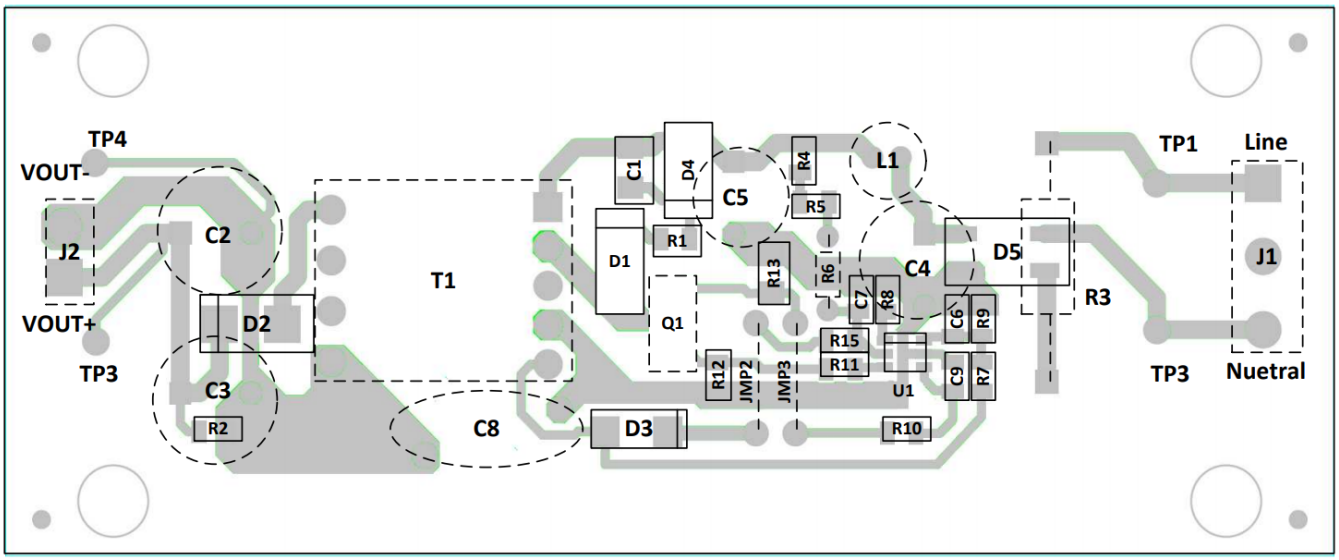

Figure 3. UCC28722 Layout Example

4.1 Layout Instructions

The following guidelines for PCB layout, found in the UCC28722 data sheet, were used during the design of the PMP21022 and are recommended for optimal performance.

- High frequency bypass capacitor C7 should be placed across Pin 2 and 5 as close to the pins as possible.
- R15 and C7 form a low-pass filter and the connection of the two should be as close to the VDD pin as possible.
- UCC28722 features a typical CS pin leading edge blanking time of 290 ns. In cases where this may not be enough, an additional bypass capacitor (C9) can be placed from the CS pin to ground. C9 may not be required for all designs, but it is wise to have the footprint available if necessary.
- C9 should be placed as close to R10 as possible. Together, these form a low-pass filter which should be as close to the CS pin as possible.
- The VS pin controls the output voltage through the transformer turns ratio and the voltage divider of R7 and R9. The trace between R7, R9, and the VS pin should be as short as possible to reduce and eliminate EMI coupling.
- IC ground and power ground should meet at the return of the bulk capacitors (C4, C5). Ensure that high frequency and high current from the power stage does not go through signal ground.
  - The high-frequency and high-current path that one should be cautious of on the primary is C4, C5+, T1 (P1, P2), Q1 emitter, Q1 collector, R13 to the return of C4 and C5.
- Keep all current loops as short as possible.
- Keep all high current and high frequency traces away from or perpendicular to the other traces in the design. This prevents high frequency noise from coupling into other traces.
- Traces on the voltage clamp formed by D1, R1, D4, and C4 should be kept as short as possible.
- C4 return needs to be as close to the bulk capacitor supply as possible. This reduces the magnitude of dv/dt cause by large di/dt.
- Avoid mounting semiconductors under magnetics. This prevents switching noise from coupling into other signals.

4.2 PMP21022 Layout

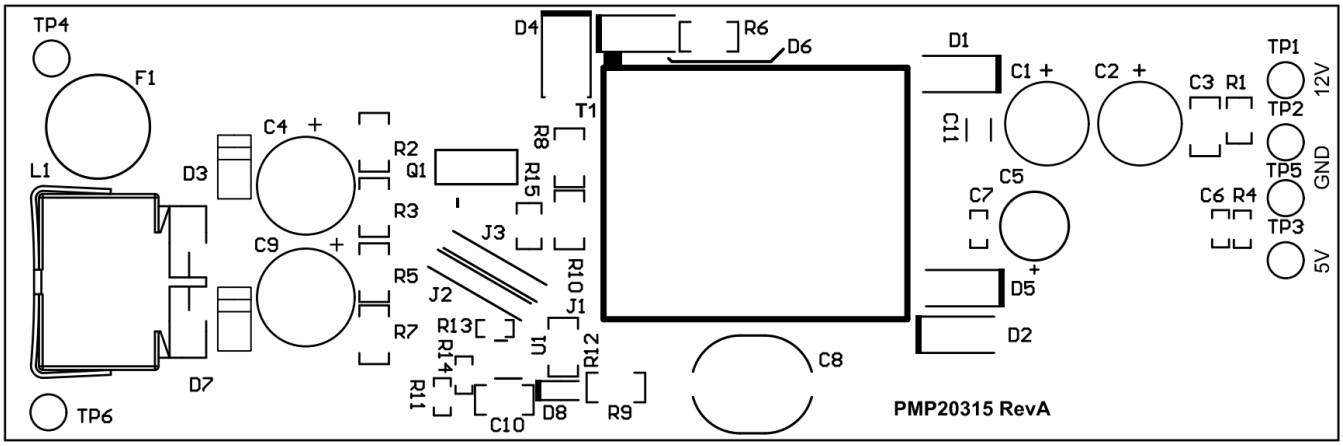

Figure 4. PMP21022 Placement

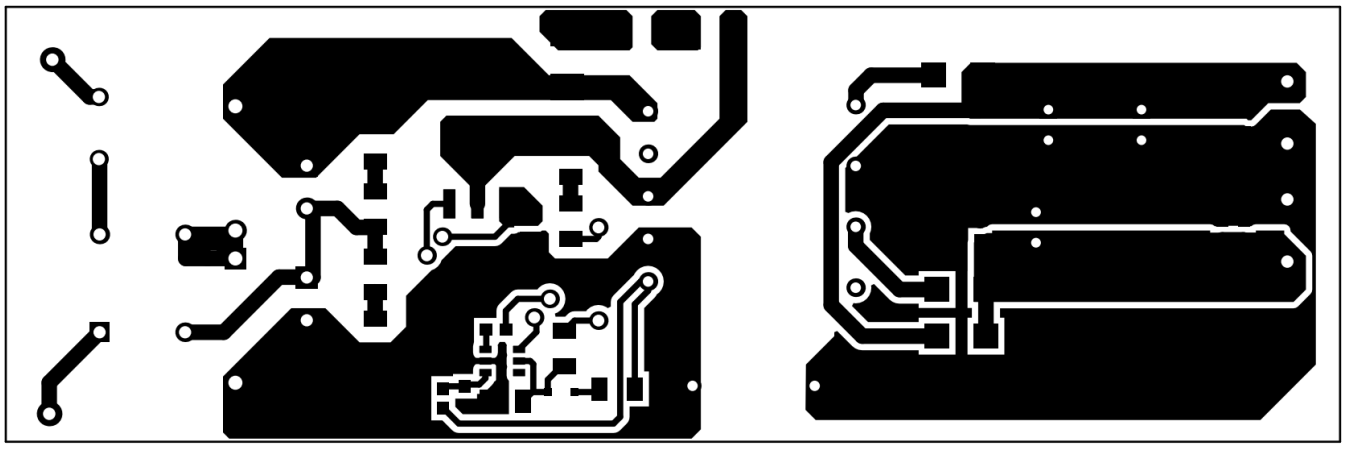

Figure 5. PMP21022 Routing

5 References

1. Texas Instruments, *UCC28722 Constant-Voltage, Constant-Current Controller With Primary-Side Regulation, BJT Drive Data Sheet*
2. Texas Instruments, *PMP21022 Reference Design*

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