Application Report
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Maximum Output Power and Thermal Considerations for UCC28720 and UCC28722

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1 Introduction

The UCC28720/2 discontinuous current mode (DCM) flyback converters were designed for off-line applications using a bipolar junction transistor (BJT) as the main switch (Q_A) instead of a field effect transistor (FET). This technique is popular in low power applications because BJTs are less expensive for the same voltage and current ratings compared to FETs allowing the power supply designer to reduce the overall cost of the design. The only problem is that BJTs are not commonly used in most flyback power converter designs and the power supply designer may not be familiar how to use a BJT or BJT controller. This application note will review BJT functionality and how to estimate BJT power dissipation, as well as, techniques to design for the highest output power and ambient temperature possible in a BJT, DCM, flyback converter with convection cooling. Figure 1 shows a simplified typical DCM flyback converter implementing a BJT switch, using the UCC28722 controller. The UCC28720/2 devices are presently used in but not limited to high voltage electricity meter applications, system bias supplies and USB chargers and adapters.

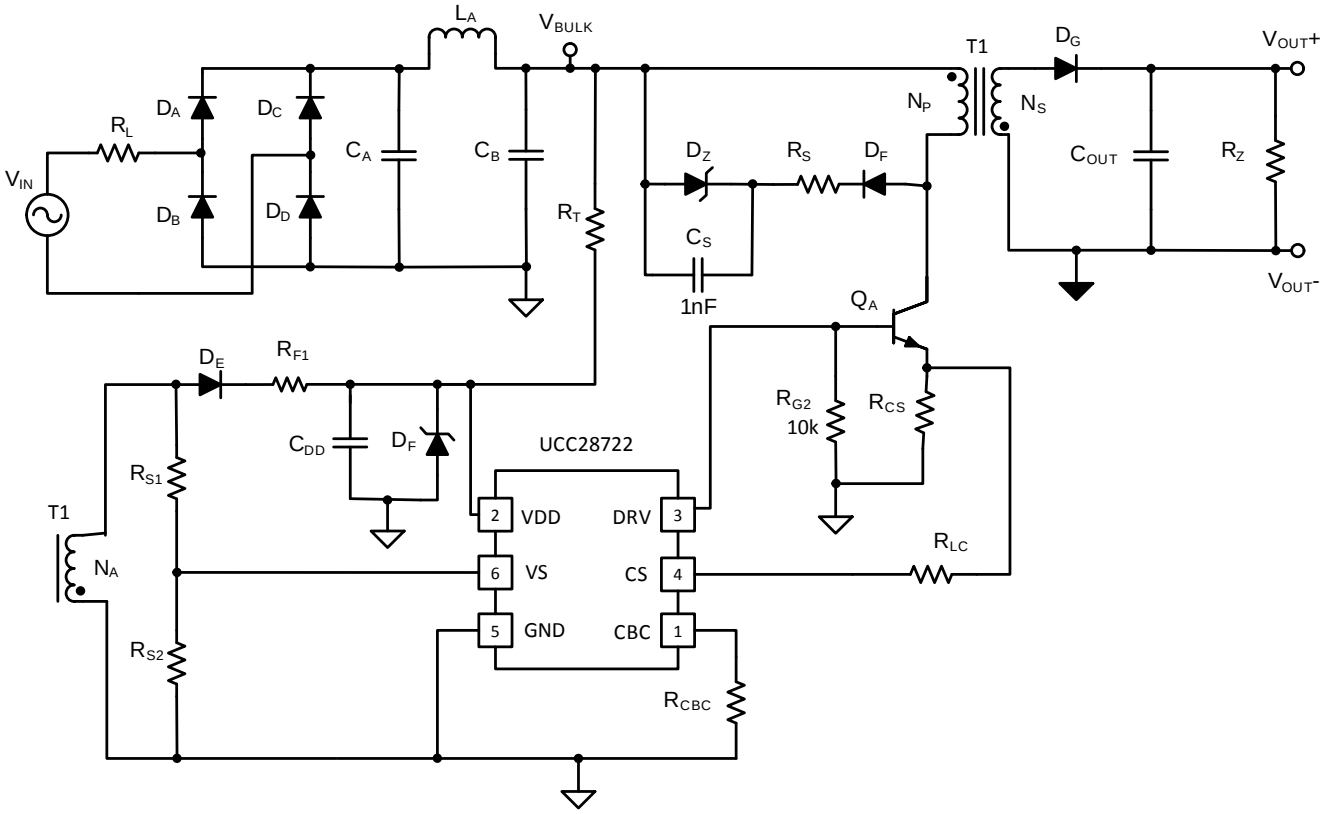

Figure 1. Offline Flyback Converter Using a BJT

2 NPN BJT Model and Operation Review

Before diving into power and thermal calculations for a BJT in a flyback converter it is probably a good idea to start by reviewing a basic model of an NPN BJT. A bipolar transistor in its simplest form is a current-controlled current sink/switch. The base (B) input current controls the current flow from collector (C) to emitter (E). Figure 2 gives conceptual and schematic diagrams of an NPN BJT. This device is doped with two N (Negatively Charged Atoms) semiconductor regions separated by a P (Positively Charge Atoms) doped region. The base is connected to the P material, while the emitter and collector are connected to N regions of the transistor.

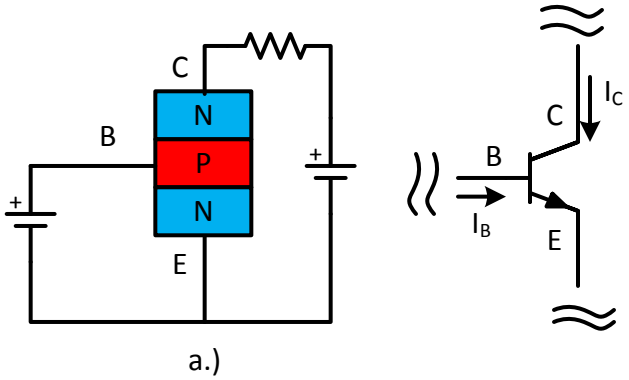

Figure 2. NPN BJT Conceptual and Schematic Diagrams

The base-emitter junction acts similar to a diode. A positive voltage applied to the base-emitter junction will attract the free electrons of the N material connected to the emitter (E). These free electrons will migrate into the P material leaving a deficiency of free electrons in the N material. This deficiency of electrons in the N material will attract electrons from the negative terminal of the bias supply connected to the base and emitter completing the circuit and allowing current to flow. A negative bias across the B-E junction will cause excess electrons to be attracted out of the P material breaking the circuit and stopping current flow, just like back-biasing a diode.

When the base-emitter junction is forward biased and the collector (C) to emitter (E) path is biased, this will open the flood gates and allow current to flow. The positive bias connected to the collector will attract free electrons to the collector terminal leaving a deficiency of electrons in the N material. This will attract electrons from the base which will deplete into the N material allowing for current to flow through the collector and emitter depletion layers completing the circuit. The amount of collector current (I_C) may be orders of magnitude greater than the base current (I_B). The ratio of I_C to I_B is generally known as the transistor DC current gain. This can be represented in the data sheet by Beta (β) or h_{FE}. Note that this ratio is specified in the transistor data sheet under certain conditions and can have significant variation.

$$h_{FE} = \beta = \frac{I_C}{I_B} \tag{1}$$

When the collector to base current ratio is forced to be less than what is specified in the data sheet for h_{FE} the transistor is defined to be operating in saturation. When a BJT is in saturation an increase of base current will not generate more collector current. The voltage from collector to emitter has collapsed to its lowest magnitude and is specified in the data sheet as the collector-emitter saturation voltage ($V_{CE(sat)}$). This voltage is generally 0.5 to 2 V depending on the BJT and current level. When the BJT is used as the main switch in adaptor and bias supply applications, the device is driven into saturation to keep conduction losses to a minimum.

$$h_{FE} = \beta > \frac{I_C}{I_B} \tag{2}$$

3 Driving/Operation of a BJT in a DCM Flyback Converter

The UCC28720/2 BJT flyback controllers are designed to drive a BJT in discontinuous conduction mode (DCM) using an FM/AM/FM modulation scheme to control the converter's duty cycle. The UCC28720/2 driver stage functional block diagram is presented in Figure 3. In power supply applications, driving a BJT is different than driving a FET. When using a FET, the gate only conducts current while the gate capacitance is charging and discharging. The BJT is always conducting when the base to emitter junction is forward biased. Also, when turning off the saturated BJT, a good portion of the collector current will come out of the base of the transistor until it is pulled out of saturation. This is unlike the FET where the gate drive never sees the FET's drain current.This puts more stress on the BJT flyback controller's base drive circuitry compared to the FET's gate drive.

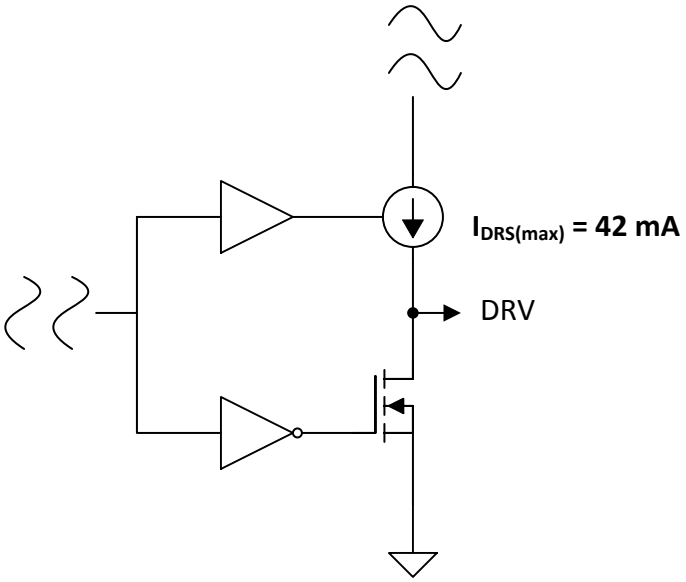

Figure 3. Simplified Driver Stage of UCC28720/2 BJT Controllers

Let's review and study the turn-on and turn-off switching waveforms of the BJT and a DCM flyback converter (shown in Figure 4), to help the reader understand the electrical stresses on the UCC28720/2 flyback controllers caused by driving a BJT in this application. Note that the BJT collector voltage (V_C), collector current (I_C), and voltage across the current sense resistor (V_{RCS}) waveforms were recorded from a 5W USB adaptor. The base current (I_B) and output diode current (I_{DG}) were drawn in as representative of the respective currents and may not be to actual scale.

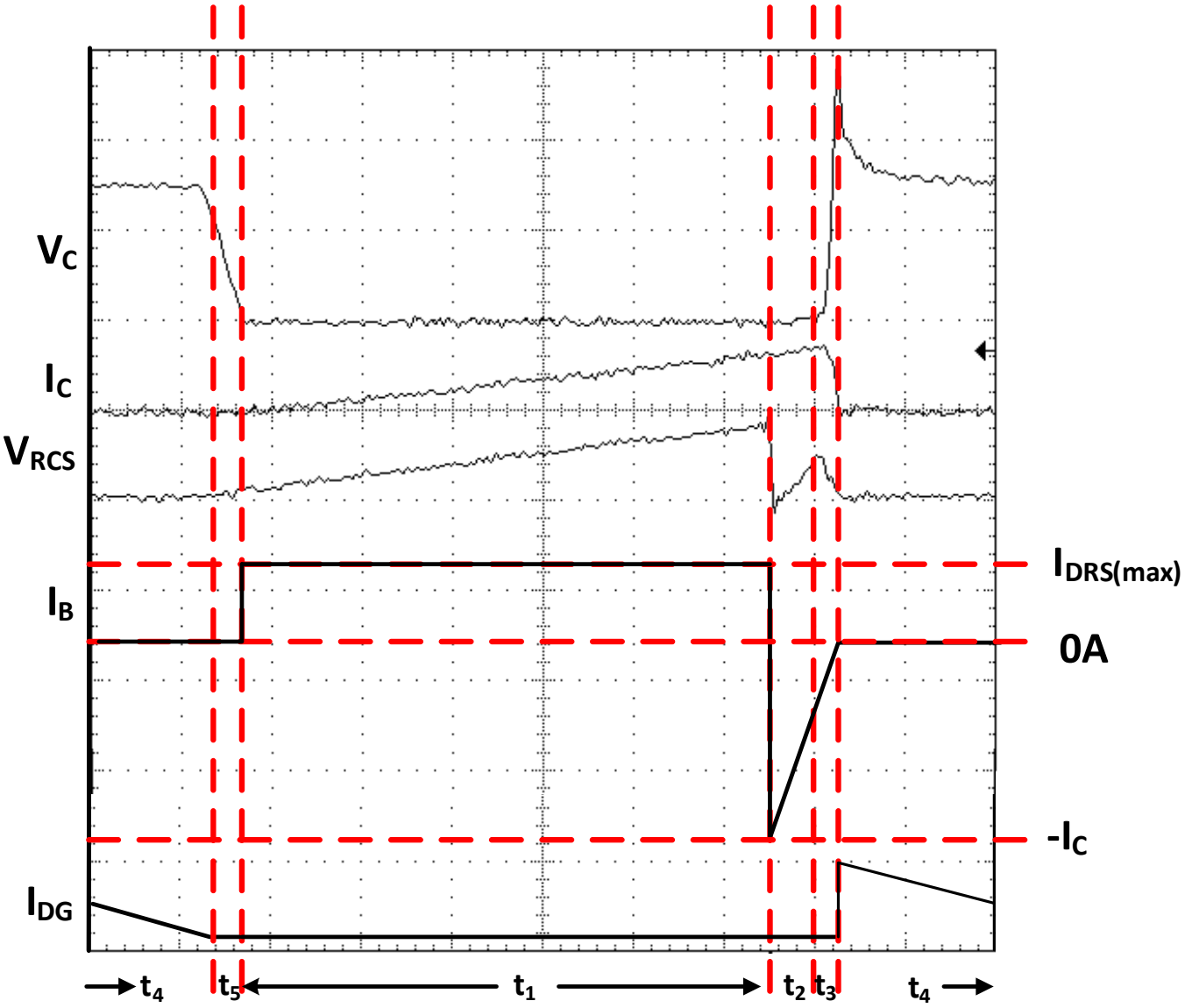

Figure 4. Switching Waveforms of a BJT in a DCM Flyback Converter

In Figure 4, at the beginning of interval t_1 the collector current is zero and the base of the BJT is driven with ($I_{DRS(max)}$) constant current at 42 mA maximum. The primary current is sensed with a current-sense resistor (R_{CS}). During interval t_1, the transformer (T1 of Figure 1) is energized and the BJT is driven into saturation. Once the desired primary peak current is reached at the end of t_1 (V_{RCS} = 780mV) the base of the BJT is pulled low with an internal FET. At this point all of the collector current (I_C) will flow out of the base of the transistor and into the DRV pin of the UCC28720/2 controller ($I_B = I_C$).

During time interval t_2, the base-collector junction is starting to go into reverse recovery and the transistor will stay on until the base current has depleted to roughly half of the collector current. Also note that the difference in collector current to emitter current during this time period will go through the base of the transistor. The transistor remains on and the magnitude of the collector current is changing with the transformer's magnetizing current. This interval is also known as the BJT storage time (t_s) and can be found in the BJT device's data sheet.

At the beginning of t_3 and the end of the storage time, the transistor begins to turn off. During this interval, both PN junctions of the transistor are going into a reverse recovery. The base and emitter will share the collector current while the transistor is turning off and the collector current is depleting. The collector voltage will increase gradually and reach its maximum once the BJT has fully turned off. This voltage is equivalent to the sum of the input voltage, reflected output voltage across the transformer, and the voltage spike caused by the leakage inductance of the transformer.

During interval t_4, energy is delivered to the secondary winding and diode D_G conducts, delivering energy to the output. Once the transformer's energy is depleted, the collector voltage starts to ring toward ground. This voltage is sensed through the auxiliary winding's turn ratio (N_A/N_P) and once the controller has observed that the transformer is de-energized, it drives the BJT base again for the next switching cycle (after delay t_5 is added to achieve valley switching). Note that the waveform presented in Figure 4 is only a snapshot of the converter when it is operating near critical conduction at full load and maximum switching frequency. To control the duty cycle, the controller will modulate the frequency (FM) and the amplitude of the primary current (AM) and drive the converter deeper into discontinuous mode. Maximum duty cycle for these converters is when the converter is operating near critical conduction by design.

4 Estimating Conduction and Switching Losses of the BJT

The calculations to estimate the conduction and switching losses in a BJT are similar to that for a diode. Base, emitter and collector saturation voltages are modeled as batteries, similar to the forward voltage of diodes. Average currents are used to estimate average conduction losses. In this application, all of the currents involved in the calculations are triangles or trapezoids, and the average calculations utilize principles of basic geometry and are well documented. One major difference is that the BJT has a storage-charge delay (t_s). The base of a BJT transistor needs an amount of storage charge (Q_S) removed from it before the device starts to turn off. It requires knowing how to calculate reverse recovery charge (Q_r) of PN junctions. The reverse-recovery charge is the amount of charge in the reverse direction it takes to get the semiconductor device to stop conducting.

To show how to calculate the losses of the BTJ switch (Q_A), we will review a 5W USB flyback converter operating at 115V RMS input, with NPN BJT specifications presented in Table 1. The peak collector current ($I_{C(PK)}$) is limited to 360 mA by the controller and the converter's maximum frequency (f_{MAX}) is limited to 72 kHz by design. Based on the minimum input voltage, the converter was designed for a maximum duty cycle (D_{MAX}) of 50%. The maximum collector voltage ($V_{C(max)}$) at this input condition and transformer turns ratio and clamp voltage is 250V.

$$I_{C(PK)} = 0.36A,\ f_{MAX} = 72kHz\ ,D_{MAX} = 0.50,V_{C(\max)} = 250V \tag{3}$$

Table 1. Data Sheet Parameters for a BJT

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_r	Rise time	V_{CE} = 200 V, device = 0.3 A		120		ns
t_s	Storage time	I_{B1}= 20 mA, IB2= –50 mA		4		µs
t_f	Fall time	T_P=30 µs, test pulse duration		90		ns

To estimate the losses in the transistor of this design will require estimating the time intervals presented in Figure 4. The sum of time t_1 and t_2 is the duration of the maximum duty cycle which is roughly 6.99 us for this design example.

$$t_1 + t_2 = \frac{D_{MAX}}{f_{MAX}} = \frac{50\%}{72kHz} \approx 6.99us \tag{4}$$

In order to estimate time t_2 the device's stored charge (Q_s) needs to be calculated. Based on the parameters from the BJT data sheet for t_s and the base discharge current (I_{B2}), the storage charge is 200nC.

$$Q_s = t_S \times |\ I_{B2}\ | = 4us \times 50mA = 200nC \tag{5}$$

During time t_1, the transistor had been driven into saturation and at the beginning of time t_1 all the collector current is going through the base of the transistor. As the base is going into a type of reverse recovery during t_2 the collector current is split between the base and emitter of the transistor. Based on this information and the trapezoidal shape of the current in the interval, the average base current ($I_{B2(avg\_t2)}$) during storage time t_2 can be calculated.

$$I_{B2(avg\_t2)} = \frac{I_{C(PK)} + \frac{I_{C(PK)}}{2}}{2} = \frac{0.36A + \frac{0.36A}{2}}{2} \approx 0.27A \quad (6)$$

With the average base current and Q_s, time $t_2$and $t_1$can be calculated with the following equation.

$$t_2 = \frac{Q_s}{I_{B2(avg\_t2)}} = \frac{200nC}{0.27A} \approx 741ns \quad (7)$$

$$t_1 = \frac{D_{MAX}}{f_{MAX}} - t2 = 6.99us - 741ns \approx 6.25us \quad (8)$$

The amount of collector reverse recovery charge (Q_r) is used to estimate switching loss time interval t_3. Based on the BJT data sheet parameters Q_r is calculated to be 36nC.

$$Q_r = t_r \times I_C = 120ns \times 0.3A = 36nC \quad (9)$$

At the end of the storage time t_2, half of the collector current is going through the base and the other half of the collector current is going through the emitter. At this time both base-to-collector and base-to emitter PN junctions are engaged in reverse recovery. The peak base current $I_{B2(t3)}$ at the beginning of t_3 with Q_s can be used to estimate the time of reverse recovery for interval t_3, which is roughly 200 ns in this design example.

$$I_{B2(t3)} = \frac{0.36A}{2} = 0.18A \quad (10)$$

$$t_3 = \frac{Q_r}{I_{C(avg\_t3)}} = \frac{36nC}{0.18A} \approx 200ns \quad (11)$$

Once intervals t_1 through t_3 have been calculated based on data sheet and system requirements, the following equation can be used to estimate the maximum loss of BJT (P_{QA}) at 115V RMS input and maximum switching frequency ($f_{SW(max)}$), where $I_{DRS(max)}$ is the maximum current at which the UCC28720/2 controllers can drive the base of the BJT (42 mA), and V_{BE} is the base to emitter forward voltage drop. $V_{CE(sat)}$ is the collector to emitter saturation voltage. For the BJT that we have been evaluating, the power dissipation of the BJT would be roughly 0.733W at maximum switching frequency of 72 kHz.

$$P_{QA} \approx I_{DRS(\max)} \times V_{BE} \times D_{MAX} + \left[\frac{I_{C(PK)}}{2} \times V_{CE(sat)} \times (t_1 + t_2) \times f_{SW(\max)}\right] + \left[\frac{I_{C(PK)}}{2} \times V_{C(\max)} \times t_3 \times f_{SW(\max)}\right] \quad (12)$$

$$P_{QA} \approx 42mA \times 0.6V \times 50\% + \left[\frac{0.36A}{2} \times 0.8V \times (6.986us) \times 72kHz\right] + \left[\frac{0.36A}{2} \times 250V \times 200ns \times 72kHz\right] \approx 0.733W \quad (13)$$

5 Estimating Controller Power Dissipation

Before discussing how to estimate the UCC28720/2 power dissipation some time needs to be spent on reviewing data sheet parameters. The specifications in Table 2 were taken from the UCC28722 data sheet which gives typical, minimum and maximum values. It is the power designer's responsibility to take the worst case specifications into account. For example the UCC28722 data sheet specifies that the maximum switching frequency can range from 72 to 89 kHz, with a typical maximum frequency of 80 kHz. The UCC28720/2 maximum frequency is set by the selection of primary transformer magnetizing inductance,

load current and efficiency [1]. To ensure a design using the UCC28722 works correctly, the power supply designer should select the magnetizing inductance to limit the switching frequency to 72 kHz, which is the lowest worst case switching frequency and will ensure the controller will not be frequency limited. Some designers make the mistake of designing around typical values and not taking the worst case values into account.

Table 2. UCC28722 Device Parameters

PARAMETER	MIN	TYP	MAX	UNIT
$f_{SW(max)}$ Maximum switching frequency	72	80	89	kHz
I_{RUN} Supply Current		2	2.65	mA
$I_{DRS(max)}$ Maximum DRV source current	31	37	42	mA
R_{DRVLS} DRV low-side drive resistance		1	2.4	Ω
V	735	780	815	mV
V_{VDD} Recommended bias supply operating voltage	9		35	V
T_J Operating Temperature	–55		150	°C

One design tip to reduce power dissipation in the UCC28720/2 controllers is to select the transformer turns ratio (N_A/N_S) to set the nominal V_{VDD} voltage close to the data sheet minimum limit. To leave some margin in your design a good target would be to design for a V_{VDD} voltage of 10 V.

$$V_{VDD} = 10\,V \tag{14}$$

The following equation can be used to estimate worst case power dissipation (P_{IC}) in the UCC28720/2 BJT flyback controllers. Where V_{VDD} is the voltage supplied to the VDD pin of the UCC28722 from the auxiliary winding, I_{RUN} is the UCC28720/2's supplied run current and R_{DRVLS} is the UCC28720/2's low side pull-down resistance of the driver FET inside the UCC28720/2 controllers used to turn off the BJT.

$$P_{IC} = V_{VDD} \times I_{RUN} + I_{DRS(\max)} \times V_{VDD} \times t_1 \times f_{max} + \left(I_{C(PK)} \times \left(\frac{t_2 \times f_{max}}{3} \right)^{\frac{1}{2}} \right)^2 \times R_{DRVLS} \tag{15}$$

In this UCC28720/2 flyback design example, the maximum power the integrated circuit would dissipate is roughly 221 mW.

$$P_{IC} = 10V \times 2.65mA + 42mA \times 10V \times 6.25us \times 72kHz + \left(0.36A \times \left(\frac{741ns \times 72kHz}{3} \right)^{\frac{1}{2}} \right)^2 \times 2.4\Omega \approx 0.221W \tag{16}$$

6 Controller Thermal Considerations

With the estimated power dissipation of the PWM controller, the device's thermal impedance ($R_{\theta JA}$), and the ambient temperature (T_{amb}), it is possible to estimate the PWM controller's junction temperature (T_J). In a UCC28722 design where the PWM controller is dissipating 221 mW with an ambient temperature of 60 degrees Celsius, the junction temperature of the UCC28722 of the controller would be roughly 100 degrees Celsius.

$$R_{\theta JA} = \frac{180℃}{W} \tag{17}$$

$$T_J = T_{amb} + P_{IC} \times R_{\theta JA} = 60℃ + 0.221\frac{180}{W} \approx 100℃ \tag{18}$$

The UCC28720/2 specifications state that the junction temperature needs to be kept below 150°C. To add thermal margin to the design it is recommended to design your power supply to run with a junction temperature 25°C less than the maximum rating. The following equation can be used to estimate the maximum ambient temperature of the UCC28720/2 controllers can be design for in convection cooling application with 25°C of margin to ensure the $T_{J(max)}$ specification is not violated. A UCC28722 design that was dissipating 221 mW of power with convection cooling could operate in an ambient temperature of up to 85°C based on these criteria.

$$T_{amb\,(\max)} = (T_{J\,(\max)} - 25℃) - P_{IC} \times R_{\theta JA} = 150℃ - 25℃ - 0.221W\frac{180℃}{W} \approx 85℃ \quad (19)$$

Because of its larger package, the UCC28720 has a slightly better junction-to-ambient thermal impedance compared to the UCC28722 and in this example could be used in a design with a maximum ambient temperature of roughly 94 °C.

$$R_{\theta JA} = \frac{141℃}{W} \quad (20)$$

$$T_{amb\,(\max)} = (T_{J\,(\max)} - 25℃) - P_{IC} \times R_{\theta JA} = 150℃ - 25℃ - 0.221W\frac{141℃}{W} \approx 94℃ \quad (21)$$

NOTE: Although the devices may operate to junction temperatures up to 150°C, their parameters are ensured only to 125°C.

7 Estimating Maximum Capable Output Power

The maximum output power ($P_{OUT(max)}$) that the UCC28720/2 BJT flyback controller is capable of controlling is limited by the flyback controller's drive current ($I_{DRS(max)}$), the selected BJT's h_{FE}, the flyback converter's maximum duty cycle (D_{max}), the flyback converter's system efficiency (η) , and the minimum input bulk voltage ($V_{BULK(min)}$), and can be defined by the following equations.

$$\eta = \frac{V_{OUT} \times I_{OUT}}{V_{BULK\,(\min)} \times I_{IN}} = \frac{P_{OUT\,(\max)}}{V_{BULK\,(\min)} \times \frac{I_{DRS\,(\max)} \times h_{FE} \times D_{max}}{2}} \quad (22)$$

$$P_{OUT\,(\max)} = \frac{I_{DRS\,(\max)} \times h_{FE} \times D_{max} \times \eta \times V_{BULK\,(\min)}}{2} \quad (23)$$

Determining the h_{FE} of a BJT transistor requires studying the BJT's family of curves in the active region. The curves in Figure 5 come from a 400-V, 1-A BJT used in a 5-W design. Based on this family of curves, it is estimated that when the BJT is turned on in the active region the h_{FE} would be between 15.5 (h_{FE1}) and 18.7 (h_{FE2}) based on the $I_{DRV(max)}$ variation.

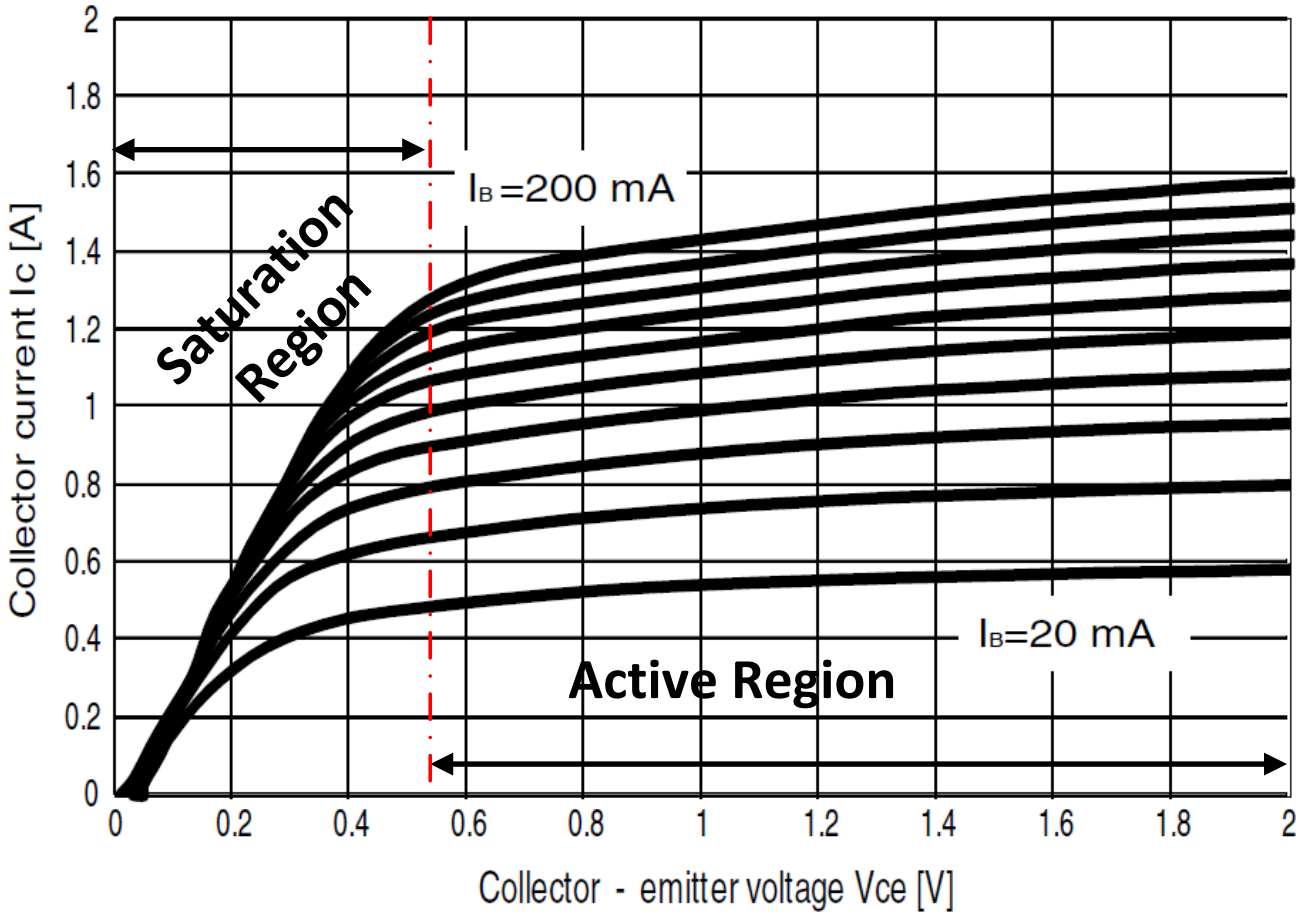

Figure 5. BJT Family of Curves

$$h_{FE} = \frac{I_C}{I_{DRS(\max)}} \tag{24}$$

$$h_{FE1} = \frac{0.65A}{42mA} \approx 15.5 \tag{25}$$

$$h_{FE2} = \frac{0.58A}{31mA} \approx 18.7 \tag{26}$$

In a UCC28722 application using the BJT with the family of curves of Figure 5 and with an estimated system efficiency of 78%, the maximum output power range would be roughly 8.1 W to 9.1 W based on h_{FE} and $I_{DRS(max)}$ variation. To give the design margin and ensure the design could supply power with device parameter variation it would be recommended to keep the maximum power under 8 W.

$$P_{OUT(\max)1} = \frac{31mA \times 18.7 \times 0.5 \times 0.78 \times 72V}{2} \approx 8.1W \tag{27}$$

$$P_{OUT(\max)2} = \frac{42mA \times 15.5 \times 0.5 \times 0.78 \times 72V}{2} \approx 9.1W \tag{28}$$

I have seen BJT transistors for this application with an h_{FE} as high as 20 at roughly 30 mA of base current. This would bring the potential maximum output power level of a flyback converter in this application up to 8.7 W. It may be possible to deliver even higher power if a BJT with a greater h_{FE} can be found by the power supply designer.

$$P_{OUT(\max)3} = \frac{31mA \times 20 \times 0.5 \times 0.78 \times 72V}{2} \approx 8.7W \quad (29)$$

There is a design technique that will allow the designer to increase the maximum power level of the BJT flyback converter. That would be to increase the minimum input bulk voltage of the design. For example, if you increased the minimum input voltage to 100 V, the flyback converter could be designed to support an output power level of 12 W. Generally, this requires using a larger bulk capacitance value or limiting the input voltage minimum range.

$$P_{OUT(\max)4} = \frac{31mA \times 20 \times 0.5 \times 0.78 \times 100V}{2} \approx 12W \quad (30)$$

If you are using a voltage doubler with an off-line converter, and design your flyback converter to work with a minimum input bulk voltage of 250 V, it would allow the BJT flyback converter to deliver power levels of up to 30 W.

$$P_{OUT(\max)5} = \frac{31mA \times 20 \times 0.5 \times 0.78 \times 250V}{2} \approx 30W \quad (31)$$

8 Summary

In lower power applications, BJT DCM flyback converters are a popular choice due to their lower overall cost compared to FET-based DCM flyback converters. However, as this application note discusses, it is important to understand how BJT's work in a switching power converter to enable the power supply designer to estimate power and thermal stresses on the BJT and on the controller. The maximum output power that a DCM flyback can be designed for using the UCC28720/2 is limited by $V_{BULK(min)}$, the BJT's h_{FE} and the controller's maximum base-drive current ($I_{DRS(max)}$). Typical off-line flyback applications using the UCC28720/2 can be designed for output power levels up to 8 W. However, by increasing the minimum flyback input bulk voltage the UCC28720/2 flyback could be designed for power levels up to 30W.

9 References

1. UCC28720 Data Sheet, UCC28720 Constant-Voltage, Constant-Current Controller With Primary-Side Regulation, September 2015, pp17..19. http://www.ti.com/product/ucc28720
2. UCC28722 Data Sheet, UCC28722 Constant-Voltage, Constant-Current Controller With Primary-Side Regulation, October 2015 http://www.ti.com/lit/gpn/ucc28722

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