Implementation of the ISO14443B Protocol in the TI TRF796x

ShreHarsha Rao

ABSTRACT

This application note discusses the anti-collision sequence (slot marker method) of the ISO14443B standard implemented in the MSP430F2370 (a 16-bit ultra-low power microcontroller from the TI MSP430 family) used with Texas Instruments' TRF796x, a fully integrated 13.56-MHz radio frequency identification (RFID) analog front end and data framing reader system.

This document is designed for use by customers who are familiar with RFID and firmware development and want to develop their own application using the TRF796x. This reference guide should be used in conjunction with the ISO14443B standard which specifies the standard protocol, commands and other parameters required for communication between the transponder and the reader.

Contents

List of Figures

List of Tables

1 Anti-Collision Sequence for ISO14443B

The following describes the anti-collision sequence for the ISO14443B.

The commands used by the PCD during anti collision are:

- **REQB** – The REQB commands are sent by the PCD initially to probe the field for PICCs of Type B. Parameter 'N' in the REQB command defines the number of slots to be used in the anti-collision sequence.
- **Slot Marker Command** – After the REQB command, the PCD may send up to (N-1) Slot Marker Commands to define the start of each timeslot. Each Slot Marker command has 1 byte which defines the slot number.

The PCD initiates communication with the tag(s) by sending a REQB command. The PICC checks the parameter 'N' on reception of the REQB command.

If N = 1, the PICC responds with an ATQB message immediately.

If N>1, the PICC internally generates a random number R which is evenly distributed between 1 and N.

If R = 1, the PICC immediately sends an ATQB message.

If R > 1, the PICCs wait for the Slot Marker command with a matched slot number (slot number = R) before sending the ATQB. If there is no collision, the reader reads the data bytes (PUPI) in the FIFO. If there is collision, the PCD repeats the anti-collision sequence until there are no collisions.

2 Pseudo-Code for ISO14443B Tag Detection

2.1 Setting Up of Registers

The default configuration after power-up supports ISO15693, single sub-carrier, high data rate, 1-out-of-4 operation. To enter another protocol (ISO14443B in this case), the ISO Control register (0x01) has to be written to with the appropriate data byte. For example, to choose an ISO14443B, 106-Kbps protocol, the ISO Control register is written with 0x0C. All the low level options register (0x02 to 0x0B) are automatically set according to the new protocol.

Next the RF field and receivers should be turned on. This can be done by setting bit B5 in the Chip Status Control (0x00) register. Now the reader is ready to transmit commands to the tag.

2.2 Enable No Response Interrupt

During an inventory process, when the PCD receives no response from the PICC, it shall wait for a preset time (defined in RX No Response Wait Time register) before sending the Slot Marker command. The TRF796x informs the microcontroller when to send the Slot Marker command to the TRF796x via a no response interrupt. This is enabled by setting bit B0 in the Collision Position and Interrupt Mask register (CPIM). Thus if there is no response within the defined time, an interrupt request is sent and a flag is set in the IRQ Status register.

Pseudo-Code:

Read the Collision Position and Interrupt Mask register value.

Set bit B0.

Write the final value to the Collision Position and Interrupt Mask register.

The Collision Position and Interrupt Mask register has masks for other interrupts like collision, errors, etc. To ensure that the mask status is maintained for other interrupts, the CPIM register is read first and then the bit zero (corresponding to No Response Interrupt) alone is set in the value obtained from the read. Alternately, if the mask status is known for all the interrupts, the register can be directly written to with the desired value, thereby avoiding the read operation.

2.3 Send REQB Command

Note: The general procedure to start transmission is described below. **This is applicable to all commands that need to be transmitted to the tag.**

The data/command that is to be transmitted is written in to the FIFO, a 12 byte buffer. Transmission starts when the first data byte is written into FIFO. The reader adds SOF, EOF and CRC to the request packet before transmitting.

1. Start condition
2. Send Reset command 0x0F (command mode – 0x8F)
3. Send Transmission command (0x90 - without CRC or 0x91 – with CRC)
4. Continuous write to register 0x1D (0x3D)
5. Data for register 0x1D (upper and middle nibble of the number of bytes to be transmitted)
6. Data for register 0x1E (lower nibble of the number of bytes to be transmitted)
7. Data byte(s) for FIFO
8. Stop condition

Note that the FIFO can be written to (and read from) in continuous mode only.

For details on the Start and Stop conditions, refer to the timing diagrams for SPI/Parallel mode.

The REQB format (according to the ISO 14443-3 spec) is as follows:

Table 1. REQB Format

APf	AFI	PARAM	CRC_B
8 bits	8 bits	8 bits	16 bits

As mentioned earlier, the SOF, CRC_B and EOF will be added automatically by the reader. Only the anti-collision prefix (APf), application family identifier (AFI) and parameters (PARAM) bytes have to written to the FIFO for transmission.

Pseudo-Code:

buf is an array that holds all the command/data bytes that are to be sent to the reader.

size is the number of bytes to be transmitted. In this case, size = 3.

AFI is the application family identifier. If 0, all the PICCs process the REQB command.

```
buf[0] = 0x8f;                  /* Reset FIFO command */
buf[1] = 0x91;                  /* Send with CRC */
buf[2] = 0x3d;                  /* Write continuous from register 1D */
buf[3] = (char) (size >> 8);    /* Data for register 1D */
buf[4] = (char) (size << 4);    /* Data for register 1E */
buf[5] = 0x05;                  /* Anti-collision prefix byte*/
buf[6] = 0x00;                  /* Application family identifier*/
buf[7] = 0x0C;                  /* PARAM byte with REQB bit set and N = 16 */
```

1. Write buf[0] to buf[7] to TRF796x via SPI or Parallel mode (refer to the Parallel/SPI timing diagrams in the TRF7960-61 data sheet, SLOU186).
2. Wait for End of TX Interrupt to ensure successful transmission (refer to Section 3 on Interrupts for further details).
3. Wait for next interrupt. This can be due to any of the following:
   a. End of RX
   b. Collision
   c. No response

   Check the IRQ status register to determine the cause of the interrupt (for more details, refer to

the section on Interrupts).

If interrupt is due to End of RX, this means that the response (from the tag) is received in the FIFO without any error/collision. Read the FIFO to obtain the data (ATQB) received from the tag.

If interrupt is due to collision, use a flag to note that collision occurred.

If the interrupt is due to a No Response, ignore.

4. Send the Slot Marker command.

2.4 Send Slot Marker Command

The Slot Marker command is sent after receiving the ATQB message from the PICC to mark the start of next slot or earlier if no ATQB is received (no response interrupt).

The Slot Marker command format is as follows:

Table 2. Slot Marker Command Format

APn	CRC_B
8 bits	16 bits

The anti-collision prefix byte (APn) is coded as APn = (nnnn 0101)b where nnnn is as defined below.

Table 3.

nnnn	SLOT NUMBER
0001	2
0010	3
0011	4
....	....
1110	15
111	16

Pseudo-Code:

buf is an array that holds all the command/data bytes that are to be sent to the reader. number denotes the slot number in the anti-collision prefix byte.

```
buf[0] = 0x8f;                    /* Reset FIFO command */
buf[1] = 0x91;                    /* Send with CRC */
buf[2] = 0x3d;                    /* Write continuous from register 1D */
buf[3] = 0x00;                    /* Data for register 1D */
buf[4] = 0x10;                    /* Data for register 1E */
buf[5] = (number << 4) | 0x05;    /* Anti-collision prefix byte*/
```

Write buf[0] to buf[5] to TRF796x via SPI or Parallel mode (refer to the Parallel/SPI timing diagrams in the TRF7960-61 data sheet, SLOU186).

A detailed description of the firmware implementation of the anti-collision sequence is given in Figure 1 in the form of a flowchart.

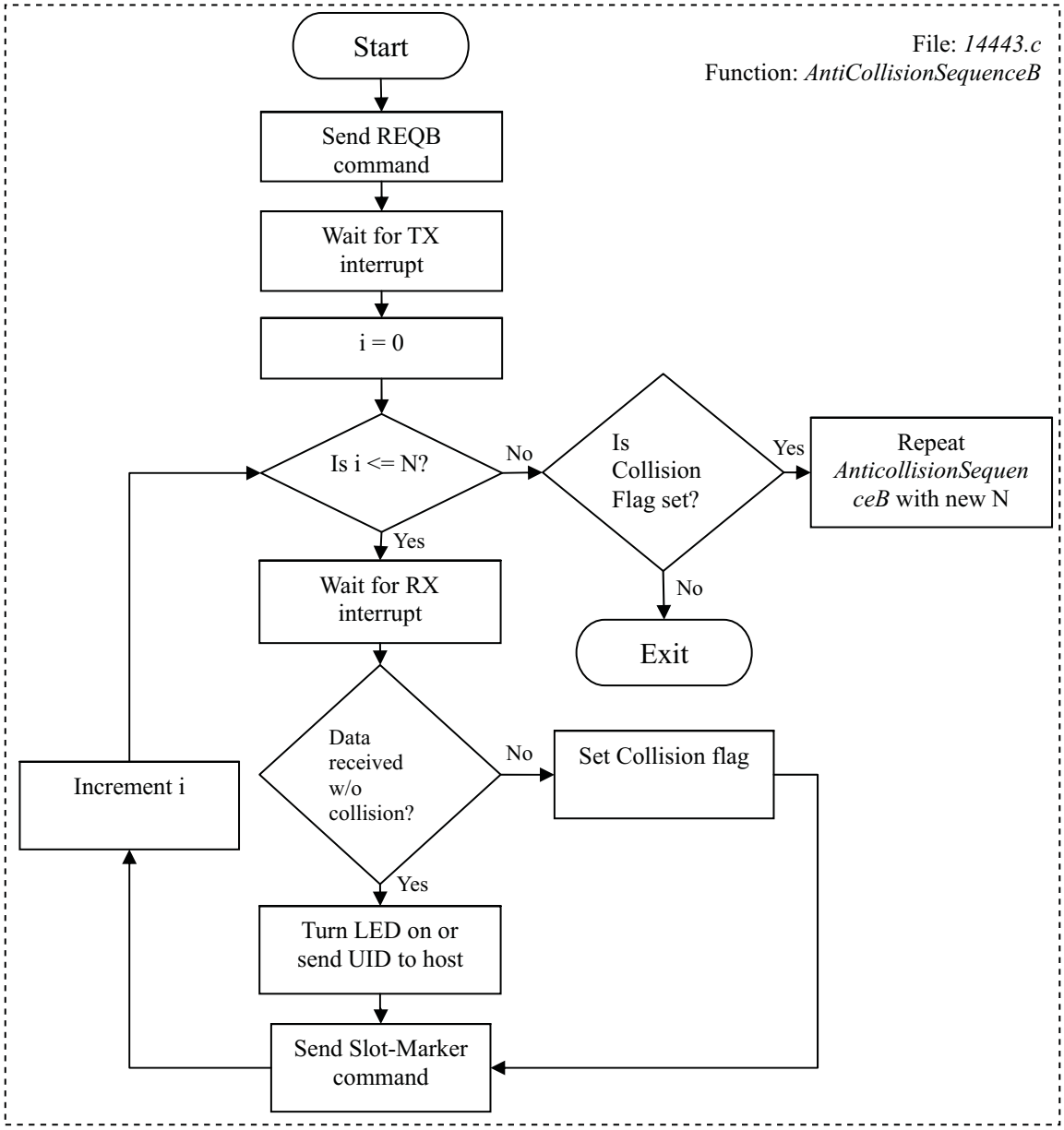

Figure 1. AntiCollisionLoop

Note: Due to the recursive nature of the anti-collision algorithm, there is a risk of stack overflow when collision occurs. It is highly recommended that the user implement stack overflow check in the firmware.

3 Interrupt Handler Routine

The reader which is a slave device has an IRQ pin to prompt/flag the MCU for attention in cases when the reader detects a response from the PICC/VICC. The interrupt handler routine described below determines how the IRQ should be handled.

The TRF796x IRQ status register (Table 5) is read to determine the cause of the IRQ. The following conditions (Table 4) are checked and appropriate actions taken:

Table 4. Inerrupt Conditions

NO.	CONDITION	ACTION
1	Transmission complete	Reset FIFO
2	Collision occurred	1. Read collision position register (TRF796x).(1)(2)(3) 2. Determine the number of valid bytes and bits. 3. Read the valid received bytes and bits in FIFO and write to local buffer. 4. Reset FIFO.
3	RX flag set (at End of RX)	1. Read FIFO status register (TRF796x) to determine the number of unread bytes and bits in FIFO. 2. Read the data in FIFO and write to local buffer. 3. Reset FIFO.
4	RX active and 9 bytes in FIFO	1. Read 9 bytes from FIFO. 2. Check if IRQ pin is still high. If yes, go to condition No. 3.
5	CRC error	Set error flag.
6	Byte framing error	Set error flag.
7	No-response time-out	
8	Any other	1. Reset FIFO. 2. Clear interrupt flag.

(1) Though registers 0Dh and 0Eh give the collision position, only register 0Eh is used because the anti-collision command in ISO 14443A is maximum only 7 bytes long. Hence 8 bits (0Dh) are enough to determine the position.

(2) The lower nibble of the Collision register (0Eh) has the bit count and that the upper nibble has the byte count. For example, if the Collision Position register holds the value 0x40, it means that the collision happened in the 4th byte on the bit 0.

(3) The anti-collision procedure in the ISO14443A standard is done in such a way, that the reader sends at least 2 bytes (cascade level and length information) in the anti-collision command. The collision position is counted from this reader command on. Therefore to know the number of valid bytes and bits, subtract 0x20 from the Collision Position register.

Table 5. IRQ Status Register

BIT	BIT NAME	FUNCTION	COMMENTS
B7	Irq_tx	IRQ set due to end of TX	Signals the TX is in progress. The flag is set at the start of TX, but the interrupt request is sent when TX is finished.
B6	Irq_srx	IRQ set due to RX start	Signals that RX SOF was received and RX is in progress. The flag is set at the start of RX, but the interrupt request is sent when RX is finished.
B5	Irq_fifo	Signals the FIFO is 1/3 > FIFO > 2/3	Signals FIFO high or low (less than 4 or more than 8).
B4	Irq_err1	CRC error	Reception CRC
B3	Irq_err2	Parity error	
B2	Irq_err3	Byte framing or EOF error	
B1	Irq_col	Collision error	For ISO14443A and ISO15693 single sub-carrier
B0	Irq_noresp	No response interrupt	Signal to MCU that next slot command can be sent.

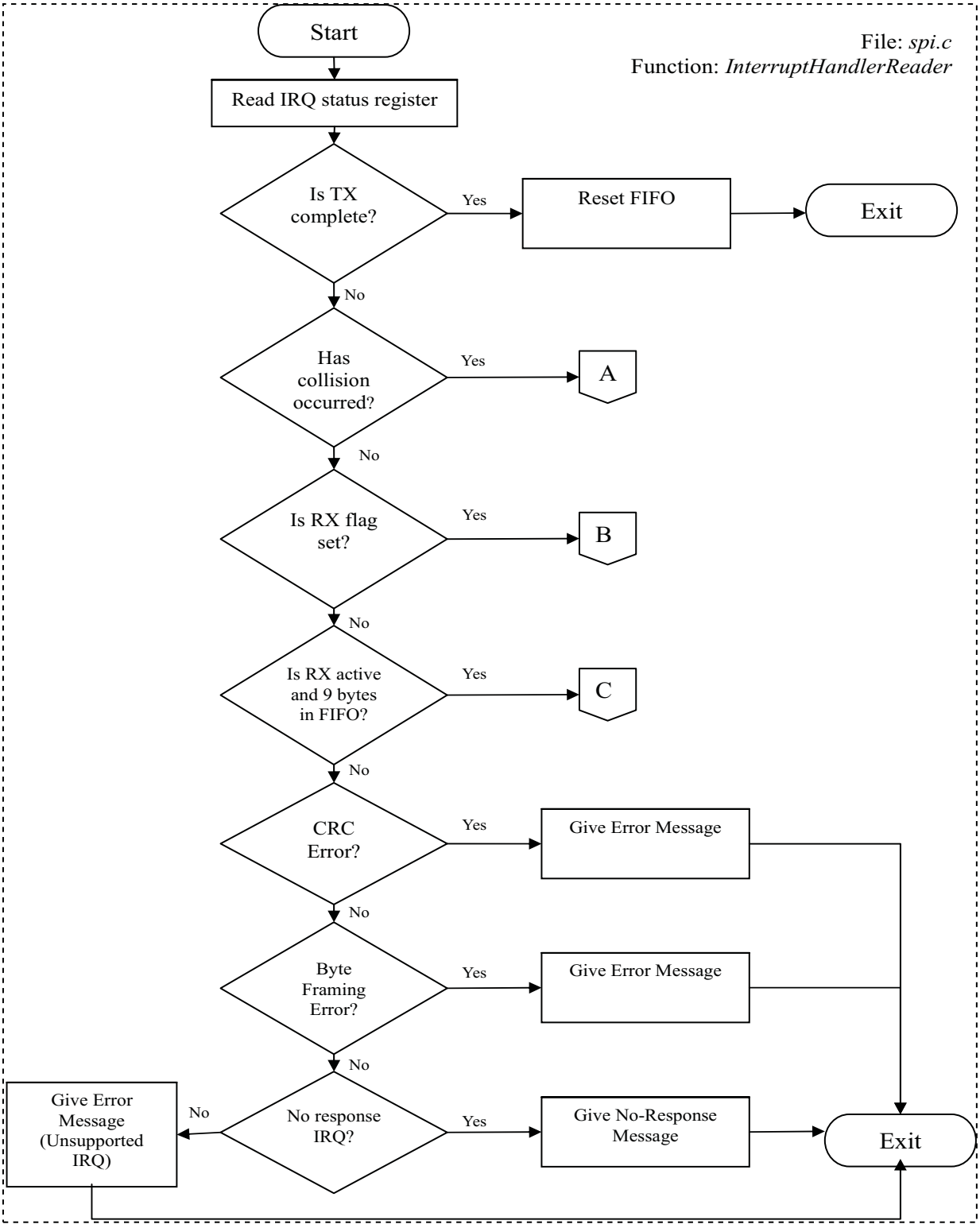

Figure 2. Inerrupt Handler Routine (1)

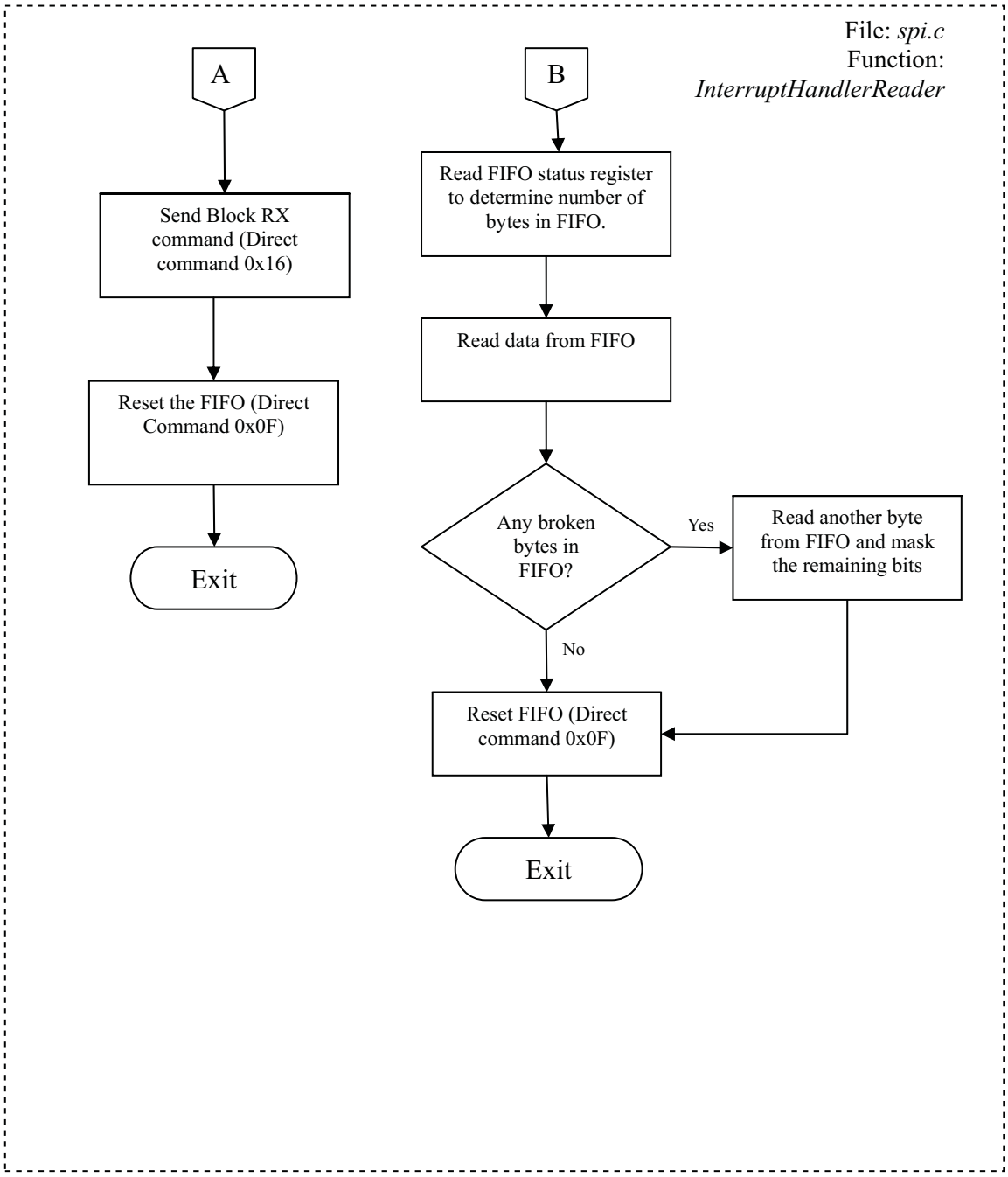

Figure 3. Interrupt Handler Routine (2)

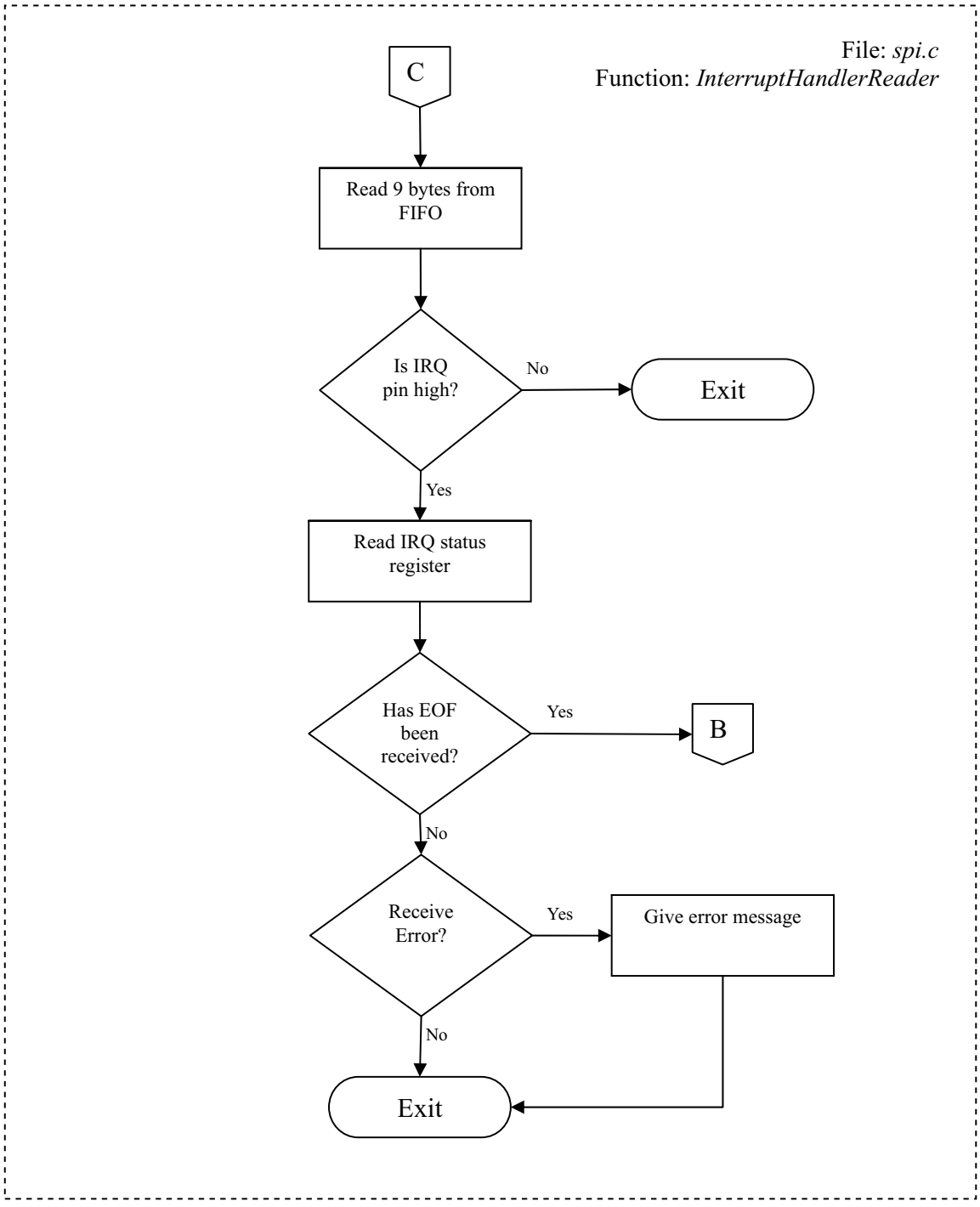

Figure 4. Inerrupt Handler Routine (3)

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DLP® Products	www.dlp.com	Broadband	www.ti.com/broadband
DSP	dsp.ti.com	Digital Control	www.ti.com/digitalcontrol
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Military	www.ti.com/military
Logic	logic.ti.com	Optical Networking	www.ti.com/opticalnetwork
Power Mgmt	power.ti.com	Security	www.ti.com/security
Microcontrollers	microcontroller.ti.com	Telephony	www.ti.com/telephony
RFID	www.ti-rfid.com	Video & Imaging	www.ti.com/video
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265