Nulling Input Offset Voltage of Operational Amplifiers

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ABSTRACT

The input offset voltage of operational amplifiers (op amps) arises from unavoidable mismatches in the differential input stage of the op-amp circuit caused by mismatched transistor pairs, collector currents, current-gain betas(β), collector or emitter resistors, etc. This application report describes the effects of mismatched components on the input offset voltage, and proposes using an external null circuit to reduce the input offset voltage of an amplifier. It also suggests a means for computing proper values of resistors in the null circuit in order to provide appropriate input-offset-voltage compensation.

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1 Introduction

Operational amplifiers (op amps) may exhibit an input offset voltage (V_{OS}) in the range of μV to mV. Since the active and passive devices in the internal op-amp circuit have inherent temperature-dependent parameters, so does the input offset voltage. The op-amp data sheets usually specify the typical and maximum values, as well as the temperature coefficient of the input offset voltage. However, the data sheets do not present the polarity of V_{OS} because the change in the input offset voltage caused by component mismatches is unknown.

The op-amp data sheets usually recommend the use of an external potentiometer connected to the null pins to zero V_{OS} at room temperature; this method is first shown in detail. In addition, an alternative approach is also presented that minimizes the input-offset-voltage range over temperature by adding a resistor with a known temperature coefficient (Ω/°C) to the null circuit. This resistor is connected to either side of the null pins, depending on the polarity of $V_{OS,}$ and serves to balance the voltages at the input terminals of an op amp.

2 Effect of Component Mismatches in the Input Offset Voltage

Consider the simplified input-stage circuit of the operational amplifier in Figure 1. The input offset voltage of the op amp results from mismatches in collector/emitter resistors and the transistor pair of the differential input. Each of these mismatches is examined separately below.

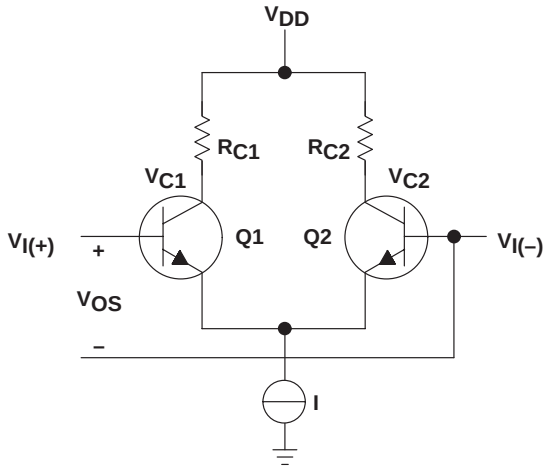

Figure 1. The Simplified Differential Input Circuit

2.1 Effect of Collector-Resistor (R_c) Mismatch on V_{os}

When the transistors Q_1 and Q_2 in Figure 1 are perfectly matched, the current, I, is divided equally between them.

Let $R_c = \frac{R_{c1} + R_{c2}}{2}$ and $\Delta R_c = R_{c1} - R_{c2}$

Then, $R_{c1} = R_c + \frac{\Delta R_c}{2}$ and $R_{c2} = R_c - \frac{\Delta R_c}{2}$

Thus, the output voltage, V_o, is [1a]:

$$V_o = V_{c2} - V_{c1} = \left(V_{DD} - \frac{\alpha I}{2} R_{c2}\right) - \left(V_{DD} - \frac{\alpha I}{2} R_{c1}\right) = \left[V_{DD} - \frac{\alpha I}{2}\left(R_c - \frac{\Delta R_c}{2}\right)\right]$$

$$- \left[V_{DD} - \left(\frac{\alpha I}{2}\right)\left(R_c + \frac{\Delta R_c}{2}\right)\right] = \Delta R_c \frac{\alpha I}{2}$$

The input offset voltage is $V_{os} = \frac{V_o}{A_d} = \frac{V_o}{g_m R_c} = \frac{\alpha\left(\Delta R_c\right)\left(\frac{I}{2}\right)}{\frac{\frac{\alpha I}{2}}{V_T} R_c} = V_T \frac{\Delta R_c}{R_c} = \frac{kT}{q} \frac{\Delta R_c}{R_c}$ (1)

where

$\alpha = \frac{\beta}{\beta + 1}$; differential gain : $A_d = g_m R_c$; $g_m = \frac{I_c}{V_T}$ and $V_T = \frac{kT}{q}$ is the thermal voltage.

Here k is Boltzmann's constant and q is the charge on the electron

2.2 Effect of Mismatched Transistors on V_{os}

Mismatch in transistors usually occurs because of mismatches in emitter areas for bipolar junction transistors (BJT) and W/L ratios for MOSFETs. Since either BJT or MOSFET transistors can be used in the differential input stage, each is analyzed separately below.

Mismatched emitter-base junction areas of BJTs give mismatches in current saturation junction I_S.

Let $I_S = \frac{I_{s1} + I_{s2}}{2}$ and $\Delta I_S = I_{s1} - I_{s2}$

Then, $I_{s1} = I_s + \frac{\Delta I_S}{2} = I_s\left(1 + \frac{\Delta I_S}{2I_s}\right)$ and $I_{s2} = I_s - \frac{\Delta I_S}{2} = I_s\left(1 - \frac{\Delta I_S}{2I_s}\right)$

Assume that the voltages across base-emitter junctions are equal($V_{BE1} = V_{BE2}$); then

$$I_{c1} = I_{s1}e^{\left(\frac{V_{BE1}}{V_T}\right)} = I_s e^{\left(\frac{V_{BE1}}{V_T}\right)}\left(1 + \frac{\Delta I_S}{2I_s}\right) = \frac{\alpha I}{2}\left(1 + \frac{\Delta I_S}{2I_s}\right) = I_c\left(1 + \frac{\Delta I_S}{2I_s}\right)$$

$$I_{c2} = I_{s2}e^{\left(\frac{V_{BE2}}{V_T}\right)} = I_s e^{\left(\frac{V_{BE2}}{V_T}\right)}\left(1 - \frac{\Delta I_S}{2I_s}\right) = \frac{\alpha I}{2}\left(1 - \frac{\Delta I_S}{2I_s}\right) = I_c\left(1 - \frac{\Delta I_S}{2I_s}\right)$$

Assume R_{c1} and R_{c2} are perfectly matched ($R_{c1} = R_{c2}$). Thus, the output voltage V_o is:[1b]

$$V_o = V_{c2} - V_{c1} = \left(V_{DD} - I_{c2}R_{c2}\right) - \left(V_{DD} - I_{c1}R_{c1}\right) = \left(I_{c1} - I_{c2}\right)R_c$$

$$= R_c\frac{\alpha I}{2}\left[\left(1 + \frac{\Delta I_S}{2I_s}\right) - \left(1 - \frac{\Delta I_S}{2I_s}\right)\right] = \frac{\alpha I}{2}\frac{\Delta I_S}{I_S}R_c$$

$$V_{os} = \frac{V_o}{A_d} = \frac{V_o}{g_m R_c} = \frac{\frac{\alpha I}{2}\frac{\Delta I_S}{I_S}R_c}{\frac{\frac{\alpha I}{2}}{V_T}R_c} = V_T\frac{\Delta I_S}{I_S} = \frac{kT}{q}\frac{\Delta I_S}{I_S} \quad (2)$$

Consider the mismatch in W/L ratios for MOSFETs in Figure 2.

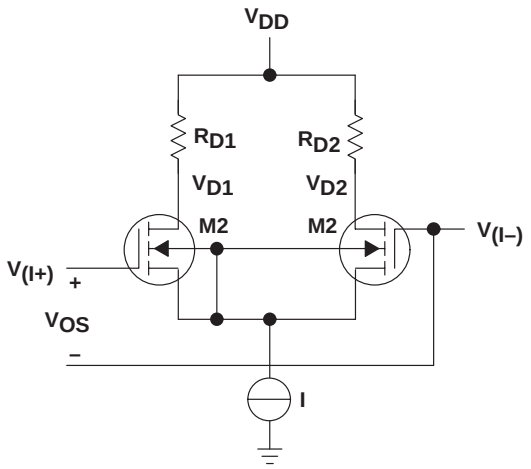

Figure 2. The Simplified Differential Input Circuit With MOSFET

$$\text{Let} \quad W/L = \frac{(W/L)_1 + (W/L)_2}{2}; \quad \Delta(W/L) = (W/L)_1 - (W/L)_2$$

$$\text{Then,} \quad (W/L)_1 = (W/L) + \frac{\Delta(W/L)}{2} = \frac{W}{L}\left(1 + \frac{\Delta(W/L)}{2(W/L)}\right)$$

$$\text{and} \quad (W/L)_2 = (W/L) - \frac{\Delta(W/L)}{2} = \frac{W}{L}\left(1 - \frac{\Delta(W/L)}{2(W/L)}\right)$$

Assume that there is no modulation effect (λ=0), R_{D1} and R_{D2} are perfectly matched, and M_1 and M_2 operate in the saturation region.

$$I_{D1} = \frac{K'_N}{2}\left(\frac{W}{L}\right)_1\left(V_{GS1} - V_{T1}\right)^2 = \frac{K'_N}{2}\left(\frac{W}{L}\right)\left(V_{GS1} - V_{T1}\right)^2\left(1 + \frac{\Delta(W/L)}{2(W/L)}\right) = \frac{I}{2}\left(1 + \frac{\Delta(W/L)}{2(W/L)}\right)$$

$$I_{D2} = \frac{K'_N}{2}\left(\frac{W}{L}\right)_2\left(V_{GS2} - V_{T2}\right)^2 = \frac{K'_N}{2}\left(\frac{W}{L}\right)\left(V_{GS2} - V_{T2}\right)^2\left(1 - \frac{\Delta(W/L)}{2(W/L)}\right) = \frac{I}{2}\left(1 - \frac{\Delta(W/L)}{2(W/L)}\right)$$

The output voltage V_o will be:[1c]

$$V_o = V_{D2} - V_{D1} = \left(V_{DD} - I_{D2}R_{D2}\right) - \left(V_{dd} - I_{D1}R_{D1}\right) = R_D\left(I_{D1} - I_{D2}\right) = R_D\frac{I}{2}\frac{\Delta(W/L)}{(W/L)}$$

$$V_{os} = \frac{V_o}{A_d} = \frac{V_o}{g_m R_D} = \frac{R_D\,\frac{I}{2}\,\frac{\Delta(W/L)}{(W/L)}}{\frac{I}{V_{GS} - V_T}R_D} = \frac{V_{GS} - V_T}{2}\,\frac{\Delta(W/L)}{(W/L)} \qquad (3)$$

where V_{GS} is the gate-source voltage, and the threshold voltage V_T is dependent on temperature since [2]

$$V_T = V_{TO} + \gamma\left(\sqrt{2\phi_F + V_{BS}} - \sqrt{2\phi_F}\right)$$

where $V_{TO} = -\frac{kT}{q} \ln \frac{N_G N_B}{n_i^2} - \frac{Q_{ox}}{C_{ox}} + 2\phi_F \pm \frac{Q_D}{C_{ox}}$

For all three of these cases, the input offset voltage of the amplifier mostly has contributions from the mismatches in those components as shown in Equations 1, 2, and 3. In addition, the V_{os} is obviously dependent on temperature through the parameter V_T of the transistors.

3 External Null Circuit

Because of mismatches in any of the aforementioned components, current flows into the two branches of the input differential amplifier unequally. Therefore, adding the appropriate R_1 and R_2 to the null pins balances the voltage at the two input terminals. Figure 3 shows the null pins connected in the simplified circuit of the input stage.

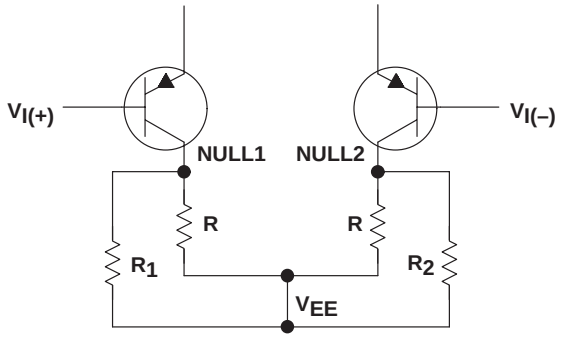

Figure 3. The Null Pins Connected to the Op Amp

An input-offset-voltage measurement is determined by the difference in voltage between the two input terminals of the op amp, i.e., $V_{os} = V_{I(-)} - V_{I(+)}$. If V_{os} is negative, then $V_{I(-)}$ is smaller than $V_{I(+)}$ so more resistance needs to be added to the null2 pin (which ties to the inverting input branch) in order to produce more voltage at this node; thus, V_{os} is less negative, and vice versa for the case of positive V_{os}. Hence, the absolute V_{os} becomes smaller for a given temperature. This report examines the behaviors of the input offset voltage over temperature for two amplifiers. One amplifier is a low-speed op amp with a small input offset voltage (μV). The second amplifier is a high-speed op amp with a large input offset voltage (mV). The same nulling-offset approach is taken for both op amps.

3.1 Effect of the Potentiometer on V_{os}

The null circuit shown in Figure 4 was set up using a potentiometer. The two circuits shown here are equivalent.

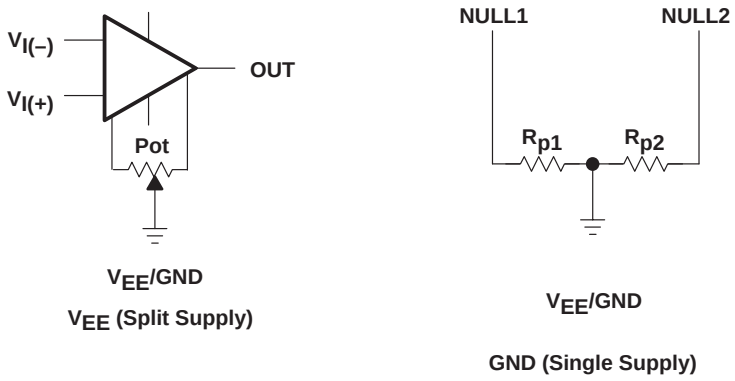

Figure 4. The Potentiometer in the Null Circuit

3.1.1 TLC070

The results shown in Figure 5 show that the input offset voltage of this op amp is negative (≅ –100 μV) at room temperature, i.e., $V_{I(–)} < V_{I(+)}$. Adjusting the potentiometer simply provides the appropriate values of R_{p1} and R_{p2} (see Figure 4) and serves to increase the voltage at the inverting input, canceling out the voltage at the noninverting input. Therefore, it brings V_{OS} closer to zero at room temperature. However, the temperature coefficient of the input offset voltage of this op amp remains fairly constant.

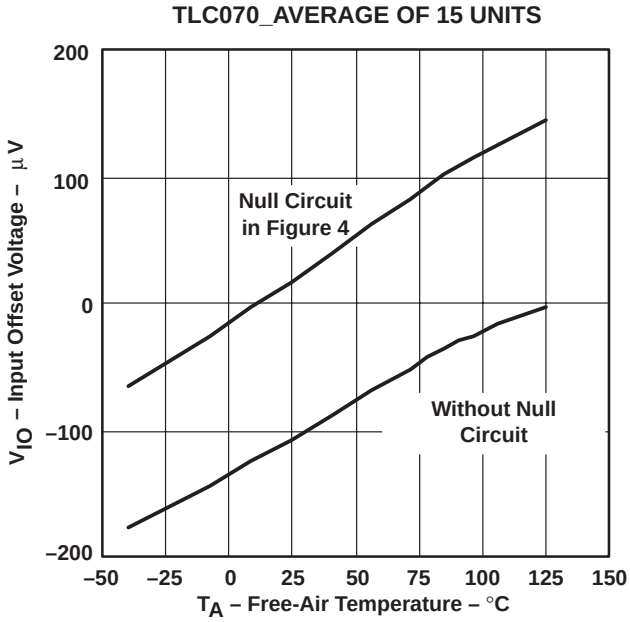

Figure 5. V_{OS} of TLC070 With the Potentiometer in the Null Circuit

3.1.2 THS4011

While the TLC070 has a low-input-offset voltage to start with, the THS4011 does not. It is a high-speed op amp whose offset voltage is generally in the mV range. Adjusting the potentiometer of the null circuit not only zeros V_{OS} at room temperature but also compensates V_{OS} variation over temperature, and the input offset voltage varies from 1.87 mV to 495 μV. Unlike the TLC070, the V_{OS} temperature coefficient of this op amp reduces dramatically. Figure 6 shows the results.

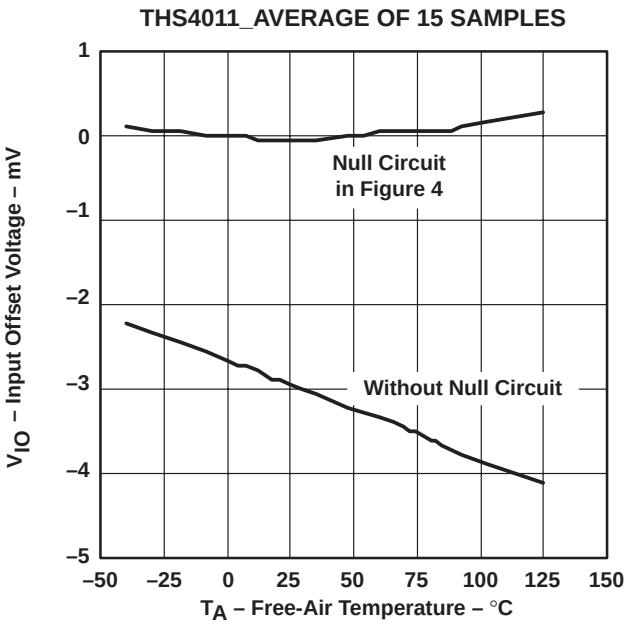

Figure 6. V_{OS} of TLC4011 With the Potentiometer in the Null Circuit

3.2 Effect of Additional Temperature-Coefficient Resistors on V_{OS}

The results in Figure 5 show that the V_{OS} temperature coefficient of the TLC070 remains fairly constant both with and without the potentiometer in the null circuit. The addition of a known-temperature-coefficient resistor in series with the potentiometer can effectively cancel out some of the temperature dependence inherent in the op amp. Figure 7 shows another experimental setup for nulling input offset voltage that attempts to reduce the variation in the input offset voltage with temperature.

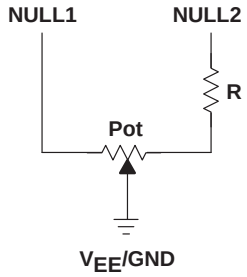

Figure 7. The Null Circuit of the Potentiometer in Series With a Resistor

3.2.1 Low Temperature-Coefficient Resistor

The addition of the temperature-dependent resistor, R, to the null circuit shown in Figure 7 is another V_{OS} compensation approach. This resistor could be of surface-mounted or thin-film type with a temperature coefficient of ±100–200 ppm/°C.

Because typical surface-mounted and thin-film resistors have roughly the same, small temperature coefficients, adding either type to the null circuit shows insignificant decrease in the temperature dependence of V_{OS} for this op amp. The results in Figure 8 show that the sensitivity of V_{OS} to temperature with and without the null circuit (Figure 7) are the same in the temperature range from –55°C to 85°C. Furthermore, the resistor only slightly affects V_{OS} between 85°C and 125°C.

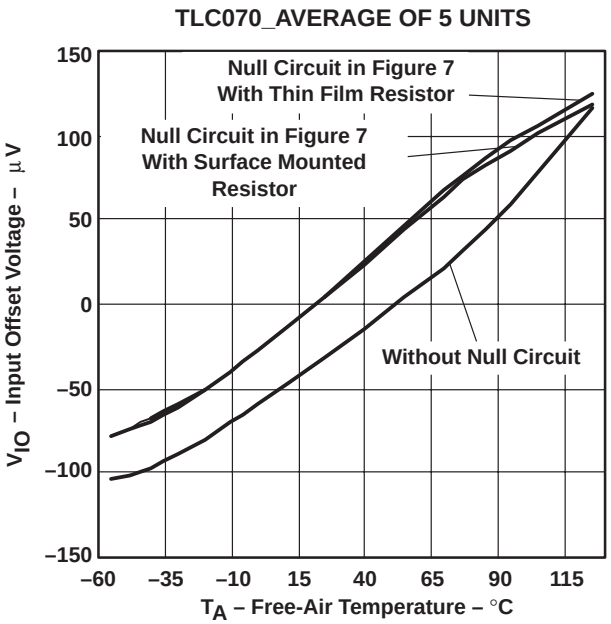

Figure 8. V_{OS} Variation of TLC070 With the Low Temperature-Coefficient Resistors in the Null Circuit

3.2.2 Effect of High Temperature-Coefficient Resistor (Thermistor) on V_{OS}

Using the potentiometer and a low-temperature-coefficient resistor in the null circuit shows little effect on V_{OS} temperature sensitivity for this op amp. An alternative way to improve V_{OS} is to employ a thermistor, R_t, which has a high, negative, temperature coefficient. Figure 9 shows plots for various values of thermistors from –40°C to 125°C. The temperature coefficients of these thermistors are relatively high (900 Ω/°C).

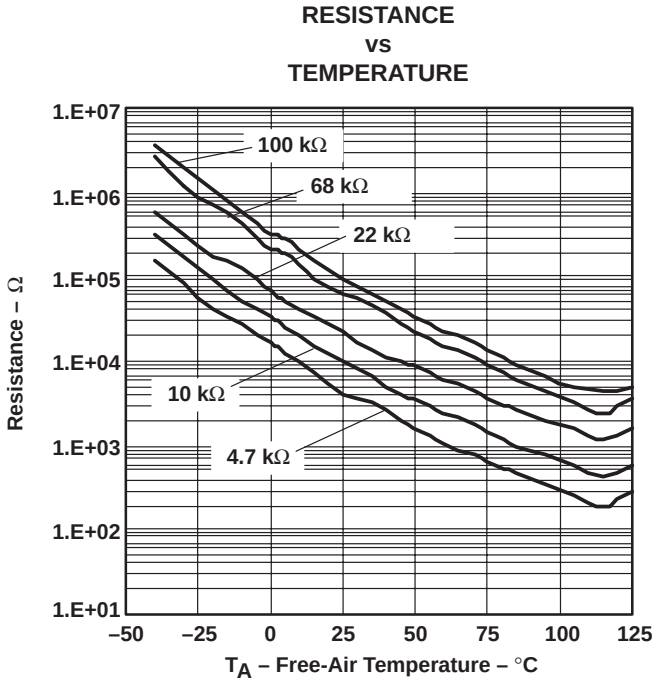

Figure 9. Temperature Dependence of Resistance for Five Thermistors

Because of the extremely high temperature coefficient of the thermistor, R_t, one must connect it in parallel with the resistor R (this resistor is sunstantially independent of temperature) so that one is able to control the variation of V_{os} with temperature. This parallel-resistor combination is connected to the null pin at the inverting-input branch or at the other null pin, depending on the following two criteria: a) the orientation of the null pins in the internal op-amp circuit; b) negative or positive temperature coefficients of the input offset voltage. Figure 10 shows a null circuit that has the parallel-resistor combination added.

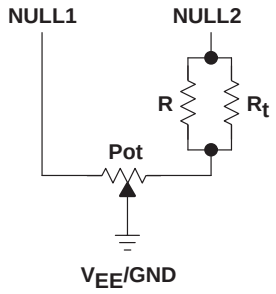

Figure 10. The Null Circuit With the Potentiometer in Series With Parallel Resistors

To adopt this approach, one must determine suitable values of the resistors R and R_t that give an appropriate compensation. One way of doing this is to connect the two leads of the potentiometer to the two null pins, and the wiper to the Vee/GND pin, then measure the resistances R_{p1} and R_{p2} of the potentiometer at –40°C and 125°C when $V_{os} \cong 0$ V. The change in resistance, ΔR, is the difference in resistance of R_{p1} or R_{p2} from –40°C to 125°C. This ΔR should be the same as the ΔR_{eq} of a parallel-resistor combination ($R//R_t$) from –40°C to 125°C. The thermistor, R_t, has a very large, negative, temperature coefficient, i.e., it is quite small at high temperature and very large at low temperature. Consequently, R dominants at low temperature, whereas R_t dominants at high temperature.

3.2.3 TLC070

Performing this calculation for the TLC070 gives ΔR approximately equal to 5 kΩ. The values of R and R_t shown in Table 1 were selected.

Table 1. Values of the Resistors in the Null Circuit of Figure 10

TEMPERATURE	R = 6kΩ at 25°C	Rt = 10kΩ at 25°C	R//Rt	ΔR
–40°C	5.99 kΩ	300 kΩ	5.88 kΩ	5.33 kΩ
125°C	6.01 kΩ	605 Ω	550 Ω	

Recall that the V_{os} temperature coefficient of this op amp with the potentiometer in the null circuit is positive (1 μV/°C), as shown in Figure 5. At low temperature,V_{os} is negative; at high temperature it is positive. Obviously, the parallel resistor combination must be connected to the null pin that increases the voltage at low temperature and decreases it at high temperature at the inverting input. With the null circuit shown in Figure 10, V_{os} is pulled up into the vicinity of zero at –40°C and also is pulled down close to zero at 125°C. As shown in Figure 11, the variation in V_{os} is reduced from 174 μV to 30 μV over the temperature range from –40°C to 125°C.

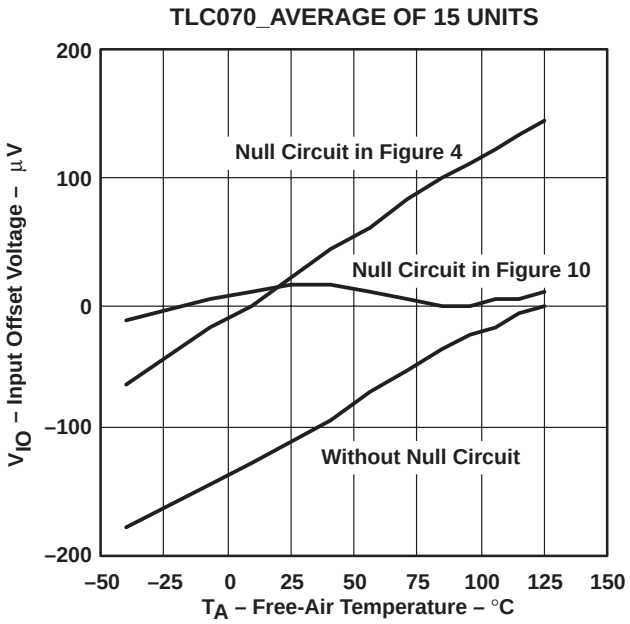

Figure 11. V_{os} With R_{eq} = 6 kΩ//10 kΩ in Series With the Potentiometer in the Null Circuit

3.2.4 THS4011

As shown in Figure 6, the potentiometer in the null circuit yields greatly improved compensation for this op amp. However, it would be interesting to see if even better compensation could be obtained (i.e., V_{os} variation even smaller than 495 μV over temperature range from –40°C to 125°C) if one carried out the same experiment as was done for the TLC070.

Since V_{os} for this op amp is quite large (mV range), it is more difficult to zero V_{os} in order to compute ΔR as accurately as for the TLC070. Measurement of ΔR was obtained by using the same method as the TLC070. Tables 2 and 3 present the resistor values for the first and second attempts.

Table 2. Values of Resistors in the Null Circuit of Figure 10 for the First Attempt

TEMPERATURE	R=1 kΩ at 25°C	Rt =10kΩ at 25°C	R//Rt	ΔR
–40°C	0.99 kΩ	300 kΩ	980 Ω	602 Ω
125°C	1.01 kΩ	605 Ω	378 Ω	

In the first attempt, the values of R and R_t shown in Table 2 were used. The results in Figure 12 show that this op amp is overcompensated by the large thermistor R_t and the small resistor R.

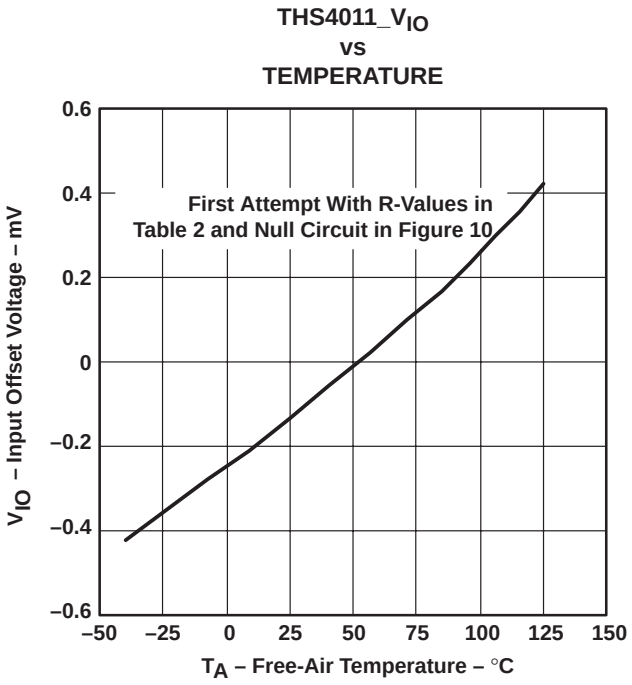

Figure 12. V_{os} With R_{eq} = 1 kΩ//10 kΩ in Series With the Potentiometer in the Null Circuit

As shown in Figure 12, the input offset voltage for this op-amp is similar to the TLC070 shown in Figure 5 except that V_{os} is larger; hence, the same technique applies to this case. To reduce the V_{os} variation with temperature, one must increase ΔR by increasing the value of the resistor R and decreasing the thermistor R_t. At low temperature, more voltage is generated at the inverting input node due to increasing R which results in $V_{os} = V_{I(-)} - V_{I(+)}$ being smaller. At high temperature, $V_{I(-)}$ is reduced due to decreasing R_t, then V_{os} also becomes smaller. As shown in Figure 13, in the second attempt, using the R and R_t values given in Table 3 results in the input offset voltage being reduced from 1.87 mV to 300 μV over the temperature range from –40°C to 125°C.

Table 3. Values of Resistors in the Null Circuit of Figure 10 for the Second Attempt

TEMPERATURE	R = 20 kΩ at 25°C	Rt = 2.2kΩ at 25°C	R//Rt	ΔR
–40°C	19.99 kΩ	36 kΩ	12.85 kΩ	12.8 kΩ
125°C	20.01 kΩ	35 Ω	34.9 Ω	

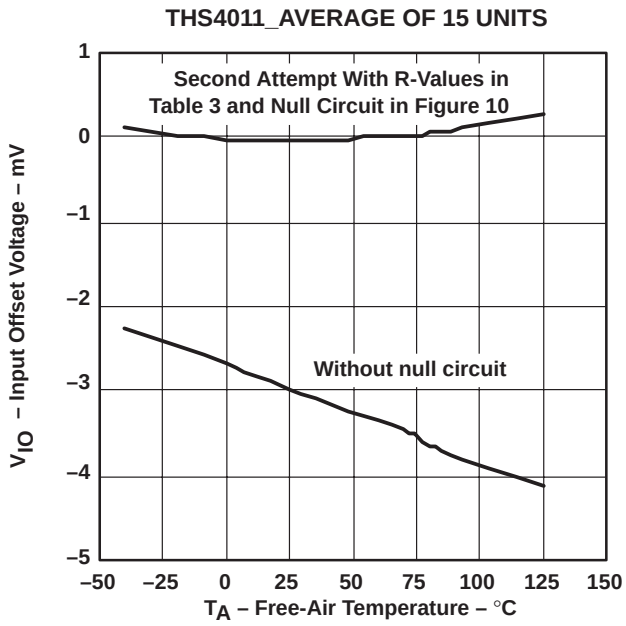

Figure 13. V_{OS} With R_{eq} = 20 kΩ//2.2 kΩ in Series With the Potentiometer in the Null Circuit

4 Summary

This report shows how to reduce the input offset voltage of operational amplifiers. Using the potentiometer itself in the null circuit as shown in Figure 3 is recommended for all single op amps that have the null pins. The input-offset-voltage range is reduced by simply adjusting the potentiometer. This is the simplest implementation.

Adding the thermistor to the null circuit in parallel with a very-low-temperature-coefficient resistor shows significant improvement in the input-offset-voltage sensitivity to temperature, but it is indeed tedious and time consuming work because one has to compute the appropriate ΔR. The V_{os} variations are not the same for every op amp because the input offset voltage of amplifiers varies from device to device. Table 4 summarizes the variation of input offset voltage with temperature for the TLC070 and THS4011 devices with the different null circuits presented in this report.

Table 4. Summary of V_{OS} Results for TLC070 and THS4011 With Various Null Circuits.

		Vos VARIATION OVER TEMPERATURE				
		WITHOUT NULL CIRCUIT	WITH NULL CIRCUIT			
			POT	POT AND RESISTOR	POT, RESISTOR, AND THERMISTOR	
TLC070	–40°C–125°C	174 μV	210 μV	194 μV(SM) 200 μV(TF)	30 μV	
	0°C–70°C	82 μV	75.8 μV	92.2 μV(SM) 96 μV(TF)	15 μV	
THS4011	–40°C–125°C	1.87 mV	495 μV		1st attempt	2nd attempt
					846 μV	300 μV
	0°C–70°C	794 μV	161 μV		330 μV	74 μV

5 References

1. Sedra, A. S. and K. S. Smith, *Microelectronic Circuits*, Oxford University Press, 1991; (a) p. 424; (b) p. 425; (c) p. 452.
2. Laker, K. R. and W. M. C. Sansen, *Design of Analog Integrated Circuits and Systems*, McGraw-Hill, New York, 1994.

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