Design Guide 92 NLA Array QFN

Texas Instruments has developed the Array QFN for the next generation small form factor, high density, QFN type packaging solutions. The Array QFN package has the intrinsic ability to support challenging high density interconnect requirements within a small footprint without sacrificing performance. The array QFN package leverages manufacturing technology to support an integrated arrayed solution with superior thermal & electrical characteristics, thus enabling high-power, and high-frequency applications support.

Note: This application report is intended as a guide. Precise process development and experimentation are needed to optimize specific applications/performance.

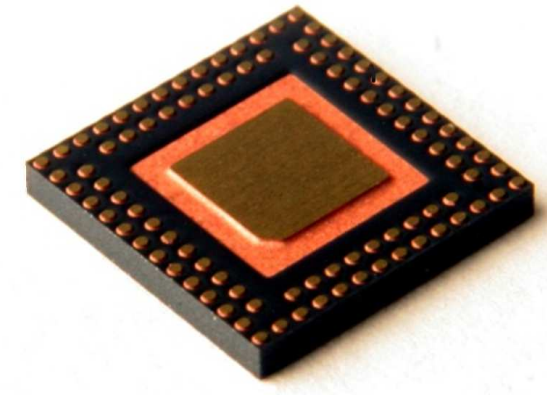


Figure 1. Example 92-NLA Package Picture Texas Instruments Array Quad Flat No Lead

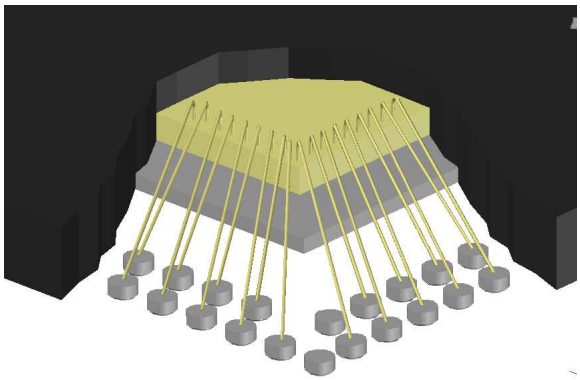


Figure 2. Illustration 92-NLA Overview

The Array QFN Package maximum thickness is 1.00 mm. The package seating height will be dependent upon the solder paste volume as well influenced by the land pad design.

1 Packaging Handling

1.1 ESD Protective Measures for IC Components

Virtually all semiconductor devices can be subject to damage by an electrostatic discharge (ESD) event. While some devices can withstand tens of thousands of volts before damage, other devices can be damaged by much lower voltages. By utilizing proper precautions and controlled handling procedures customers can insure a higher level in reliability and quality in their end products.

1.2 MSL labeling

TI surface-mount products are tested for moisture sensitivity using industry testing procedures outlined in IPC/JEDEC J-STD-020D.1, JEDEC levels 1 through 6 define relative levels of moisture sensitivity with Level 1 denoting a package is not moisture sensitive.

By nature of their construction materials plastic IC packages absorb moisture from the surrounding environment; and its from this trapped moistures conversion to steam during a reflow process that a failure from internal delamination in phenomenon called popcorning. It is also worthy that damage from this affect might not be visible with external inspection. It's therefore highly recommended an inventory control program is in place controlling both floor life once a devices packing is opened as well a devices shelf life.

2 Manufacturing Considerations

2.1 Typical Board Mount / Assembly Process Flow

PCB – Land pattern design & pad plating requirements

Screen printing solder paste

Monitoring the solder paste volume (uniformity)

Package placement & mounting using standard SMT equipment

Inspection (X-ray) prior to reflow, insure placement accuracy review for defects (i.e. bridging, missing etc)

Solder reflow (optional: flux residue cleaning if required)

Inspection after reflow checking for defects

2.2 SMT Process

When attaching the array QFN's exposed die pad and leads to a PCB it is paramount to achieve an optimal solder joint known to offer low resistance and high board level reliability while still achieving a high-yielding assembly process. A few key focus areas and their contributing factors are highlighted in Table 1

Table 1. Essentials for Assembly Quality

Solder paste quality	Uniform viscosity and texture, free from foreign material, protected from drying out while on stencil. Shipment and storage held within recommended environmental conditions. Inventory controlled to insure expired materials are removed from manufacturing inventory.
Land Pattern / Stencil	PCB land patterns that meet industry design requirements (IPC-2221/2222) for land pattern and matching stencil (IPC7528B/IPC-SM-7351A / IPC-SM-782) that not only prints but correctly releases optimal solder amount.
PCB quality	Manufactured using manufacturing acceptance standards & procedures (IPC-A-610). Stored correctly with clean, flat, solder lands free of oxidation, corrosion, or any solder mask residue. Inventory controlled stock used within recommended dates.
Placement accuracy	Component placement accuracy to solder pads is contingent upon several factors, including fiducial marks; datum point location; size of printed circuit board; flatness of printed circuit board; mounting equipment used; etc. Array QFN packages will require a little higher placement precision then standard QFN's due to additional terminal rows.
Solder volume	Solder volume control is important to ensure optimum contact of all intended solder connections while controlling to insure bridging is not occurring.
Solder reflow profile	A solders reflow temperature profile is dependent on the PCB design, thickness, components peak temperature, moisture sensitivity level (MSL), component density, and solder manufactures recommended temperature profile for paste being used. It is therefore recommended a reflow profile be tailored for each PCB / solder combination used in an assembly.
Inspection / Cleanliness of PCB	Post reflow inspection is and integral part of overall systems quality, providing ability to adjust and/or repair work in process as well continual feedback to assembly process. Flux Residue, Rosin, water-soluble fluxes, circuit board resins and epoxies, component materials, and/or other contaminates can contribute to quality issues within the assembly process that should be monitored.

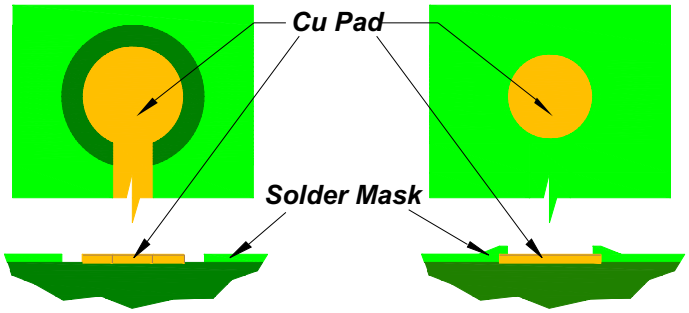
2.3 Printed Circuit Board (PCB) Design Guidelines

One of the key efforts in implementing the Array QFN package is design of the land pad. The Array QFN has exposed pads at the package bottom. Electrical and mechanical connections between the component and PCB are normally made by soldering the part using screen printed solder paste and reflowing after placement. To ensure consistent solder joint geometries and superior reliability results it is essential the land pattern design considers the components exposed interconnection pattern.

2.4 PCB Design Recommendations

Generally printed board design and construction is a key factor in achieving high reliability. It is therefore advisable that selected PCB manufacturer meet solderability requirements within ANSI/J-STD-003, while additionally meeting manufacturing design requirement in IPC-2220 series plus IPC-7351 and/or for high frequency applications IPC-2141 & IPC-2251.

2.5 Land Pad Styles



NSMD-Non Solder Mask Defined ***SMD-Solder Mask Defined***

Figure 3.

Although TI recommends NSMD (Non Solder Mask Defined) pads over SMD (Solder Mask Defined) pads when surface mounting the Array QFN, both types can be utilized. Benefits of NSDM include: allows tighter tolerance on copper etching, improved routing while providing a larger solderable area and edges free from solder mask, thus providing improved solder-joint reliability thought a higher wettable surface area with a decreased stress rate within the solder joints. When routing signals between periphery pads the trace should be centered in order to maximize solder mask coverage for board fabrication purposes.

IPC-7351 is one of the industry standard guidelines for developing PCB pad patterns. Because the Array QFN is a newer package style, this application report is intended as a guide and should be used in combination with applicable IPC design standards while designing an optimum PCB land pattern for devices application and board type being used.

2.6 Land Pattern Design Recommendations

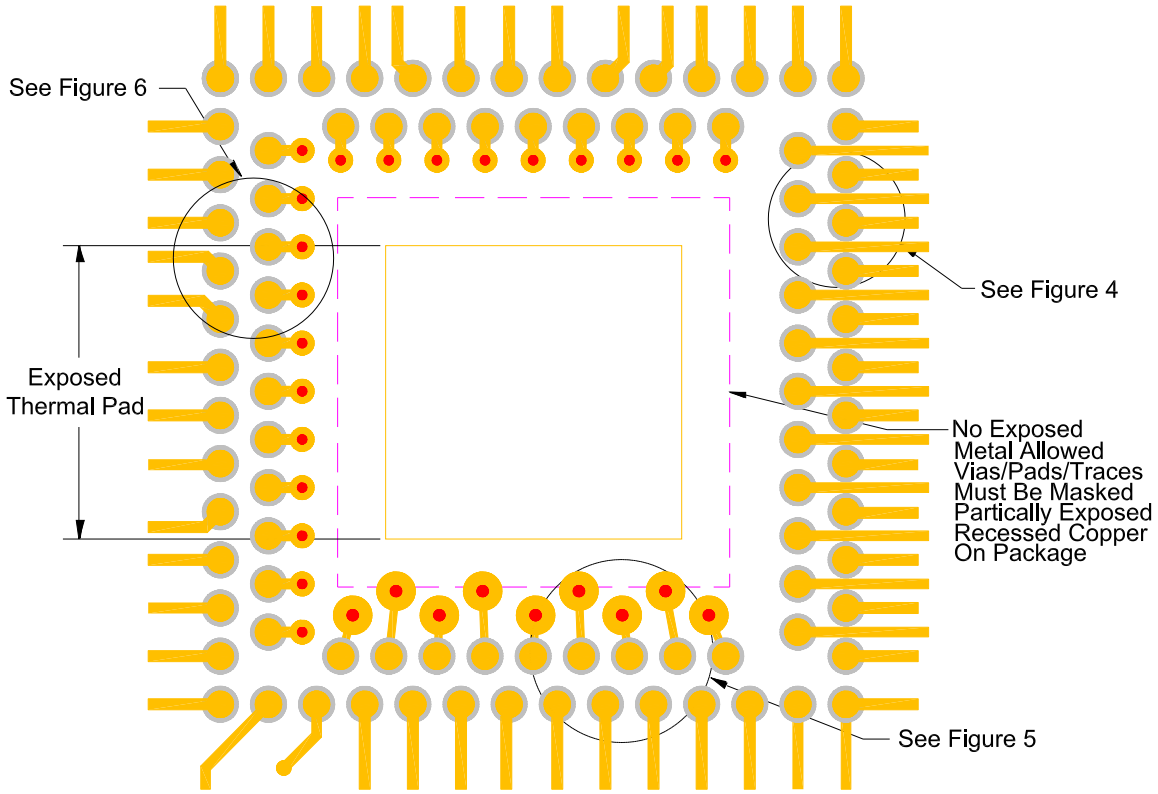


Figure 4.

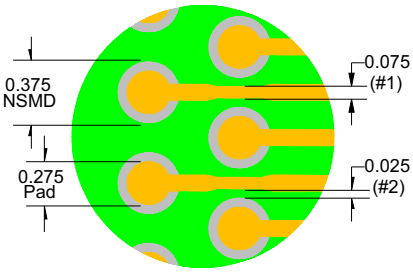


Figure 5. Example Inner Row Escapes Top Layer

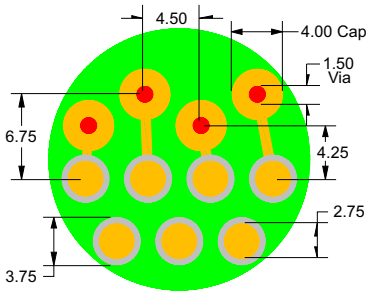


Figure 6. Example Design of Inner Via Escapes to Any Layer

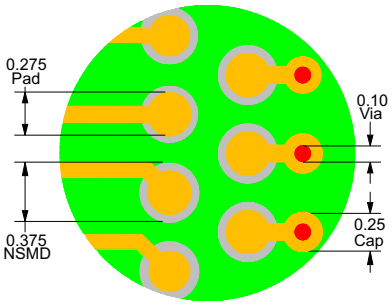


Figure 7. Example Inner Row Via Escapes to Layer 2

Notes:

1. 0.075 wide trace normally too narrow for outer layers.
2. Customers should determine their applications required electrical spacing requirements. Optimally spacing ≥0.05 will improve shorting potential.
3. Customers should contact their board fabrication site for recommended solder mask tolerances, recommended via sizes, and via tenting recommendations for vias placed in thermal pad
4. If microvias are placed inside solder pads it's recommended that flatness be controlled else issues may arise with solder voiding
5. Variations in thermal pad dimensions may exist between (device) part numbers. The exposed thermal pad sizes can be confirmed within the product data sheet.

2.7 Thermal Via Use in Array QFN Designs

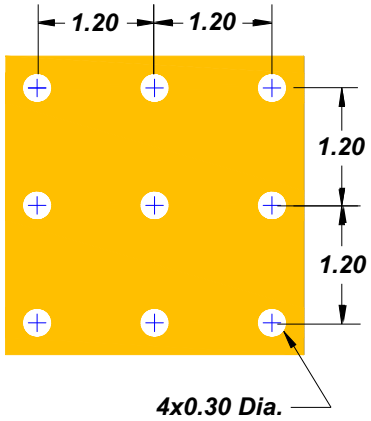


Figure 8. Example Via Layout Design Via layout – Designs will vary depending on layout constraints

In order to effectively transfer heat from the top metal layer of the PCB to the inner or bottom layers, thermal vias are recommended to be incorporated into the thermal pad design. The number of thermal vias will depend on the application, power dissipation, and electrical requirements. For temperature-critical applications via pitches down to 1mm can be used & vias may be filled or plugged.

Vias filled or plugged help prevent solder loss and protrusions. This often produces the best thermal performances but is not necessary or recommended due to increased PCB cost and because solder tends to wet the upper surface area prior to filling the vias.

Solder mask tenting is optional & if used top side is recommended to eliminate the risk of solder loss or protrusions thru via onto the opposite side of the PCB. Trials have shown that via tenting from the top is less likely to produce voids between the exposed pad and PCB pad when compared to via tenting from the bottom.

For this specific design TI is recommending a 0,3 mm diameter drill size to limit or control solder loss.

Thermal vias should interconnect to an internal ground plane.

2.8 Pad Surfaces

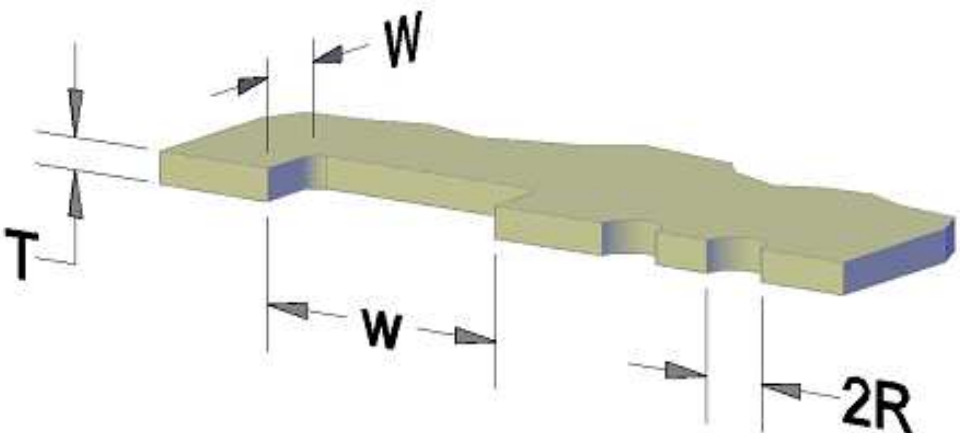
Solder pads must have good wettability to the soldering material (solder paste) selected for the application. Application should utilize a well proven pad finish for SMT assembly, and especially on fine pitch applications were quality of the plating finish increases in importance in relation to board overall reliability performance.

3 Solder Stencil

The function of the stencil is to deposit the correct amount of solder on the PCB and the volume of printed solder is determined by stencil openings, stencil thickness and actual amount of solder released. IPC7525 Is an industry guideline for stencil design and for this application stencil thickness can be between 100-125um thick with 125um preferred. Stencil design perimeters are determined by the exposed metal feature sizes and both aspect & area ratios to insure consistent solder release to PCB.

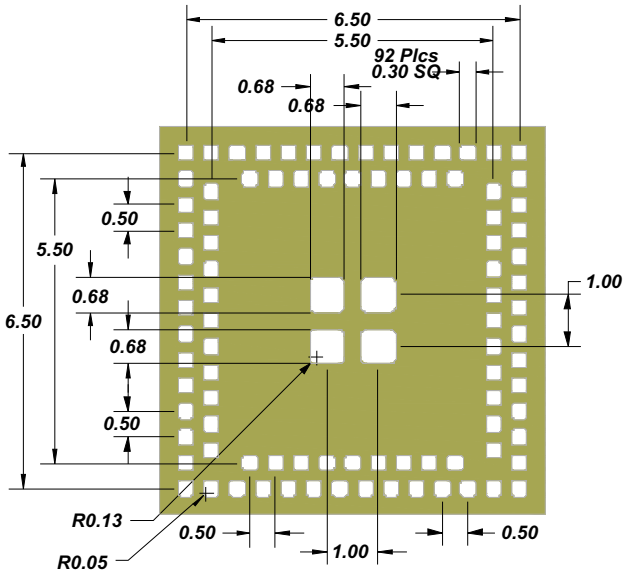
To ensure a uniform and high solder paste transfer to the PCB, laser cut (mostly made from stainless steel) or electroformed stencils (Nickel) should be preferred. Rounding the corners of the apertures (radius ~50 µm) combined with a Trapezoidal Aperture design (smaller at top) are supportive in ease of paste release by reducing the solders surface tension additionally 5% under to 8% over print have been used without issues.

3.1 Stencil Design – determining Aspect & Area Ratios



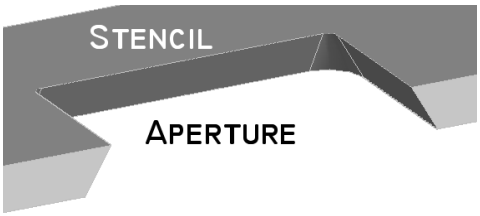
Basic concept: Aspect ratio (W/T, 2R/T) > 1.4, Area Ratio (W/4T, R/2T) > 66%.

3.1.1 Array QFN Stencil Design Recommendations:



Stencil Configuration Best Practices

- Stencil should include a trapezoidal type aperture where bottom opening is between 25 to 50 micron larger than the top to insure ease of solder release



- Laser cut electro-polished or electroformed stencil is preferred
- No sharp corners, all corners rounded
- Designed to match land pattern
- Stencil 100-125um thick
- Placement accuracy 50um
- Optimized aperture design to insure reliable solder release
- Goal is to achieve an optimum barrel solder joint at pins while avoiding or minimizing voids

3.2 Solder Paste

A “no clean” solder paste Type 4 (20 to 38 um particle size or finer), SAC305 type, is preferred for surface mounting the array QFN to the PCB this is due to its packages low standoff and stencils small pad openings. Solder is sensitive to age, temperature, humidity, and other environmental conditions, as well consistency in volume printed thus controls must be put in place for its use to insure product stability and reliability.

3.3 Component Placement

Array QFN packages can be placed using standard pick and place equipment. Component pick and place systems are composed of a vision system that recognizes and positions the component and a mechanical system which physically performs the pick and place operation. Two commonly used types of vision systems: (1) a vision system operates via package silhouette and (2) a vision system that locates individual features within the packages construction. Both methods are valid when used in placing the array QFN. Inherently machines used for finer pitch placement and optimize lighting have a higher resolution / accuracy and thus are recommended for array QFN mounting. Additionally component placement using either force ≤ 3N or by using component thickness +0.05mm have shown to work effectively without issue.

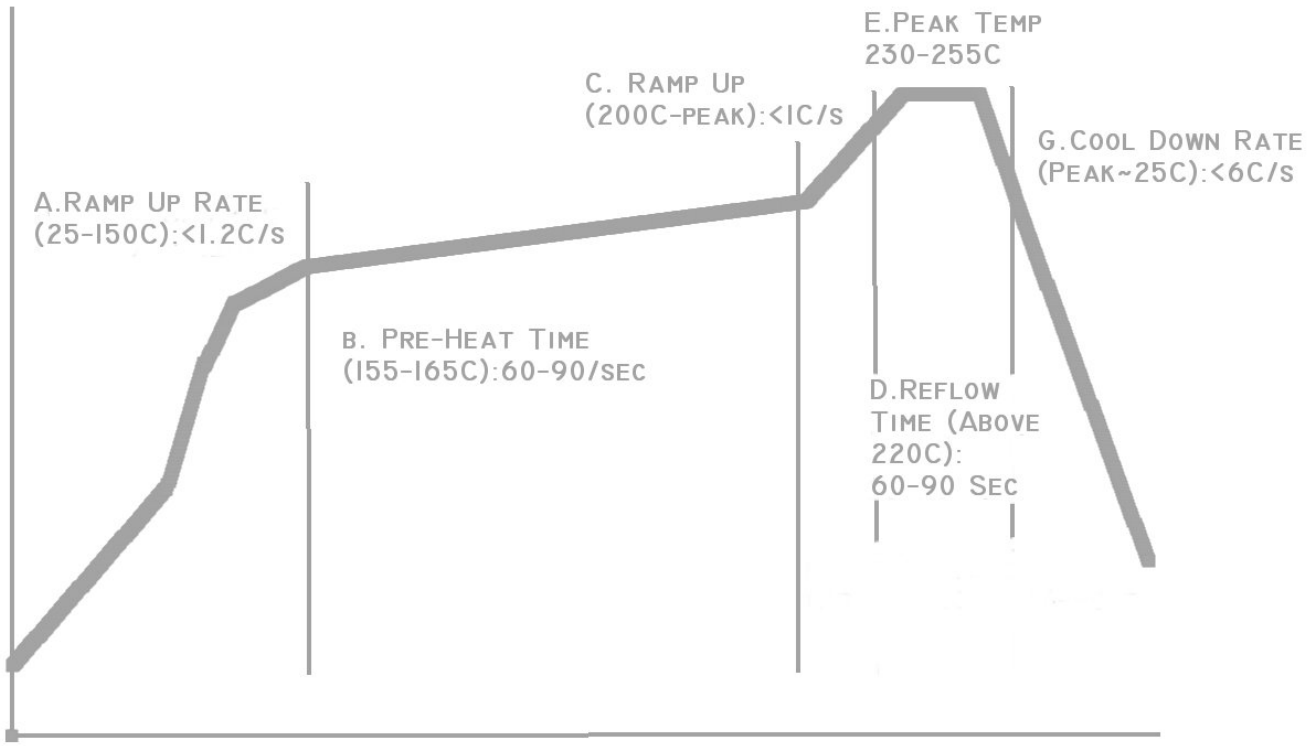
3.4 Reflow Profile

TI recommends following the solder paste supplier's recommendations to optimize flux activity and to achieve proper melting temperatures of the alloy within the guidelines of J-STD-20. TI prefers parts to be processed with the lowest peak temperature possible while also remaining below the components peak temperature rating as listed on the MSL label. The exact temperature profile would depend on several factors including maximum peak temperature for the component as rated on the MSL label, Board thickness, PCB material type, PCB geometries, component locations, sizes, densities within PCB, as well solder manufactures recommended profile, and capability of the reflow equipment to as confirmed by the SMT assembly operation. It is therefore recommended a localized temperature profile be captured using remote sensing for each array QFN application to insure correct reflow curve is applied.

3.4.1 Example Reflow Temperature Profile

Profile illustrated below is from a single side mounted 8 layer test board (see notes above)

	A	B	C	D	E	F
	Ramp Up 1(25~150C	Pre-Heat (155~165C)	Ramp Up (200C~Peak)	Reflow Time (Above 220C)	Peak Temperature	Cooling Down (Peak ~25C)
Spec.	<1.2C/Sec	60~90 Sec	<1 C/Sec	60~90 Sec	230~255C	<6C/Sec



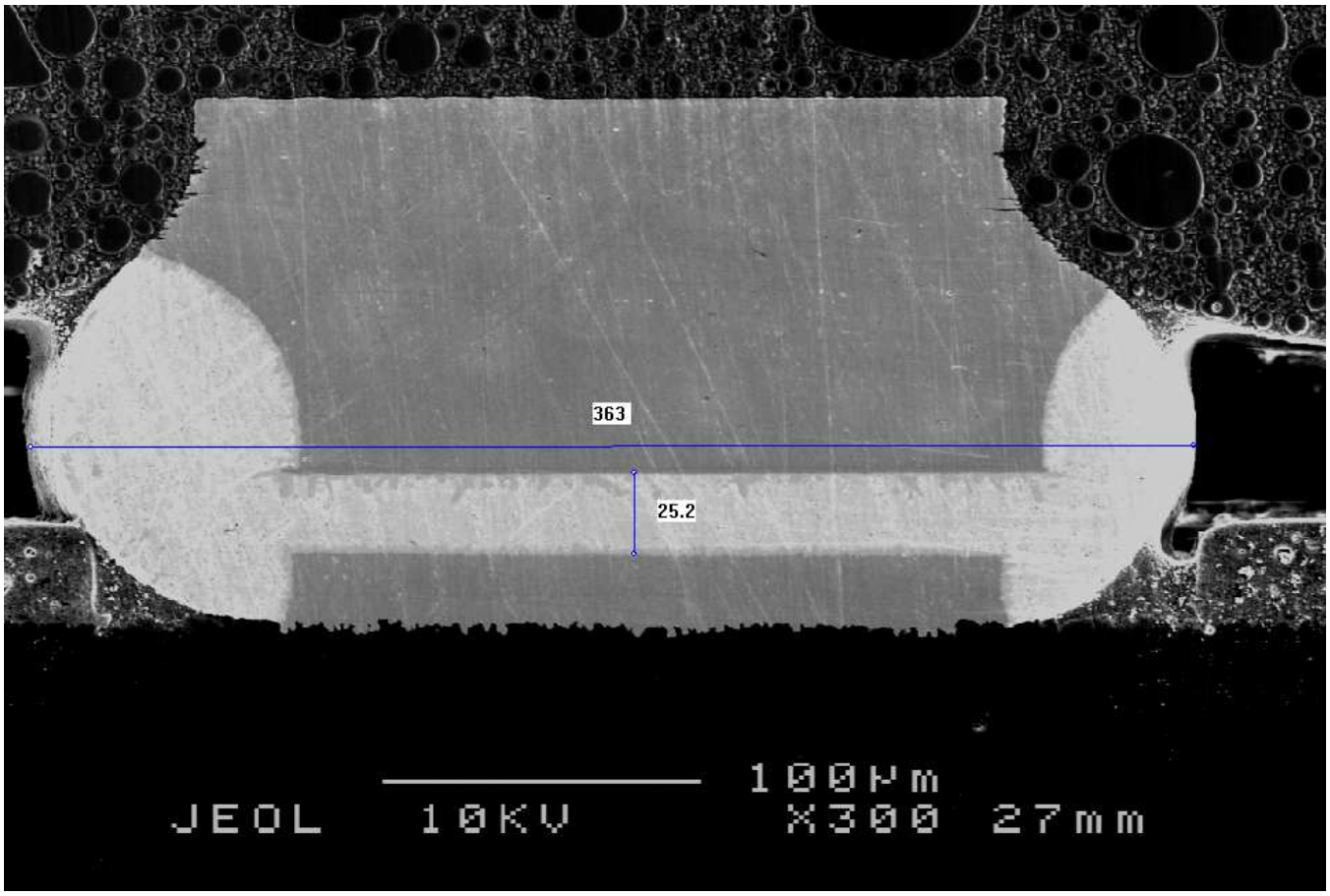
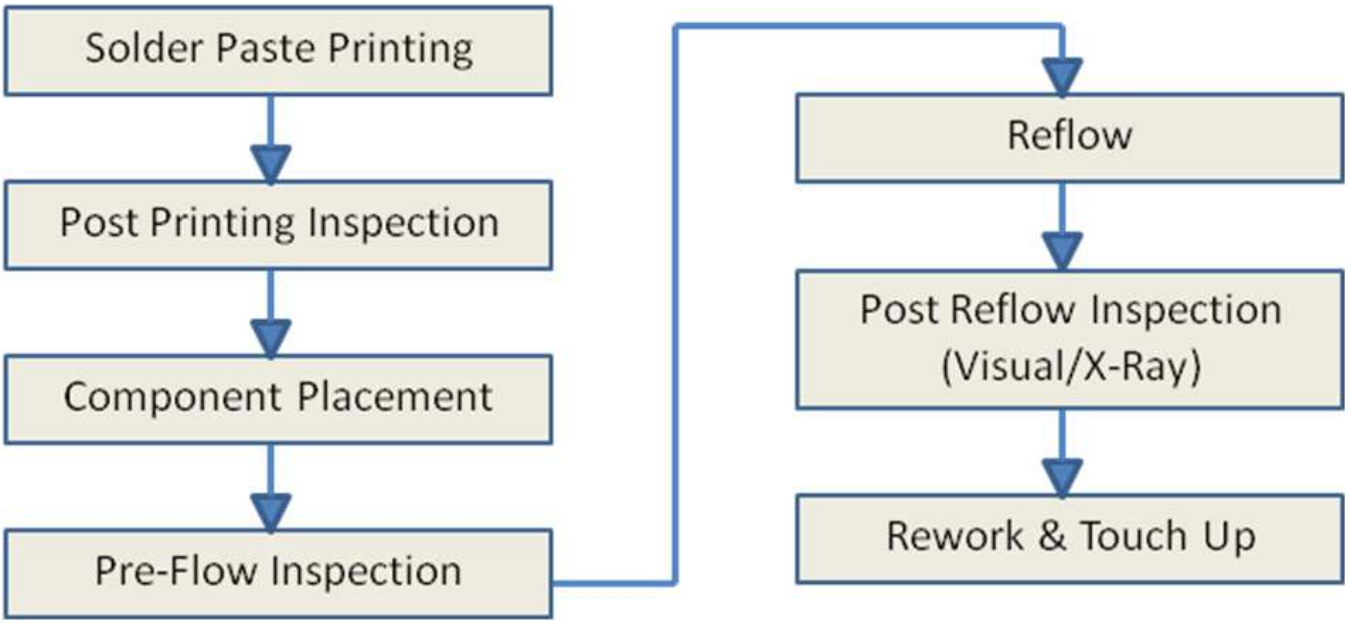


Figure 9. Example Cross Sectioned Solder Joint With (Good) Barrel Shape

4 Board Mount Assembly Flow

The standard bound mount assembly flow can be used for Array QFN without any problem. It very important to include the solder print inspection and post reflow inspection, especially during the process development. The solder paste volume should be around 90% of the stencil aperture volume for a good paste release. After reflow, the mounted package should be inspected using x-ray for voids, solder balling, solder bridge or other defects. Cross section may be required to determine the solder joint integrity.

A typical reflow profile for No Clean solder paste is shown in section 4.4.1 since the actual reflow profile depends on the solder paste being used coupled with the board density and equipment utilized, TI does not recommend a specific profile. The profile illustrated above is only to be used as reference; TI recommends customers contact their solder manufacturer for suggested temperature profile for their specific application.



7.0 Reference Document

7.1 IPC-T-50 Terms and Definitions

7.2 IPC-SM-7351A or -782 Land Pattern Design

7.3 IPC-A-610 Assembly Acceptability

7.4 IPC-7711 Rework of Electronic Assemblies

7.5 JEDEC-020D MSL

7.6 JEDEC-033 MSL

7.7 JEDEC-22-B102 Solderability

7.8 JEDEC-22-B104 TCT Test

7.9 JEDEC-22-B111 Drop Test

7.10 JEDEC-22-B113 Bending Test

7.11 EIA/JESD-2 & -7 Thermal Performance Test

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