Texas Instruments

TSW1001: ADS5500/5541/5542/ 5520/5521/5522 14- and 12-Bit Single-Channel ADC With LVDT1422 Output EVM

User's Guide

2006 High-Speed Data Converter Products

SLLU092

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 3.6 V and the output voltage range of 3.6 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 50°C. The EVM is designed to operate properly with certain components above 50°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Chapter 1

Overview

This user's guide document gives a general overview of the ADS55xx with LVDT1422 output evaluation module (EVM), and provides a general description of the features and functions to be considered while using this module.

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1.1 Purpose

The ADS55xx with LVDS output EVM provides a platform for evaluating the ADS55xx high-speed analog-to-digital converters (ADC) family under various signal, input, and supply conditions. This document should be used in combination with the EVM schematic diagram supplied.

1.2 EVM Basic Functions

Analog input to the ADC is provided via external SMA connectors. The single-ended input the user provides is converted into a differential signal at the input of the device. One input path uses a differential amplifier, while the other input is transformer-coupled.

The EVM provides external SMA connectors for input of the ADC clock. The single-ended input the user provides is converted into a differential signal at the input of the device. One input path uses a PECL differential driver, while the other input is transformer-coupled. The EVM also allows the user to send a single-ended or true-differential clock if desired.

Digital output from the EVM is via three LVDS output pairs driven by the LVDT1422, using SMA cabling.

Power connections to the EVM are via banana jack sockets. Separate sockets are provided for the ADC analog and buffer supplies, the external driver supply, and the differential amplifier supply.

1.3 Power Requirements

The EVM can be powered directly with only a single 3.3-V supply if using the module with transformer-coupled input and internal reference mode. If using the differential amplifier input, ±5 V is required. Provision has also been made to allow the EVM to be powered with independent supplies to provide higher performance.

Voltage Limits

Exceeding the maximum input voltages can damage EVM components. Undervoltage may cause improper operation of some or all of the EVM components.

The ADS55xx EVM provides a platform for evaluating the analog-to-digital (ADC) devices shown in Table 1−1.

Table 1−1. Device List

DEVICE	RESOLUTION	SAMPLE RATE (1)
ADS5500	14-bit resolution	125 MSPS
ADS5541	14-bit resolution	105 MSPS
ADS5542	14-bit resolution	80 MSPS
ADS5520	12-bit resolution	125 MSPS
ADS5521	12-bit resolution	105 MSPS
ADS5522	12-bit resolution	80 MSPS

1) The maximum clock rate of the LVDT1422 driver is 100 MHz.

The EVM allows the user to evaluate an ADS55xx ADC under various input signal and supply conditions. This document should be used in combination with the device data sheet when evaluating a device.

1.4 ADS55xx EVM Operational Procedure

The ADS55xx EVM provides a flexible means of evaluating the ADS55xx in a number of modes of operation. A basic setup procedure that can be used as a board confidence check is as follows:

1) Verify all jumper settings against the schematic jumper list in the following tables:

Table 1−2. Two-Pin Jumper List

JUMPER	FUNCTION	INSTALLED	REMOVED	DEFAULT
W3	Access point for providing SCLK for programming ADC internal registers	Connects pin 2 to GND	Removes pin 2 from GND	Installed
W6	Access point for providing SDATA for programming ADC internal registers	Connects pin 3 to GND	Removes pin 3 from GND	Installed
W7	Access point for providing SEN for programming ADC internal registers	Connects pin 4 to GND	Removes pin 4 from GND	Installed
W8	LVDT1422 falling edge select	Connects LVDT1422 pin 37 to GND	Removes LVDS pin from GND	
W9	LVDT1422 disable	Connects LVDT1422 pin 48 to GND	Removes LVDS pin from GND	

Table 1−3. Three-Pin Jumper List

JUMPER	FUNCTION	LOCATION: PINS 1− 2	LOCATION: PINS 2−3	DEFAULT
SJP1	Common-mode voltage from ADC	Provides common-mode voltage to differential amplifier	Provides common-mode voltage to transformer T2	2−3
SJP2	ECL driver-input power select	Provides 5 VDC	Provides 3.3 VDC	1−2
W2	ADC output enable control	ADC output enabled	ADC output disabled	1−2
SJP6	Reset polarity select	Used with active-low ADC reset	Used with active-high ADC reset	2−3

Table 1−4. Five-Pin Jumper List

JUMPER	FUNCTION	LOCATION	DATA FORMAT	OUTPUT CLOCK POLARITY	DEFAULT
W5	ADC data format and output clock polarity select	Pins 4−5 Pins 3−5 Pins 2−5 Pins 1−5	Straight binary 2s compliment Straight binary 2s compliment	Data valid on rising edge Data valid on rising edge Data valid on falling edge Data valid on falling edge	Pins 4−5

2) Connect supplies to the EVM as follows:

   3.3-V ADC output buffer supply to J17 and return to J18.

   3.3-V ADC analog supply to J11 and return to J10.

3) Switch power supplies on.

4) Use a function generator with 50-Ω output to input an 80-MHz–125-MHz, 0-V offset, 1-Vrms sine-wave signal into J3. The frequency of the clock must be within the specification for the device speed grade.

5) Use a frequency generator with a 50-Ω output to provide a 10-MHz, 0-V offset, −1-dBFS-amplitude sine-wave signal into J7. This provides a transformer-coupled differential input signal to the ADC.

6) The digital pattern on the output connector J8 should now represent a sine wave and can be monitored using a logic analyzer.

Chapter 2

Circuit Description

This chapter describes the circuit functions of the ADS55xx with LVDT1422 output EVM.

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2.1 Schematic Diagram

The schematic diagram for the EVM is attached to the end of this document.

2.2 Circuit Function

The following paragraphs describe the functions of individual circuits. See the appropriate data sheet for device operating characteristics.

2.2.1 Analog Inputs

The EVM can be configured to provide the ADC with either transformer-coupled or differential amplifier inputs from a single-ended source. The inputs are provided via SMA connectors J7 for transformer-coupled input, and J1 and J2 for differential amplifier input. To set up for one of these options, the EVM must be configured as follows:

1) For a 1:1 transformer-coupled input to the ADC, a single-ended source is connected to J7. R22 and R35 must be removed and R41 and R45 must be installed. SJP1 must have pins 2 and 3 shorted. This is the default configuration for the EVM.

2) For a single-ended input into the differential amplifier, a single-ended source is connected to J1. R22 and R35 must be installed, and R41 and R45 must be removed. SJP1 must have pins 1 and 2 shorted. C12, C32, C35, and R40 provide the user with the option to add filters if desired.

3) For a differential input into the amplifier, the positive source is connected to J1 and the negative source to J2. R22 and R35 must be installed, and R41 and R45 removed. SJP1 must have pins 1 and 2 shorted. R8 must be replaced with a 54.9-Ω resistor and R19 with a 383-Ω resistor for proper amplifier termination.

2.2.2 Clock Inputs

The EVM provides three methods for inputs for the ADC clock pins. The initial configuration of the EVM provides a transformer coupled clock to the converter.

2.2.2.1 Transformer-Coupled Differential ADC Clock

To provide a transformer-coupled differential clock using a single-ended input source, C25 and C40 must be installed, and R11, R25, R32, C36, C39, and C49 must be removed. R31 is 0 Ω for proper transformer configuration. This is the default configuration for the EVM.

2.2.2.2 True Differential ADC Clock

To provide a true-differential ADC clock input, install J4, R11, R25, C25, and C40, replace R31 with a 49.9-Ω resistor, and remove R32, C36, C39, C49, and T3. The positive source should be connected to J3 and the negative source to J4.

2.2.2.3 ECL Differential ADC Clock

To provide an ECL differential clock input, install C36, C39, and C49 and remove C25 and C40. Configure SJP2 to provide either AVDD or +VCC supply to the ECL differential driver supply pin.

2.2.3 Control Inputs

The EVM has three discrete inputs and a 3-pin serial bus to control the operation of the device:

2.2.3.1 Output Enable

With jumper W2 installed between pins 1 and 2, the ADC outputs are enabled. The device outputs are disabled with jumper W2 installed between pins 2 and 3.

2.2.3.2 DFS Control

By adjusting the voltage on the data format and clock polarity select (DFS) pin, the user can set the mode of operation of the device. Test point 10 should be used to monitor this level. Once the appropriate voltage is reached, the ADC automatically sets the corresponding data format and clock polarity setting. Jumper W5 selects the voltage used for this pin. See Table 1−3 for the data format and clock polarity settings determined by the position of the jumper on W5.

2.2.3.3 IREF Control

By adjusting the resistance on pin 31 (IREF), the user can adjust the bias current used by the ADS55xx device. The default value for the EVM is 56.2 kΩ. Care must be taken when changing this value. See the appropriate data sheet for more information.

2.2.4 Power

Power is supplied to the EVM via banana jack sockets. A separate connection is provided for a 3.3-V analog supply (J11 and J10), 3.3-V buffer supply (J17 and J18), ±5-V amplifier supply (J14, J13, and J12), and 3.3-V external buffer supply (J19 and J20).

2.2.5 Outputs

The data outputs from the ADC are serialized onto three LVDS pairs via an LVDS1422 transceiver. The LVDT1422 outputs the 14-bit data serialized 7:1 onto two LVDS data lines labeled TAP, TAN and TBP, TBN, and the clock is sent out on the third LVDS output, labeled TCLKP, TCLKN. These outputs use SMA coaxial connectors. Figure 2−1 illustrates the ordering of the serialized data.

The parallel data outputs from the ADC are also routed to connector J8. This connector is a standard 40-pin header on a 100-mil grid, and allows easy connection to a logic analyzer. The connector pinout is listed in Table 2−1.

Figure 2−1. LVDS Data Bit Ordering

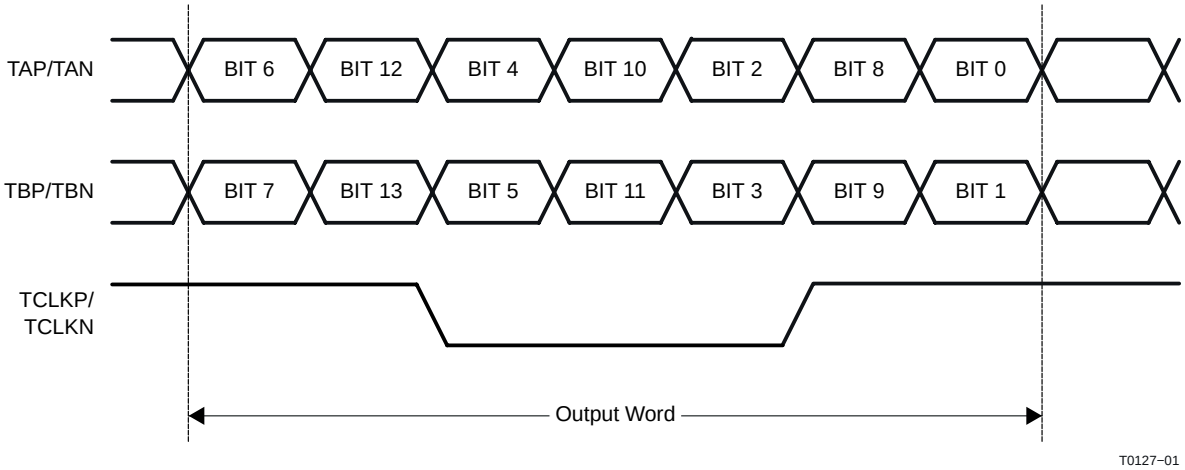

Table 2−1. Output Connector J8

J8 PIN	DESCRIPTION	J8 PIN	DESCRIPTION
1	DGND	21	DGND
2	Output Clock	22	Data Bit 6
3	DGND	23	DGND
4	NC	24	Data Bit 7
5	DGND	25	DGND
6	NC	26	Data Bit 8
7	DGND	27	DGND
8	NC	28	Data Bit 9
9	DGND	29	DGND
10	Data Bit 0 (LSB)	30	Data Bit 10
11	DGND	31	DGND
12	Data Bit 1	32	Data Bit 11
13	DGND	33	DGND
14	Data Bit 2	34	Data Bit 12
15	DGND	35	DGND
16	Data Bit 3	36	Data Bit 13 (MSB)
17	DGND	37	DGND
18	Data Bit 4	38	Overflow
19	DGND	39	DGND
20	Data Bit 5	40	NC

Chapter 3

Physical Description

This chapter describes the physical characteristics and PCB layout of the EVM and lists the components used on the module.

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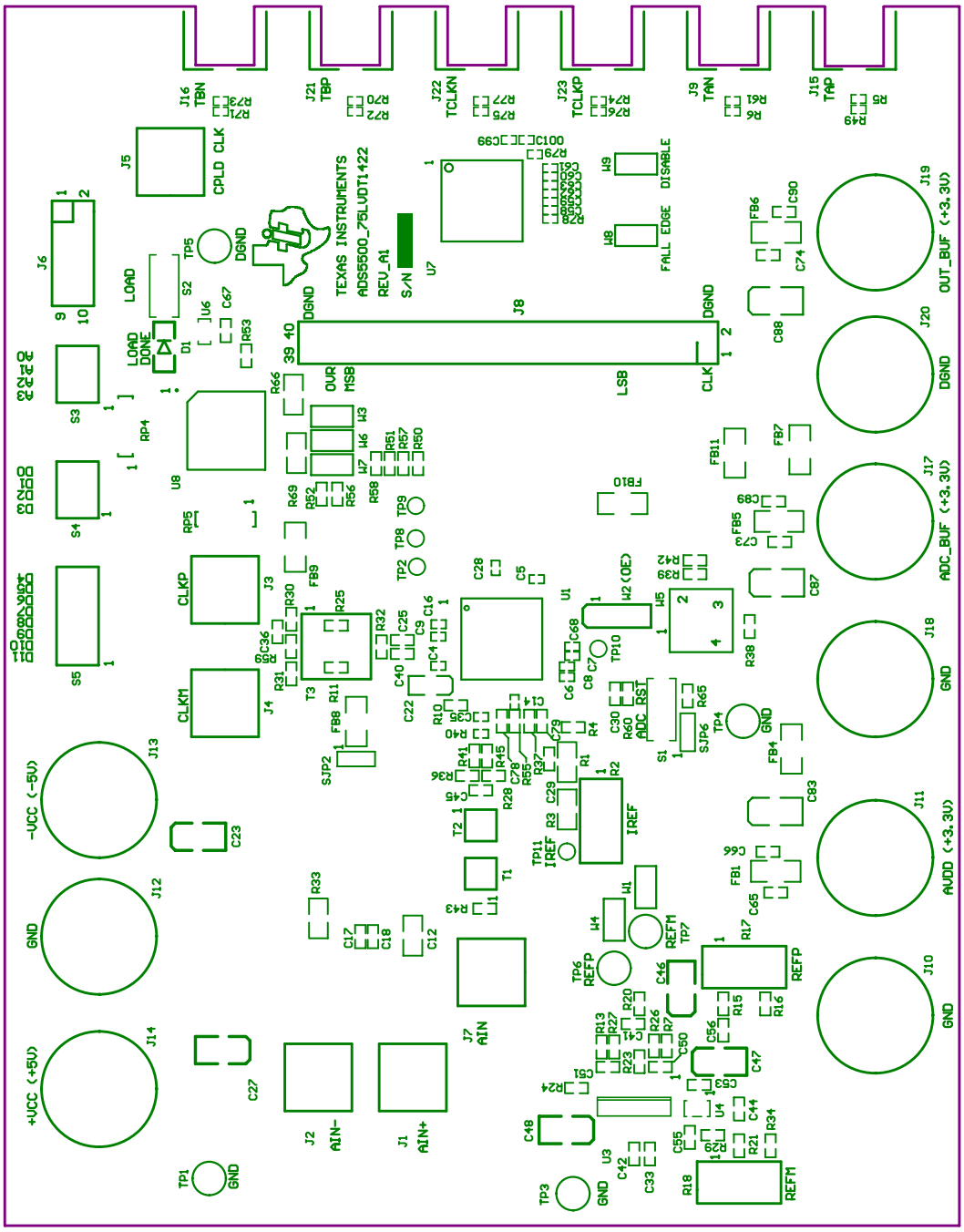
3.1 PCB Layout

The EVM is constructed on a 6-layer, 4.5-inch x 4.15-inch, 0.062-inch thick PCB using FR-4 material. The individual layers are shown in the following figures.

Figure 3−1. Top Silkscreen



K001

Figure 3−2. Top Layer

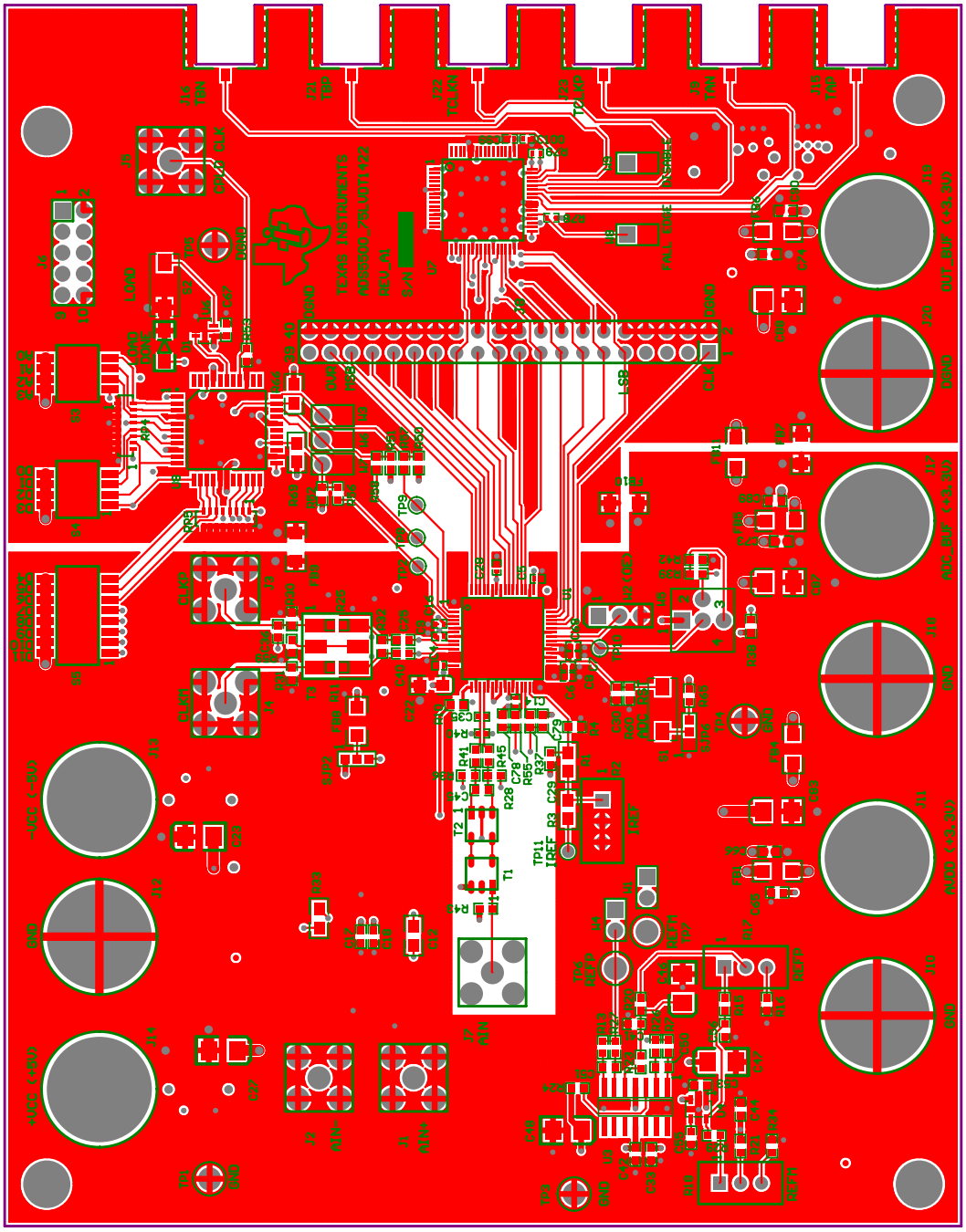


Figure 3−3. Top Layer (NH)

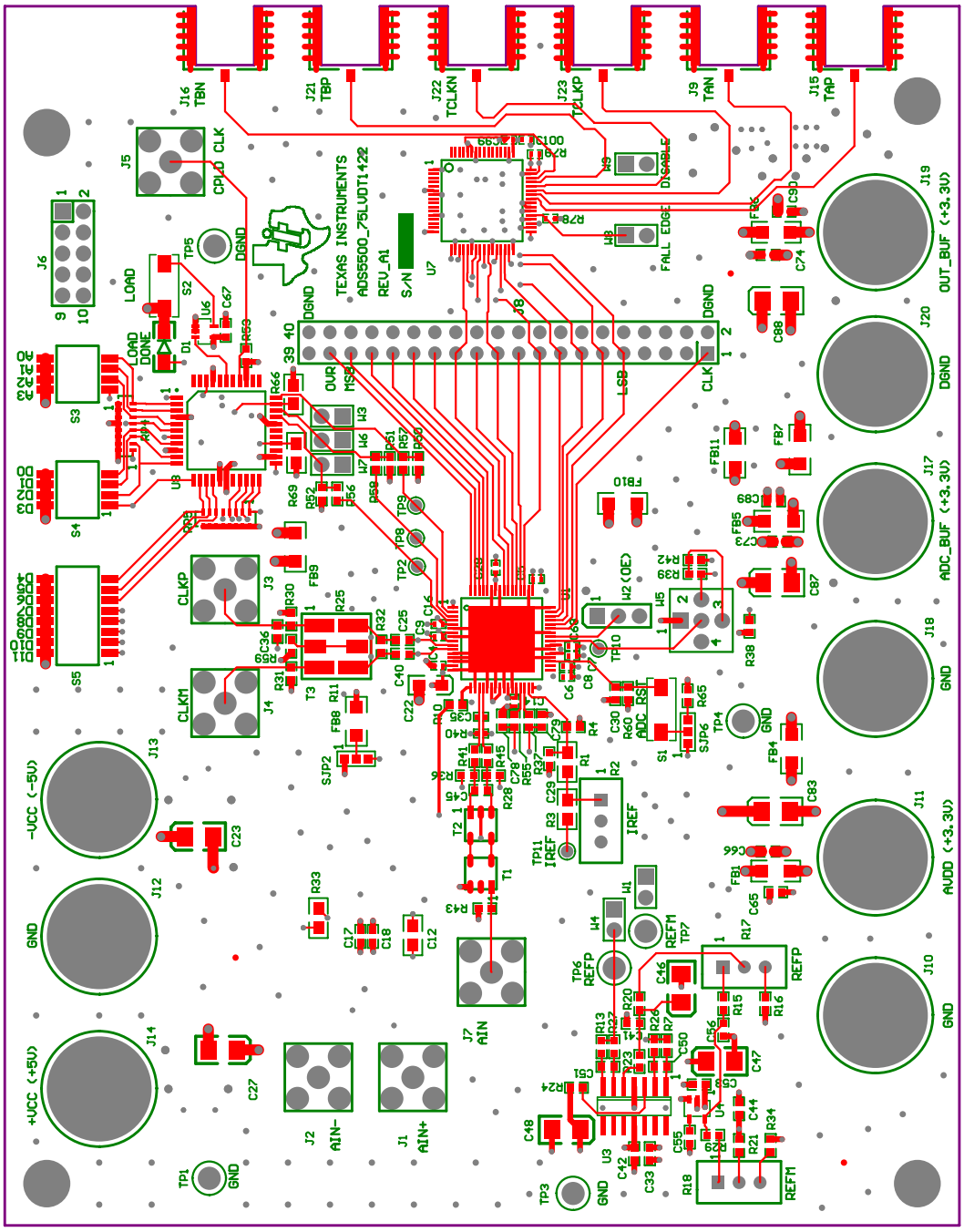


Figure 3−4. Internal Plane 1, Ground Plane

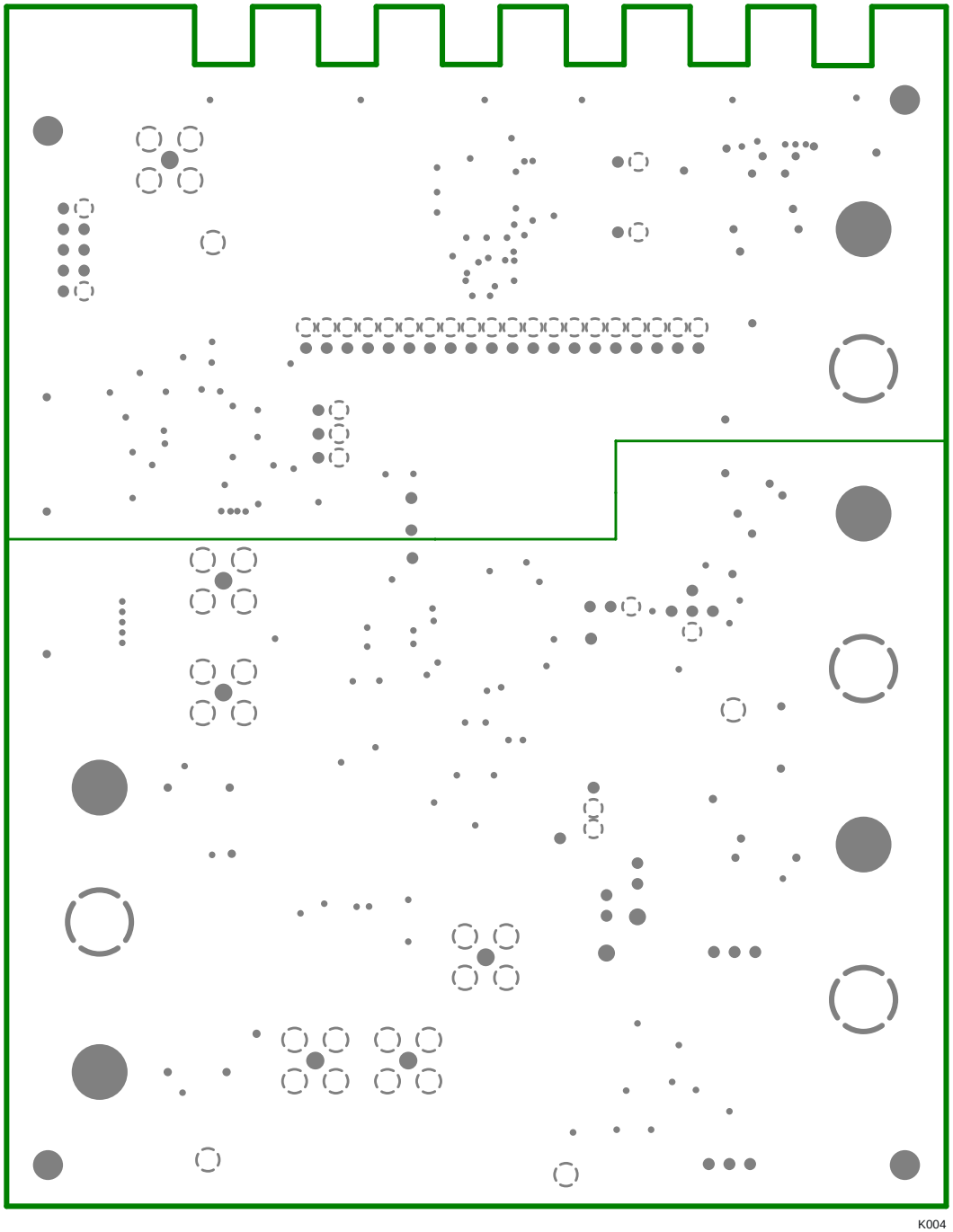


Figure 3−5. Internal Plane 2, Split Power Plane #1

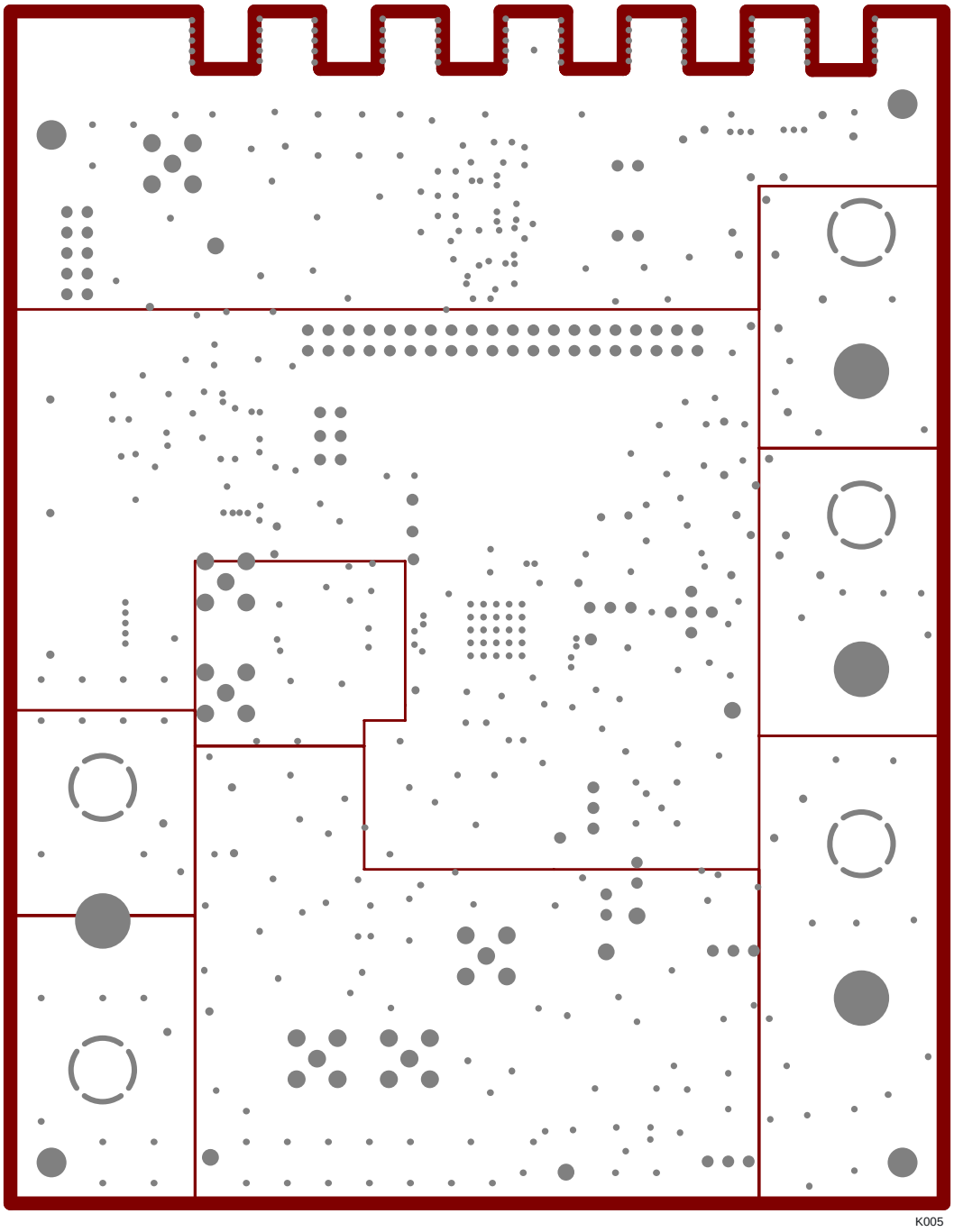


Figure 3−6. Intenal Plane 3, Split Power Plane #2

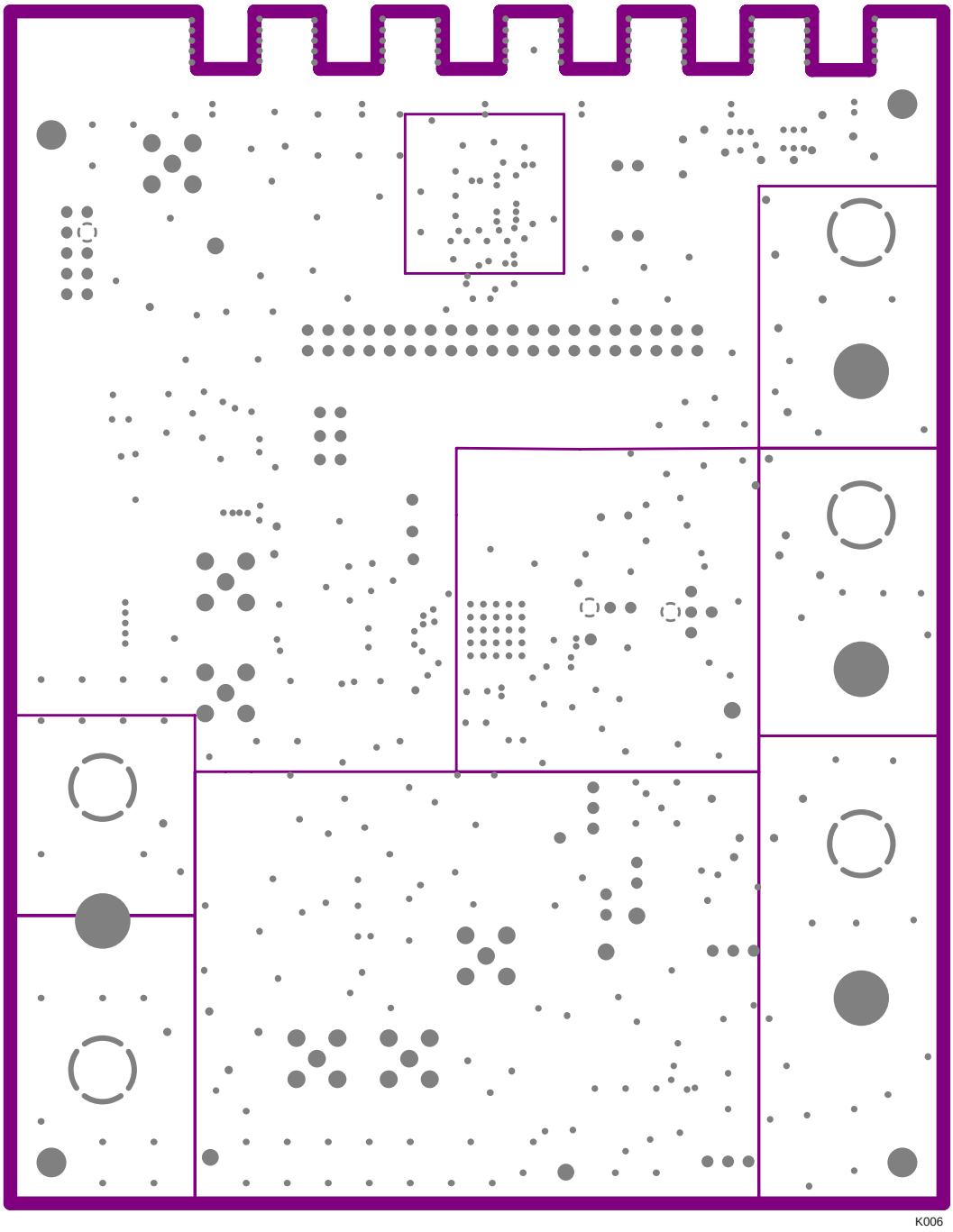


Figure 3−7. Internal Plane 4, Ground Plane

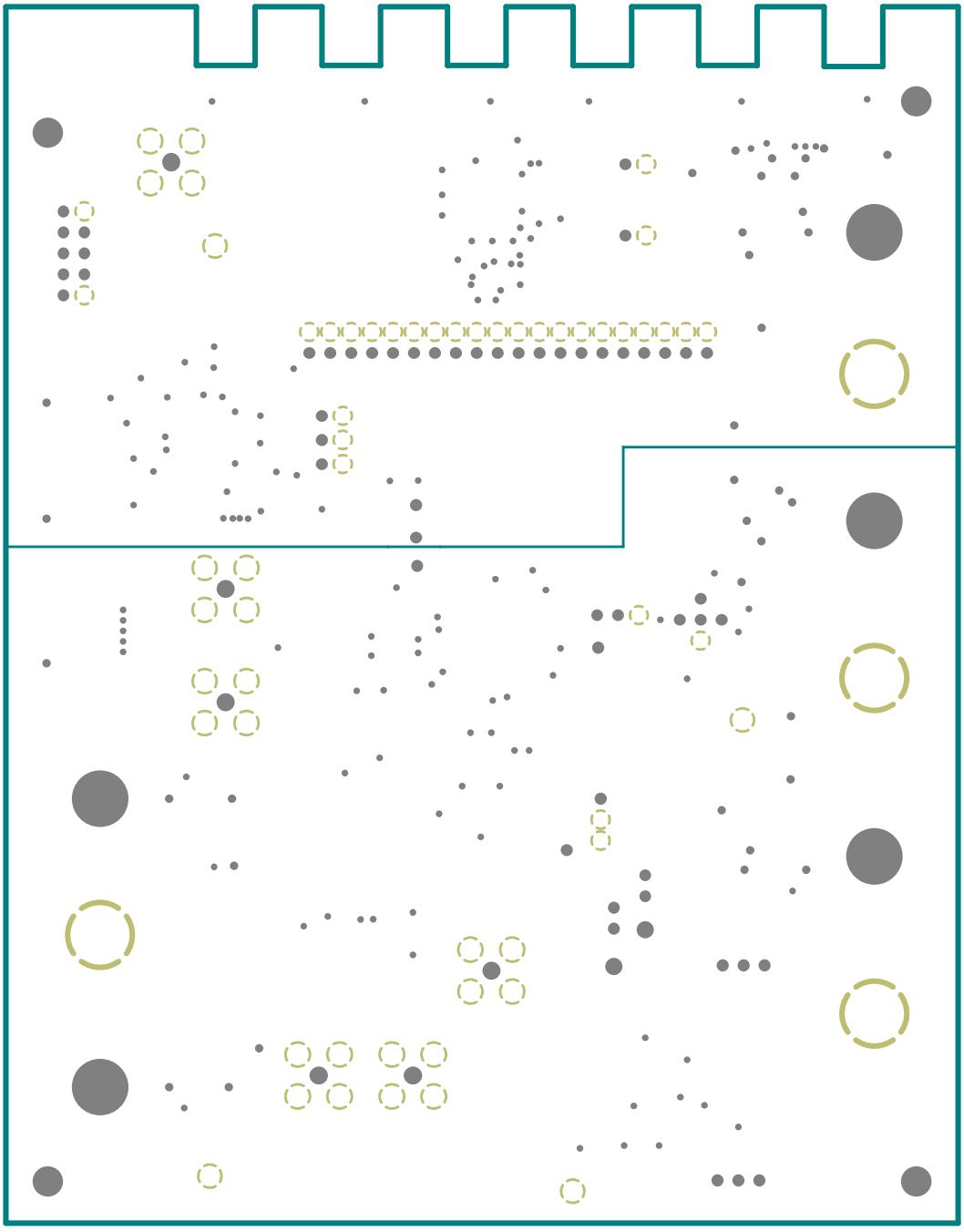


Figure 3−8. Bottom Layer

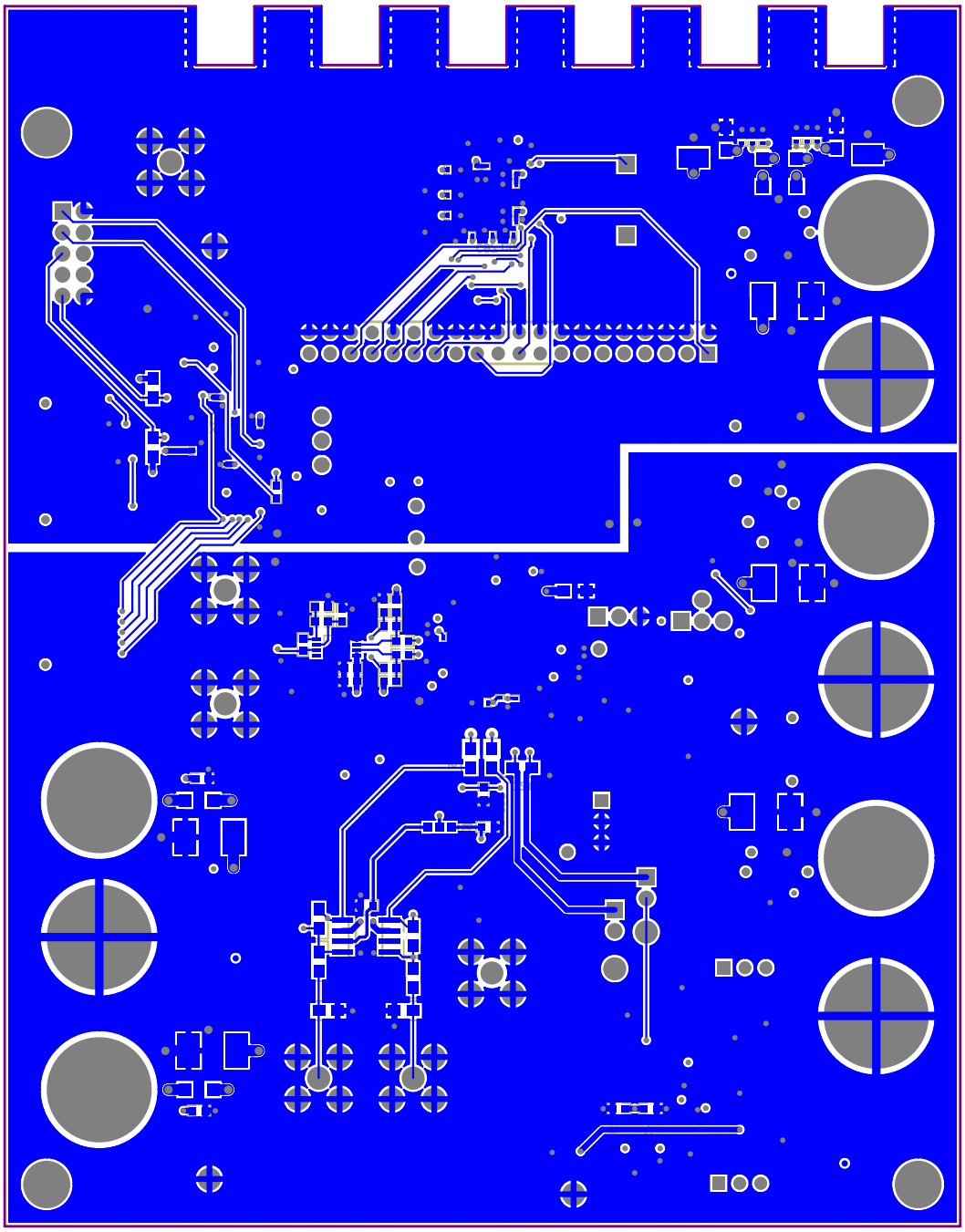


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Figure 3−9. Bottom Layer (NH)

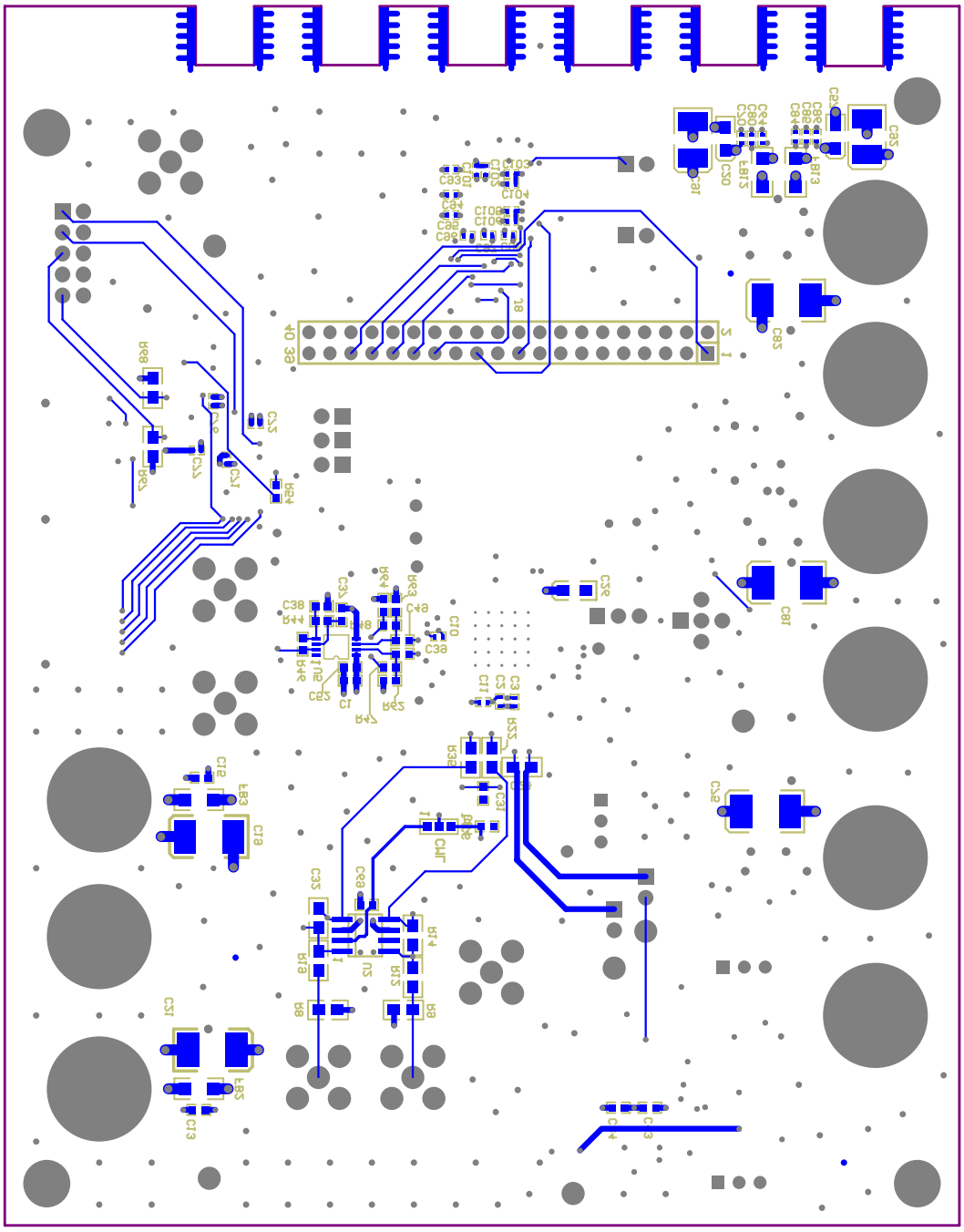

Figure 3−10. Bottom Silkscreen

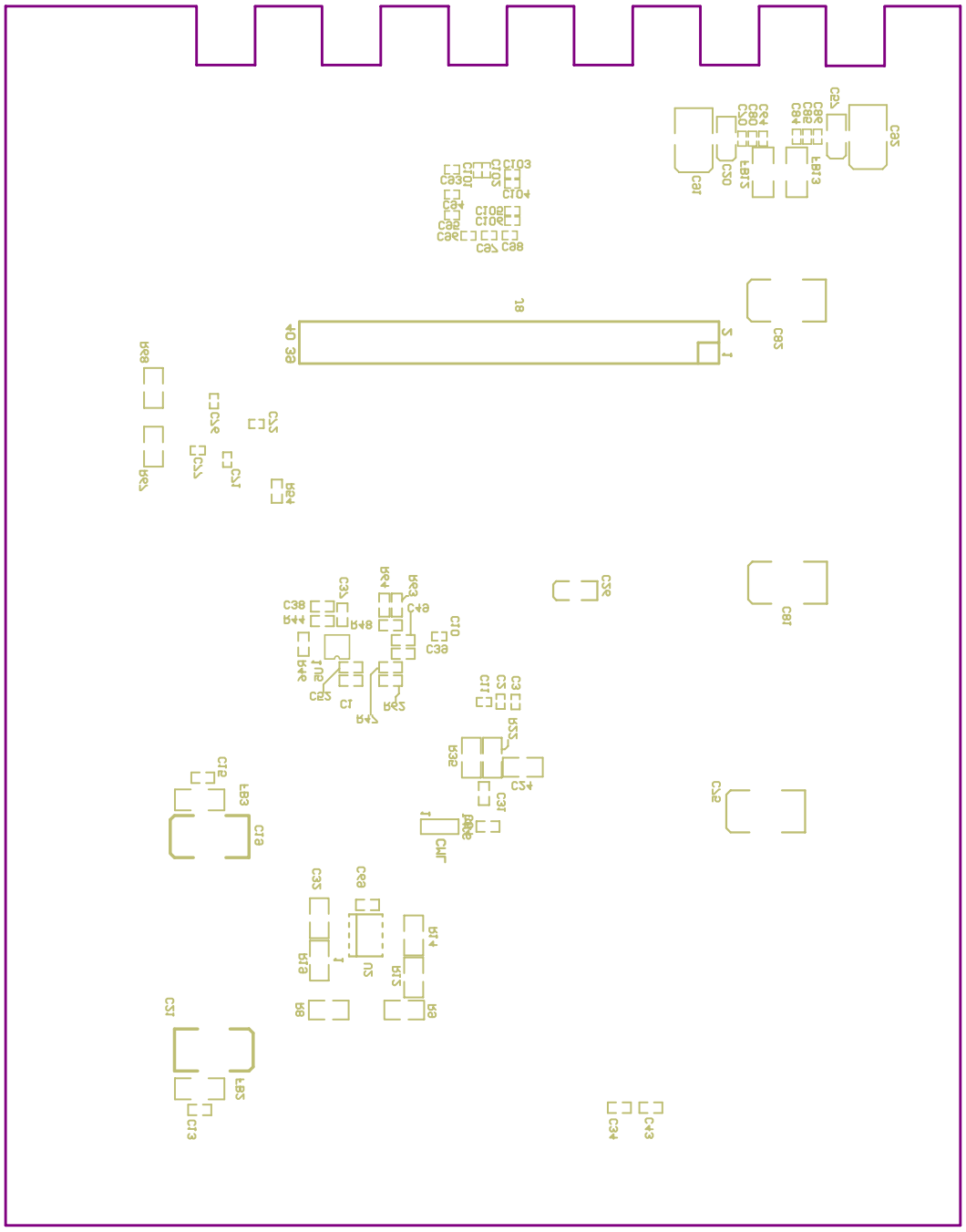

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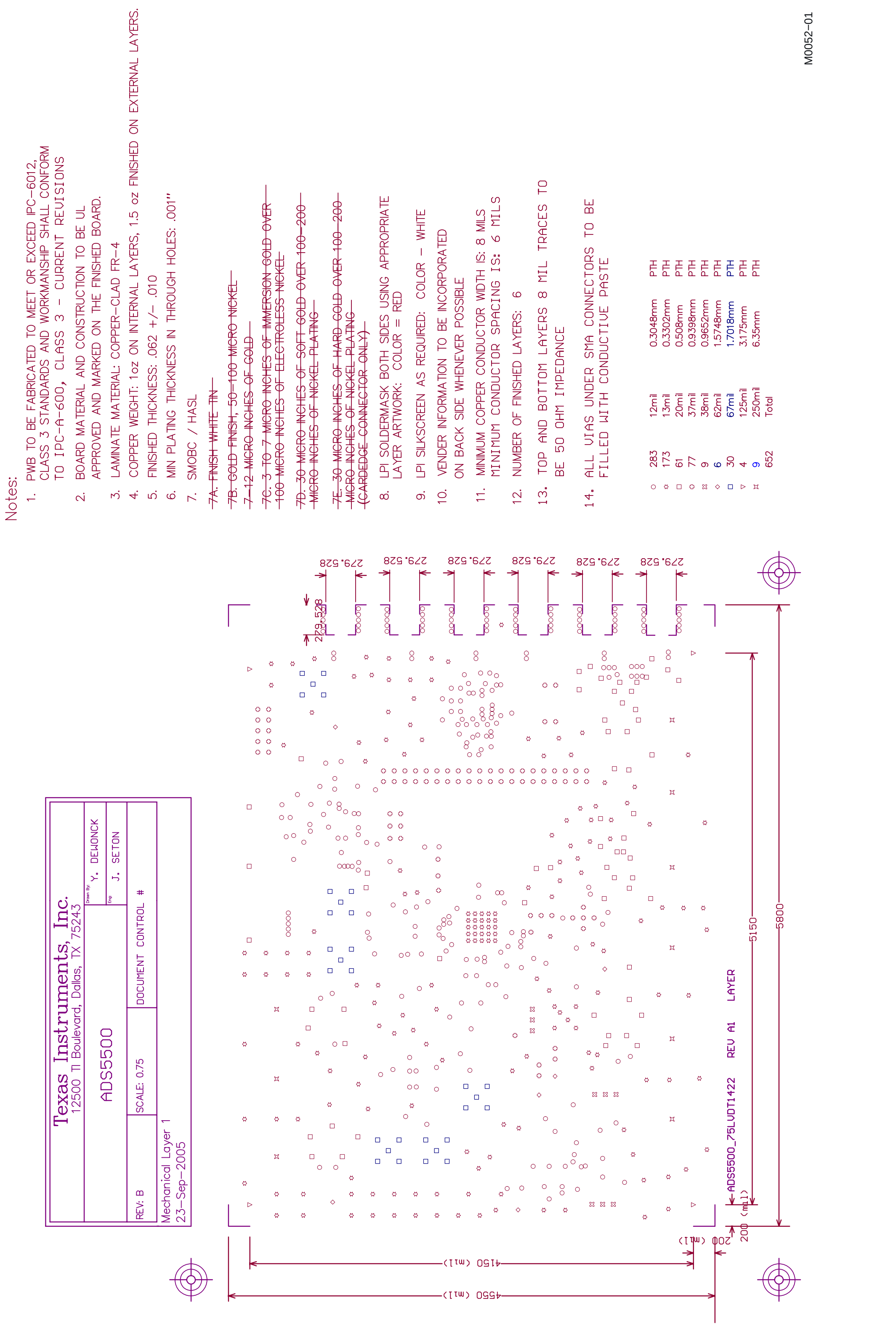
Figure 3−11. Drill Drawing



3.2 Parts List

The following pages contain the bill of materials.

Table 3−1. Bill Of Materials For ADS5500_75LVDT1422

Value	Footprint	Qty	Part Number	Vendor	Digi-Key Number	REF DES	Not Installed
CAPACITORS							
47-µF, 10-V, 20%, tantalum	7343	5	ECS-T1AD476R	Panasonic	PCS2476CT-ND	C19, C21, C75, C81, C82	
10-µF, 10-V, 20%	3528	5	ECS-T1AX106R	Panasonic	PCS2106CT-ND	C23, C27, C83, C87, C88	C46, C47, C48
10-µF, 10-V, 10%	3216	4	T491A106K010AS	KEMET	399-1563-1-ND	C20, C22, C26, C57	
220-µF, 6.3-V, 10%	6032	2	TAJC227K006R	AVX	478-1713-1-ND	C91, C92	
0.1-µF,16V, 10%	805	0	ECJ-2VB1C104K	Panasonic	PCC1812CT-ND		C24
6.8-pF, 50-V, ±0.25-pF	805	0	08055A6R8CAT2A	AVX	478-1302-1-ND		C12, C23
470-pF,100-V, 10%	603	0	ECJ-1VB2A471K	Panasonic	PCC1950CT-ND		C33, C34
0.047-µF,16-V, 10%	603	0	ECJ-1VB1H473K	Panasonic	PCC2286CT-ND		C50, C51
10-pF, 50V, ±0.5-pF	603	0	ECJ-1VC1H100D	Panasonic	PCC100CVCT-ND		C45
0.01-µF, 50-V,10%	603	4	ECJ-1VB1C103K	Panasonic	PCC1750CT-ND	C31, C52, C54, C69	C55
0.1-µF,16-V, 10%	603	15	ECJ-1VB1C104K	Panasonic	PCC1762CT-ND	C1, C13, C15, C17, C18, C25, C37, C38, C40, C65, C66, C73, C74, C89, C90	C29, C30, C36, C39, C41, C42, C43, C44, C49, C67
1-µF, 6.3-V,10%	603	1	ECJ-1VB0J105K	Panasonic	PCC1915CT-ND	C78	C53, C79
2.2-µF, 6.3-V, +80%/−20%	603	0	ECJ-1VF0J225Z	Panasonic	PCC2181CT-ND		C56
0.01-µF,16-V, +80%/−20%	402	14	ECJ-0EF1C103Z	Panasonic	PCC1747CT-ND	C93–C106	

Value	Footprint	Qty	Part Number	Vendor	Digi-Key Number	REF DES	Not Installed
0.1-µF,16-V ±80%/−20%	402	20	ECJ-0EF1C104Z	Panasonic	PCC1731CT-ND	C2−C11, C14, C16, C28, C64, C68, C70, C80, C84, C85, C86	C71, C72, C76, C77
27-pF, 50-V, 5%	402	0	ECU-E1H270JCQ	Panasonic	PCC270CQCT-ND		C35
RESISTORS							
0-Ω, 1/16 W, 1%	805	1	ERJ-6ENF0R00V	Panasonic	P0.0CCT-ND	R8	
54.9-Ω, 1/16 W, 1 %	805	1	ERJ-6ENF54R9V	Panasonic	P54.9CCT-ND	R9	
383-Ω, 1/16 W, 1%	805	1	ERJ-6ENF3830V	Panasonic	P383CCT-ND	R12	
392-Ω, 1/16 W, 1%	805	2	ERJ-6ENF3920V	Panasonic	P392CCT-ND	R14, R33	
402-Ω, 1/16 W, 1%	805	0	ERJ-6ENF4020V	Panasonic	P402CCT-ND		R22, R35
412-Ω, 1/16 W, 1%	805	1	ERJ-6ENF4120V	Panasonic	P412CCT-ND	R19	
1-kΩ, 1/16 W, 1%	805	0	ERJ-6ENF1001V	Panasonic	P1.0KCCT-ND		R66, R67, R68, R69
10-kΩ, 1/16 W, 1%	805	0	ERJ-6ENF1002V	Panasonic	P10.0KCCT-ND		R3
20-kΩ, 1/16 W, 1%	805	0	ERJ-6ENF2002V	Panasonic	P20.0KCCT-ND		R1
0-Ω, 1/16 W, 1%	603	5		Panasonic	P0.0CCT-ND	R31, R56, R57, R58, R59	R11, R25
1-Ω, 1/16 W, 5%	603	2	9C0603A1 JLHFT	Panasonic	311-1 GTR-ND	R37, R55	
100-Ω, 1/16 W, 1%	603	0	ERJ-3EKF1000V	Panasonic	P100HCT-ND		R23, R24
113-Ω, 1/16 W, 1%	603	1	ERJ-3EKF1130V	Panasonic	P113HCT-ND	R64	
24.9-Ω, 1/16 W, 1%	603	2	ERJ-3EKF24R9V	Panasonic	P24.9HCT-ND	R41, R45	
36.5-Ω, 1/16 W, 1%	603	2	ERJ-3EKF36R5V	Panasonic	P36.5HCT-ND	R28, R36	
49.9-Ω, 1/16 W, 1%	603	4	ERJ-3EKF49R9V	Panasonic	P49.9HCT-ND	R10, R30, R47 R48	R7, R13, R43, R53, R62, R63
82.5-Ω, 1/16 W, 1%	603	0	ERJ-3EKF82R5V	Panasonic	P82.5HCT-ND		R54

Value	Footprint	Qty	Part Number	Vendor	Digi-Key Number	REF DES	Not Installed
200-Ω, 1/16 W, 1%	603	0	ERJ-3EKF200V	Panasonic	P200HCT-ND		R32
499-Ω, 1/16 W, 1%	603	2	ERJ-3EKF499V	Panasonic	P499HCT-ND	R44, R46	R15
1-kΩ, 1/16 W, 1%	603	3	ERJ-3EKF1001V	Panasonic	P1.00KHCT-ND	R38, R39, R42	
2-kΩ, 1/16 W, 1%	603	0	ERJ-3EKF2001V	Panasonic	P2.00KHCT-ND		R26, R27
2.55-kΩ, 1/16 W, 1%	603	0	ERJ-3EKF2551V	Panasonic	P2.55KHCT-ND		R34
2.87-kΩ, 1/16 W, 1%	603	0	ERJ-3EKF2871V	Panasonic	P2.87KHCT-ND		R29
4.75-kΩ, 1/16 W, 1%	603	1	ERJ-3EKF4751V	Panasonic	P4.75KHCT-ND	R65	
5.62-kΩ, 1/16 W, 1%	603	0	ERJ-3EKF5621V	Panasonic	P5.62KHCT-ND		R16
49.9-kΩ, 1/16 W, 1%	603	3	ERJ-3EKF4992V	Panasonic	P49.9KHCT-ND	R50, R51, R52	
56.2-kΩ, 1/16 W, 1%	603	1	ERJ-3EKF5622V	Panasonic	P56.2KHCT-ND	R4	
10-kΩ, 1/16 W, 1%	603	1	ERJ-3EKF1002V	Panasonic	P10.0KHCT-ND	R60	R20, R21
174-Ω, 1/16 W, 1 %	402	0	ERJ-2RFK1740X	Panasonic	P174LCT-ND		R40
10-kΩ, 1/16 W, 1%	402	2	ERJ-2RKF1002X	Panasonic	P10.0KLCT-ND	R78, R79	
1-kΩ variable	POT_RES_TH	0	CT94W102	CERMET	CT94W102-ND		R17, R18
100-kΩ variable	POT_RES_TH	0	CT94W104	CERMET	CT94W104-ND		R2
100-kΩ R-pack	CTS-742-4RES	0	742C163100KJCT	CTS	742C163100KJCT-ND		RP4, RP5
CONNECTORS, JUMPERS, HEADERS, FERRITE BEADS, TRANSFORMERS, ICS							
Ferrite bead	1206	9	EXC-ML32A680U		P10437CT-ND	FB1, FB2, FB3, FB5, FB6, FB8, FB10, FB12, FB13	FB4, FB7, FB9, FB11
Transformer	TC4-1W_TRANSFORMER	2	TC4-1W	Mini-Circuits		T1, T2	
Transformer	MC-CD542	1	ADT4-1WT	Mini-Circuits		T3	

Value	Footprint	Qty	Part Number	Vendor	Digi-Key Number	REF DES	Not Installed
SMA connectors	SMA_Jack	4	901-144-8RFX	AMP	ARFX1231-ND	J1, J2, J3, J7	J4, J5
SMA edge-mount connectors	SMA_End	6	82 SMA-S50-0-45/111_NE	HUBER		J9, J15, J16, J21, J22, J23	
Black test point	Test_point	4	5011K-ND	Keystone	5011K-ND	TP1, TP3, TP4, TP5	
RED test point	Test_point	0	5010K-ND	Keystone	5010K-ND		TP6, TP7
RED test point	Test_point2	4	5000K-ND	Keystone	5000K-ND	TP2, TP8, TP9, TP10	TP11
2-pos header	2pos_jumper	5	HTSW-150-07-L-S	Samtec		W3, W6, W7, W8, W9	W1, W4
3-pos header	3pos_jumper	1	HTSW-150-07-L-S	Samtec		W2	
3-circuit jumpers	SJP3	0					SJP1, SJP2, SJP6
5-circuit jumpers	5POS_ JUMPER_TH	1				W5	
Switch	EVQ-PJ	1	EVQ-PJX04M	Panasonic	P8050SCT-ND	S1	S2
Switch, 4-position	SWITCH_ 4POS_SMT	0	DHS4S	APEM			S3, S4
Switch, 8-position	SWITCH_ 8POS_SMT	0	DHS8S	APEM			S5
40-pin IDC connector	20X2X.1	1	HTSW-120-07-L-D	Samtec	N/A	J8	
10-pin IDC connector	5X2X.1	0	HTSW-120-07-L-D	Samtec			J6
Red banana jack	BANANA_ JACK	5	ST-351A	ALLIED		J11, J13, J14, J17, J19	

Value	Footprint	Qty	Part Number	Vendor	Digi-Key Number	REF DES	Not Installed
Black banana jack	BANANA_ JACK	4	ST351B	ALLIED		J10, J12, J18, J20	
Green LED	LED-1206	0	CMD15-21VGC/ TR8	Panasonic	L62205CT-ND		D1
ADS5500IPAP(1)	64-HTQFP (PAP)	1	ADS5500IPAP	TI		U1	
THS4503ID(1)	8-SOP(D)	1	THS4503ID	TI	296-12938-5-ND	U2	
OPA4227UA	14-SOP(D)	0	OPA4227UA	TI	OPA4227UA-ND		U3
TPS79225DBVR	5-SOT(DBV)	0	TPS79225DBVR	TI	296-11869-2-ND		U4
MC10EP16DT	8-TSSOP (DGK)	1	MC10EP16DT	ON Semi-conductor	MC10EP16DTOS-ND	U5	
TPS3801J25DCKR	5-SOT(DCK)	0	TPS3801J25DCKR	TI	296-3326-2-ND		U6
SN75LVDT1422PAG (1)	64-TQFP (PAG)	1	SN75LVDT1422PAG	TI		U7	
EPM7032BTC44	44-TQFP (PGT)	0	EPM7032BTC44-3	ALTERA			U8
Screws	4-40 screw	4					
Plastic standoff, hex (1/4 x .5”)	4-40 screw	4	1902CK-ND	Allied	1902CK-ND		

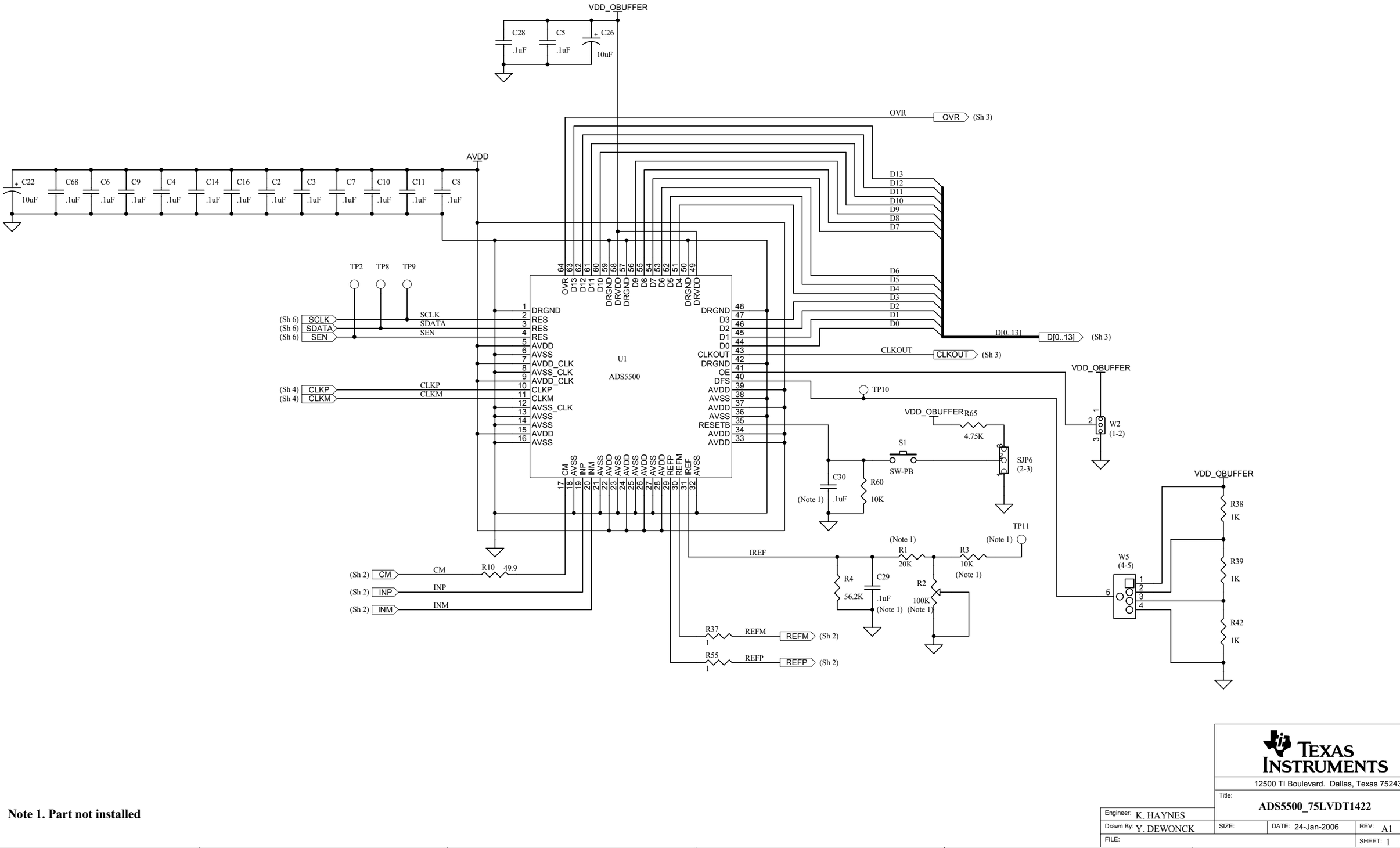
(1) TI-supplied

Surface-mount jumper location: SJP6 = 2−3; SJP1 = 2−3; SJP2 = 1−2

Jumper shunt location: W2 pins 1−2, W5 pins 4−5; do not install W1, W3, W4, W6, W7

3.3 Schematics

The following pages contain the schematics.



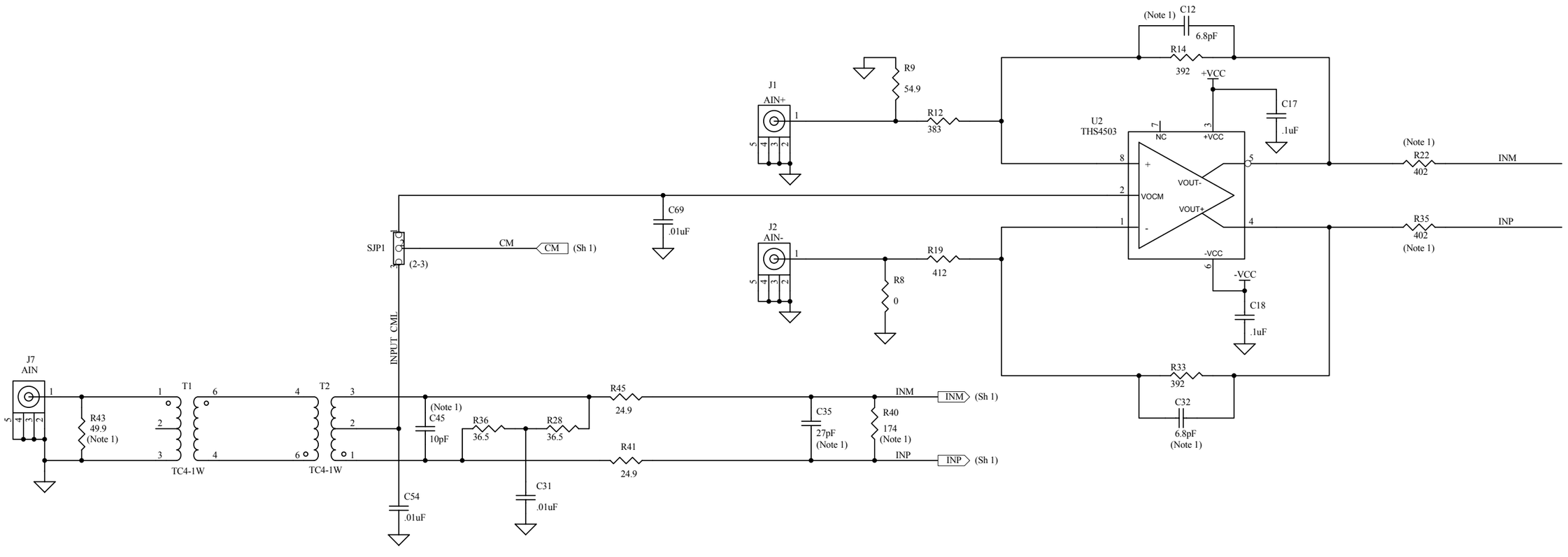
Note 1. Part not installed

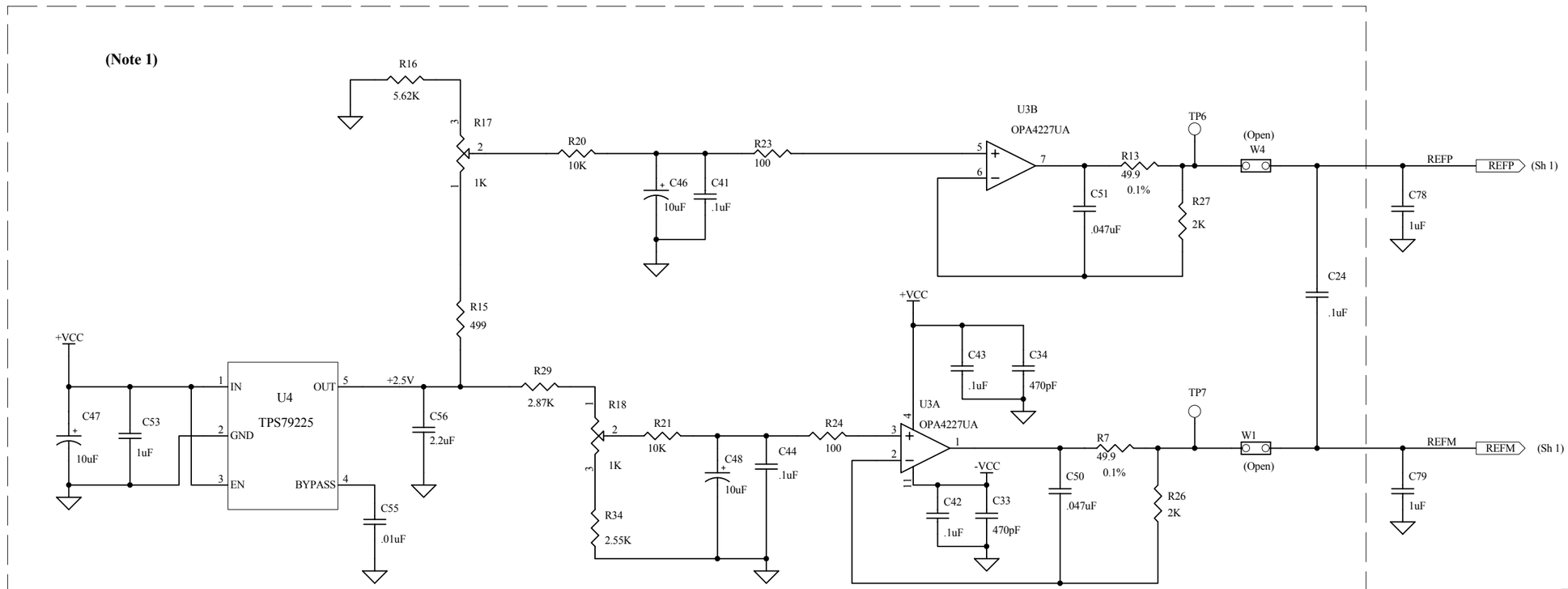
TEXAS INSTRUMENTS

12500 TI Boulevard. Dallas, Texas 75243

Title: **ADS5500_75LVDT1422**

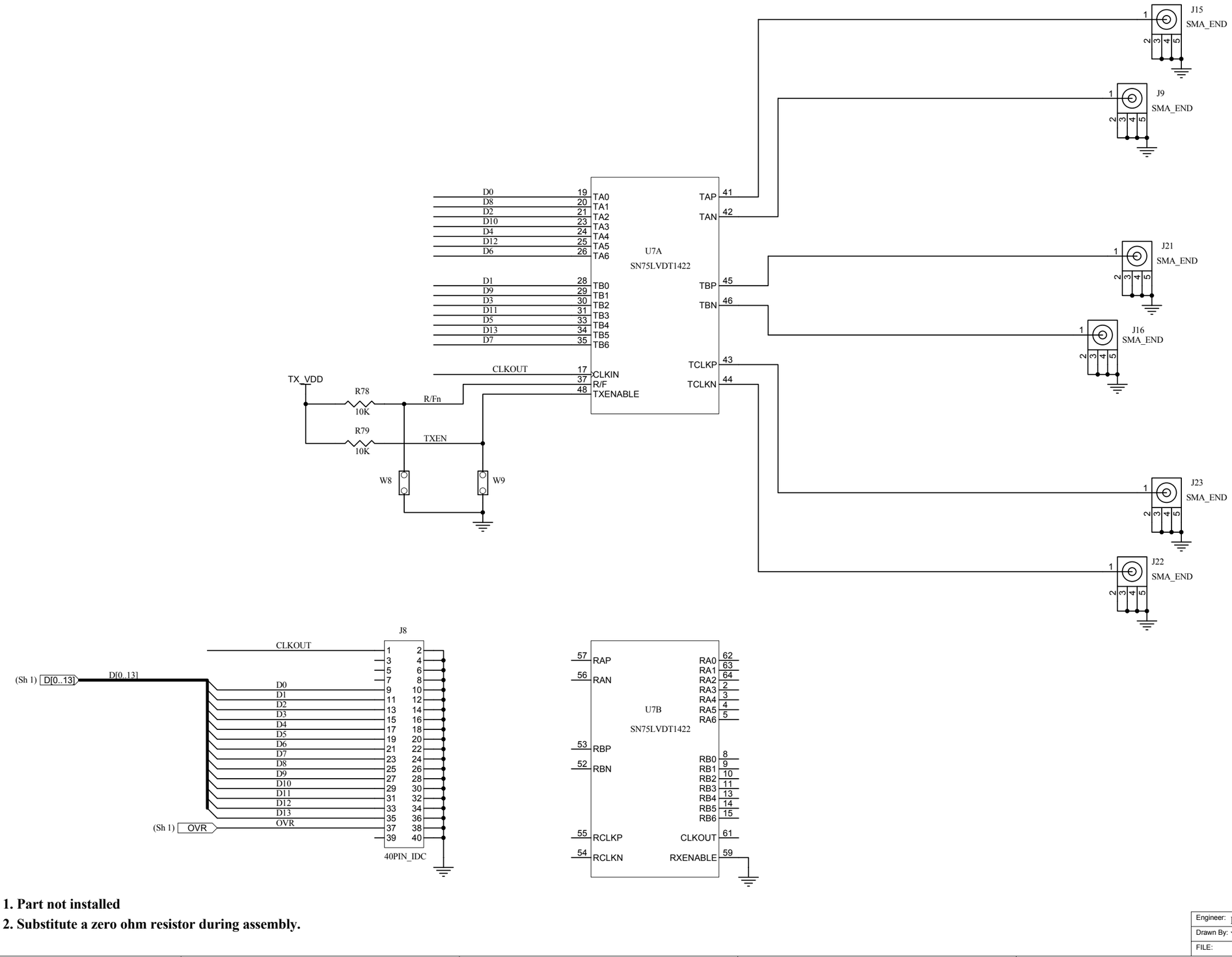
Engineer: K. HAYNES			
Drawn By: Y. DEWONCK	SIZE:	DATE: 24-Jan-2006	REV: A1
FILE:			SHEET: 1 OF: 6





Note 1. Part not installed

Engineer: K. HAYNES	TEXAS INSTRUMENTS		
Drawn By: Y. DEWONCK	12500 TI Boulevard. Dallas, Texas 75243		
FILE:	Title: ADS5500_75LVDT1422		
	DOCUMENTCONTROL #		REV: A1
	DATE: 24-Jan-2006	SIZE:	SHEET: 2 OF: 6



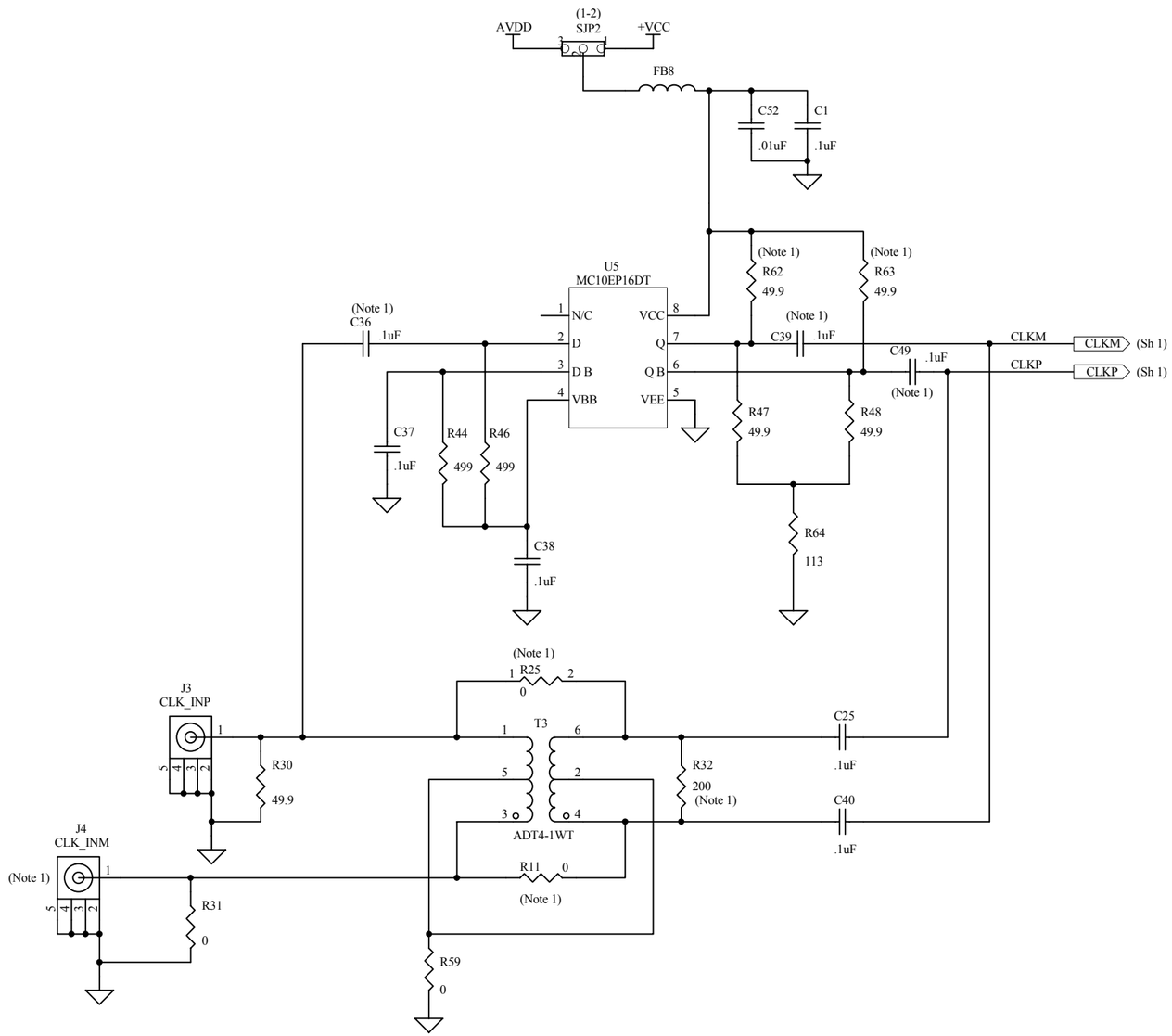
Note 1. Part not installed

Note 2. Substitute a zero ohm resistor during assembly.

TEXAS INSTRUMENTS

12500 TI Boulevard. Dallas, Texas 75243

Engineer: K. HAYNES	Title: ADS5500_75LVDT1422		
Drawn By: Y. DEWONCK	DOCUMENTCONTROL #		REV: A1
FILE:	DATE: 24-Jan-2006	SIZE:	SHEET: 3 OF: 6



Note 1. Part not installed

Engineer: K. HAYNES	
Drawn By: Y. DEWONCK	
FILE:	

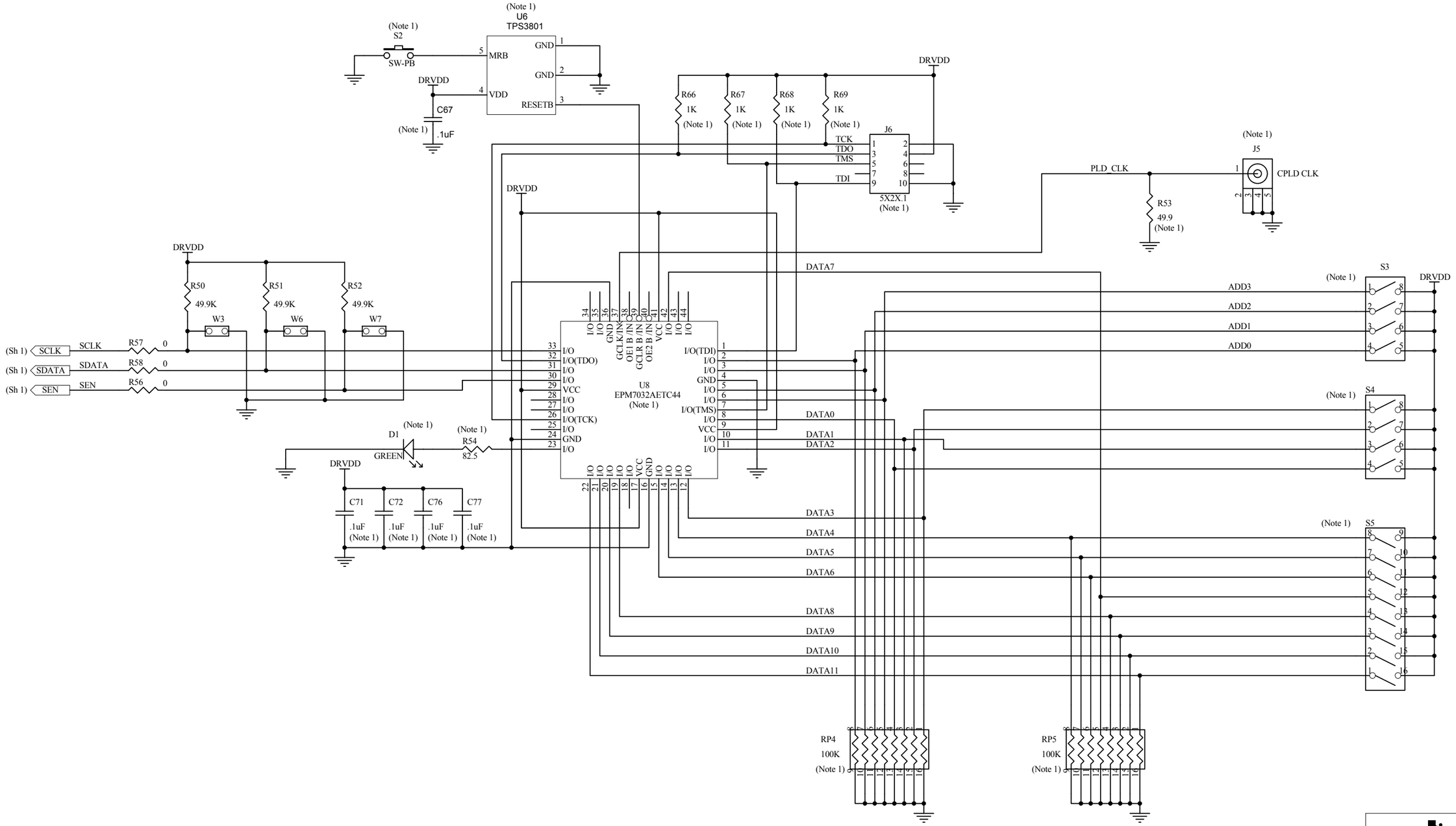
TEXAS INSTRUMENTS

12500 TI Boulevard. Dallas, Texas 75243

Title: **ADS5500_75LVDT1422**

DOCUMENTCONTROL # | REV: A1

DATE: 24-Jan-2006 | SIZE: | SHEET: 4 OF: 6



Note 1. Part not installed

TEXAS INSTRUMENTS
12500 TI Boulevard. Dallas, Texas 75243

Title: **ADS5500_75LVDT1422**

Engineer: K. HAYNES			
Drawn By: Y. DEWONCK	SIZE:	DATE: 24-Jan-2006	REV: A1
FILE:			SHEET: 5 OF: 6