Functional Safety Information

TCAN1051-Q1 and TCAN1051V-Q1 Functional Safety FIT Rate, FMD, and Pin FMA

Table of Contents

List of Figures

List of Tables

Trademarks

1 Overview

This document contains information for TCAN1051-Q1 and TCAN1051V-Q1 (as well as the TCAN1051H-Q1, TCAN1051G-Q1, TCAN1051HV-Q1, TCAN1051GV-Q1, TCAN1051HG-Q1 and TCAN1051HGV-Q1). These are Controller Area Network (CAN) transceivers in the SOIC (D) and VSON (DRB) packages to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

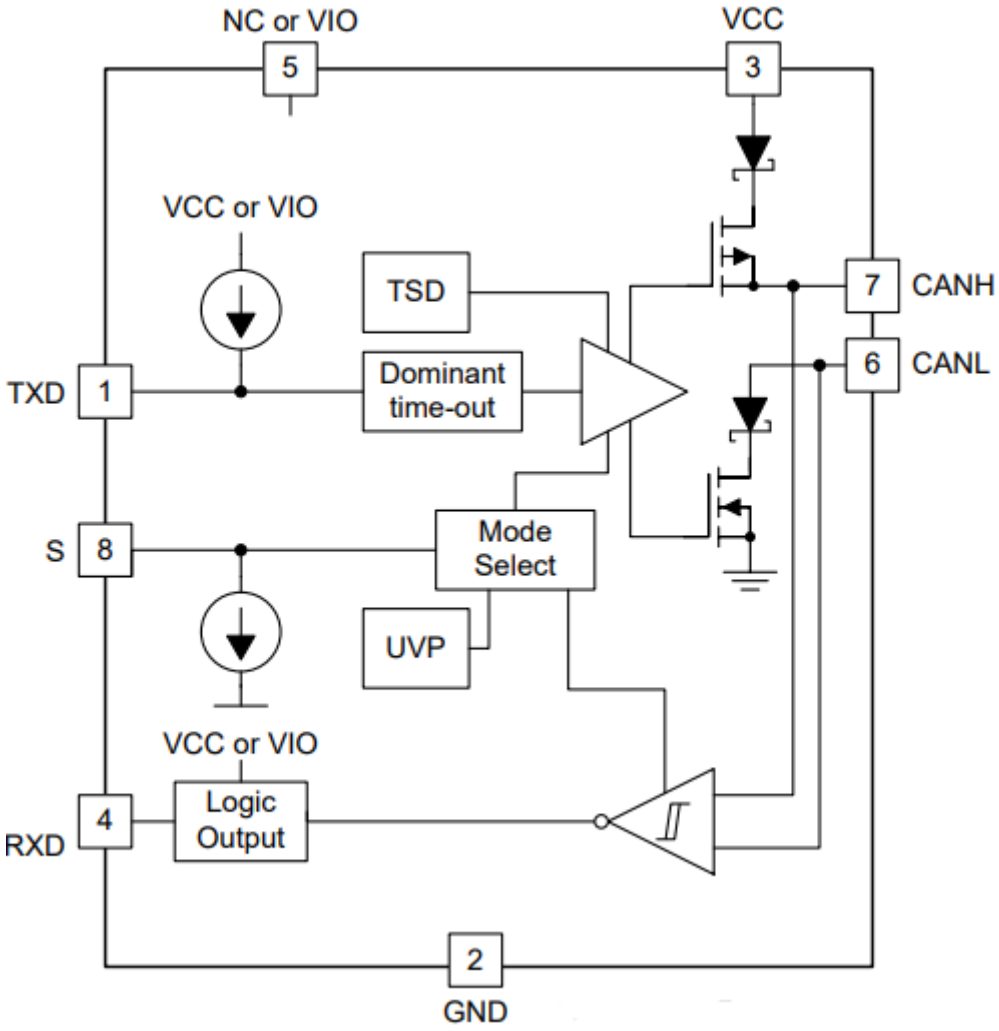

Figure 1-1. Functional Block Diagram

TCAN1051-Q1 and TCAN1051V-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for TCAN1051-Q1 and TCAN1051V-Q1 (as well as the TCAN1051H-Q1, TCAN1051G-Q1, TCAN1051HV-Q1, TCAN1051GV-Q1, TCAN1051HG-Q1 and TCAN1051HGV-Q1) based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours) 8-pin SOIC (D)	FIT (Failures Per 10^9 Hours) 8-pin VSON (DRB)
Total Component FIT Rate	12	6
Die FIT Rate	4	2
Package FIT Rate	8	4

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 124 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS ASICs Analog & Mixed =<50V supply	20 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TCAN1051-Q1 and TCAN1051V-Q1 (as well as the TCAN1051H-Q1, TCAN1051G-Q1, TCAN1051HV-Q1, TCAN1051GV-Q1, TCAN1051HG-Q1 and TCAN1051HGV-Q1) in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Transmitter fail	45%
Receiver fail	45%
CANL or CANH driver stuck dominant	5%
Short circuit any two pins	5%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of TCAN1051-Q1 and TCAN1051V-Q1 (as well as the TCAN1051H-Q1, TCAN1051G-Q1, TCAN1051HV-Q1, TCAN1051GV-Q1, TCAN1051HG-Q1 and TCAN1051HGV-Q1). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2.)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to VCC (see Table 4-5)
- Pin short-circuited to VBAT (see Table 4-6)
- Pin short-circuited to VIO (see Table 4-7)

Table 4-2 through Table 4-7 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- VCC = 4.5 to 5.5V
- VBAT = 6 to 24V
- VIO = 3 to 5.5V

4.1 SOIC and VSON Packages

Figure 4-1 shows the TCAN1051-Q1/TCAN1051V-Q1 SOIC pin diagram. Figure 4-2 shows the TCAN1051-Q1/TCAN1051V-Q1 VSON pin diagram. For a detailed description of the device pins please refer to the Pin Configurations and Functions section in the TCAN1051-Q1/TCAN1051V-Q1 data sheet.

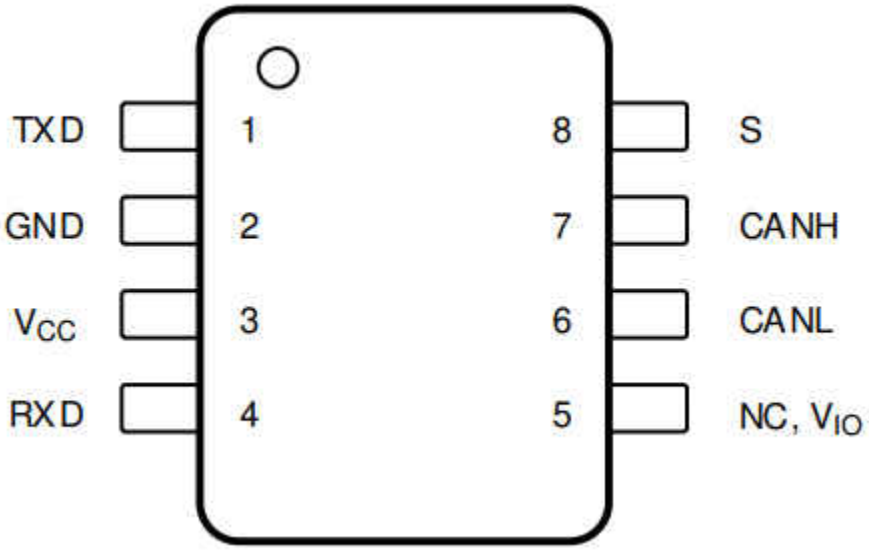

Figure 4-1. SOIC Pin Diagram

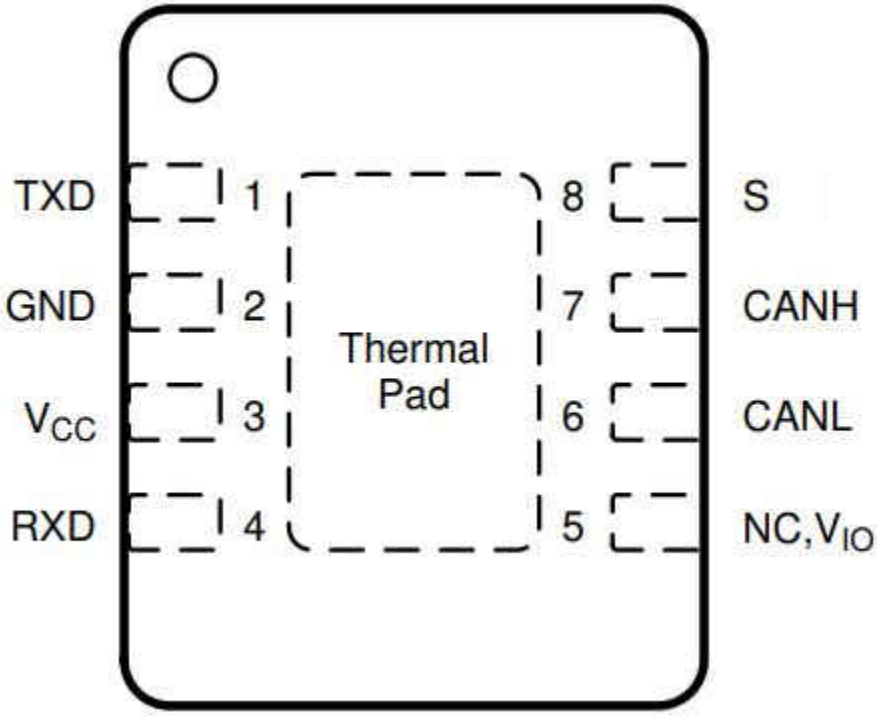

Figure 4-2. VSON Pin Diagram

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
TXD	1	Device will enter dominant time out mode. Unable to transmit data.	B
GND	2	None	D
VCC	3	Device unpowered, high I_{CC} current.	B
RXD	4	Transceiver output biased dominant, unable to receive data from the CAN bus. Internal damage possible.	A
NC	5	None	D
VIO	5	Device will be in protected mode. Transceiver passive on bus.	B
CANL	6	$V_{O(REC)}$ spec violated. Degraded EMC performance.	C
CANH	7	Device cannot drive dominant to the bus, no communication possible.	B
S	8	S biased low, transceiver unable to enter silent mode.	B
Thermal Pad	-	None	D

Note

The VSON package includes a thermal pad.

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
TXD	1	TXD pin defaults recessive, device always recessive and unable to transmit data.	B
GND	2	Device unpowered.	B
VCC	3	Device unpowered.	B
RXD	4	No RXD output, unable to receive data.	B
NC	5	None	D
VIO	5	Device will be in protected mode. Transceiver passive on bus.	B
CANL	6	Device cannot drive dominant on the bus, unable to communicate.	B
CANH	7	Device cannot drive dominant on the bus, unable to communicate.	B
S	8	S pin defaults high, transceiver stuck in silent mode.	B
Thermal Pad	-	None	D

Note

The VSON package includes a thermal pad.

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
TXD	1	GND	Device will enter dominant time out mode. Unable to transmit data.	B
GND	2	VCC	Device unpowered, high I_{CC} current.	B
VCC	3	RXD	RXD output biased recessive, unable to receive data.	B
NC	5	CANL	None	D
VIO	5	CANL	Bus biased recessive, no communication possible. I_{OS} current may be reached on CANL.	B
CANL	6	CANH	Bus biased recessive, no communication possible. I_{OS} current may be reached on CANH/CANL.	B
CANH	7	S	Driver turns off when a dominant is driven. May not enter normal mode.	B

Note

The VSON package includes a thermal pad. All device pins are adjacent to the thermal pad. The device behavior when pins are shorted to the thermal pad depends on which net is connected to the thermal pad.

Table 4-5. Pin FMA for Device Pins Short-Circuited to VCC

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
TXD	1	TXD biased recessive, unable to transmit data.	B
GND	2	Device unpowered, high I_{CC} current.	B
VCC	3	None	D
RXD	4	RXD pin biased recessive, unable to receive data.	B
NC	5	None	D
VIO	5	IO pins will operate as 5V input/outputs. Microcontroller may be damaged if VCC > VIO.	C
CANL	6	RXD always recessive, no communication possible. I_{OS} current may be reached.	B
CANH	7	$V_{O(REC)}$ spec violated, degraded EMC performance.	C
S	8	S biased high, transceiver always in silent mode.	B

Table 4-6. Pin FMA for Device Pins Short-Circuited to VBAT

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
TXD	1	Absolute maximum violation, transceiver may be damaged. Unable to transmit data.	A
GND	2	Device unpowered, high I_{BAT}current	B
VCC	3	Absolute maximum violation, transceiver may be damaged. Bus may be unable to communicate.	A
RXD	4	Absolute maximum violation, transceiver may be damaged. Unable to receive data.	A
NC	5	None	D
VIO	5	Absolute maximum violation, transceiver may be damaged.	A
CANL	6	RXD always recessive, no communication possible. I_{OS}current may be reached.	B
CANH	7	$V_{O(REC)}$ spec violated, degraded EMC performance.	C
S	8	Absolute maximum violation, transceiver may be damaged. Transceiver stuck in silent mode.	A

Table 4-7. Pin FMA for Device Pins Short-Circuited to VIO

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
TXD	1	TXD biased recessive indefinitely, unable to transmit data.	B
GND	2	Device unpowered, high I_{IO} current.	B

Table 4-7. Pin FMA for Device Pins Short-Circuited to VIO (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VCC	3	IO pins will operate as 5V input/outputs. Microcontroller may be damaged if VCC > VIO.	C
RXD	4	RXD pin biased recessive indefinitely, unable to receive data.	B
NC	5	None	D
VIO	5	None	D
CANL	6	RXD always recessive, no communication possible. I_{OS} current may be reached if VIO ≥ 3.3V.	B
CANH	7	$V_{O(REC)}$ spec violated if, degraded EMC performance.	C
S	8	S biased high indefinitely, transceiver always in silent mode.	B

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (August 2021) to Revision B (December 2021) **Page**

- Added references to the document for TCAN1051H-Q1, TCAN1051G-Q1, TCAN1051HV-Q1, TCAN1051GV-Q1, TCAN1051HG-Q1 and TCAN1051HGV-Q1 2

Changes from Revision * (November 2020) to Revision A (August 2021) **Page**

- Changed the RXD pin description in the *Pin FMA Short-Circuited to Ground* table 4

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265