Functional Safety Information

SN6505x-Q1 Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

Trademarks

1 Overview

This document contains information for SN6505x-Q1 (SOT-23 (6) package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

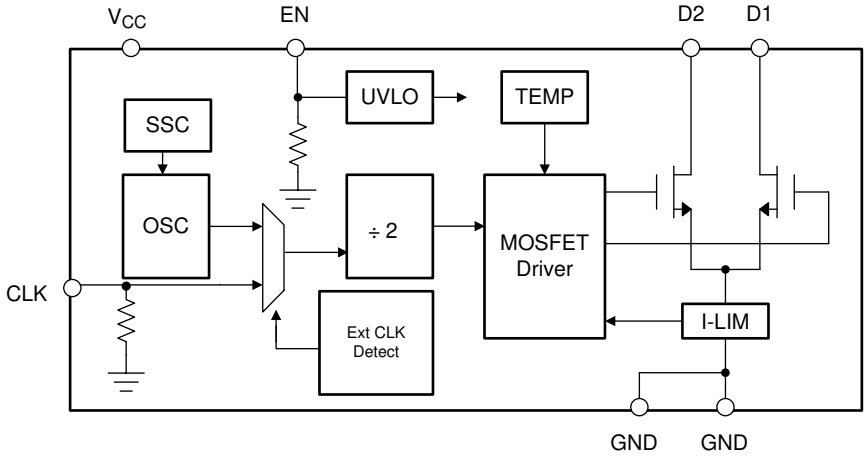

Figure 1-1. Functional Block Diagram

SN6505x-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 SOT-23 (6) Package

This section provides Functional Safety Failure In Time (FIT) rates for SOT-23 (6) package of SN6505x-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	6
Die FIT Rate	2
Package FIT Rate	4

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: TBD mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for SN6505x-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
D1 and/or D2 FET stuck off	43%
D1 and/or D2 FET stuck ON	31%
D1 and/or D2 output not in timing or voltage specification	20%
D1 and/or D2 output undetermined	6%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the SN6505x-Q1 (SOT-23 (6) package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (seeTable 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- External push-pull transformer connected with a winding between D1 and V_{CC}, another winding connected between D2 and V_{CC}.

4.1 SOT-23 (6) Package

Figure 4-1 shows the SN6505x-Q1 pin diagram for the SOT-23 (6) package. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the SN6505x-Q1 data sheet.

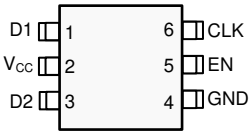

Figure 4-1. Pin Diagram (SOT-23 (6)) Package

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
D1	1	D1 pin stuck low creates short circuit path between Vcc and ground through transformer winding, causing high current to flow and possible damage to transformer. Output voltage out of designed spec.	A
V_{CC}	2	No power to the device. No isolated output voltage.	B
D2	3	D2 pin stuck low creates short circuit path between Vcc and ground through transformer winding, causing high current to flow and possible damage to transformer. Output voltage out of designed spec.	A
GND	4	Device continues to function as expected. Normal operation.	D
EN	5	Disables the device. No isolated output supply generated.	B
CLK	6	With CLK stuck low, external clock synchronization functionality is disabled.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
D1	1	With D1 open, one primary transformer winding does not store energy. Isolated output supply out of intended set-point.	B
V_{CC}	2	No power to device, so no switching action of D1/D2. Isolated output voltage does not build up.	B
D2	3	With D2 open, one primary transformer winding does not store energy. Isolated output supply out of intended set-point.	B
GND	4	No power to device, so no switching action of D1/D2. Isolated output voltage does not build up.	B
EN	5	Disables the device. No isolated output supply generated.	B
CLK	6	With CLK pin open, external clock synchronization functionality is lost.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
D1	1	V_{CC}	D1 stuck high. Makes potential difference between one transformer winding zero. When D1 FET switches on, high current flows from supply to ground. Isolated output supply out of intended set-point.	A
V_{CC}	2	D2	D2 stuck high. Makes potential difference between one transformer winding zero. When D2 FET switches on, high current flows from supply to ground. Isolated output supply out of intended set-point.	A
D2	3	GND	Not considered. Corner pin.	D
GND	4	EN	EN stuck low. Disables the device. No isolated output supply generated.	B
EN	5	CLK	If EN is tied high on PCB, external clock synchronization functionality is lost.	B
CLK	6	D1	Not considered. Corner pin.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
D1	1	D1 stuck high. Makes potential difference between one transformer winding zero. When D1 FET switches on, high current flows from supply to ground. Isolated output supply out of intended set-point.	A
V_{CC}	2	No effect. Normal operation.	D
D2	3	D2 stuck high. Makes potential difference between one transformer winding zero. When D2 FET switches on, high current flows from supply to ground. Isolated output supply out of intended set-point.	A
GND	4	No power to device, so no switching action of D1/D2. Isolated output voltage does not build up.	B
EN	5	With EN stuck high, functionality to disable the device lost.	B
CLK	6	With CLK stuck high, functionality to synchronize with external clock lost.	B

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