Application Note

Construction and Marking Report for ATEX / IECEx Certification

1 Construction and Marking Report for ATEX / IECEx Certification

1.1 ISO7021 and ISO7021F Device Construction Information

The components being certified comply with IEC 60079-0 Edition 7 and IEC 60079-11 Edition 6. When one of these components is used in equipment, the component is soldered onto a PCB inside a suitable enclosure and reevaluated as equipment. The creepage and clearance distances across the isolating component have been evaluated, but the distance to other circuitry remains the end-equipment user's responsibility.

When the component is fitted in intrinsically-safe equipment, a 500V Routine Dielectric Strength Test must be conducted in accordance with clause 6.3.13 of IEC 60079-11:2011.

This assembly is an isolating component between separate, intrinsically-safe circuits. The assembly must be connected to suitable, certified, intrinsically-safe circuits, and consider the following entity parameters:

Table 1-1. Entity Parameters for an a Typical Application

PACKAGE	ENTITY PARAMETERS FOR SIDE 1	ENTITY PARAMETERS FOR SIDE 2	AMBIENT TEMPERATURE RANGE
SOIC-8 (D)	Ui = 50V	Ui = 50V	-55°C to +85°C
	Ii = 300mA	Ii = 300mA	
	Pi = 1.0W	Pi = 1.0W	
	Li = 0	Li = 0	
	Ci = 4pF	Ci = 4pF	

1.2 Information About Pin Numbers and Pin Signal Names

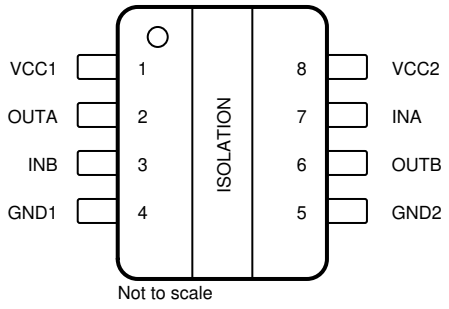

Figure 1-1. ISO7021 and ISO7021F Pin-out

The ISO7021 and ISO7021F are dual-channel digital isolators. This assembly can be used as an isolating component between separate, intrinsically-safe circuits. The two-channel isolator comes in a 8-SOIC package with one forward-direction channel and one reverse direction channel. The device has default high and low output options. If the input power, or signal, is lost, default output is high for the ISO7021 and low for the ISO7021F.

1.3 Constructional Diagrams

Figure 1-2 displays mount and bond diagram of the ISO7021.

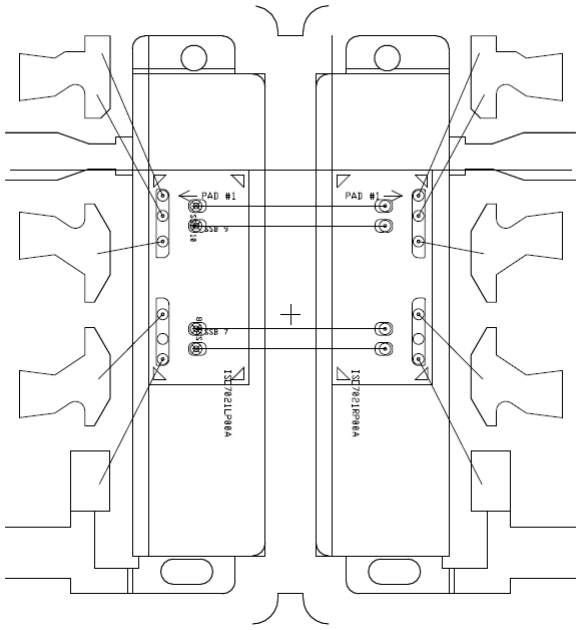

Figure 1-2. ISO7021D Mount and Bond Diagram

Figure 1-3 displays mount and bond diagram of the ISO7021F.

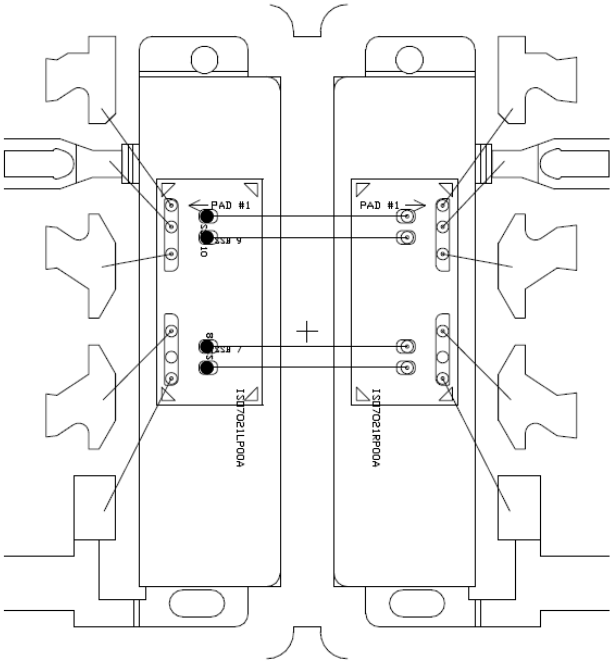

Figure 1-3. ISO7021FD Mount and Bond Diagram

1.4 Information About Creepage and Clearance Specification

The minimum specified creepage and clearance distance across the ISO7021 and ISO7021F digital isolator in the 8-SOIC (D) package is 4.0mm. This is above the 3.0mm minimum requirement of Table 5 of IEC 60079-11:2011 for peak voltage up to 60V for Ex ia level of protection. The CTI is specified to be at least 600V.

Creepage is the shortest path between two conductive parts across the isolation barrier. Creepage is measured along the surface of the insulation. This path is typically found around the end of the package body, as shown in Figure 1-4.

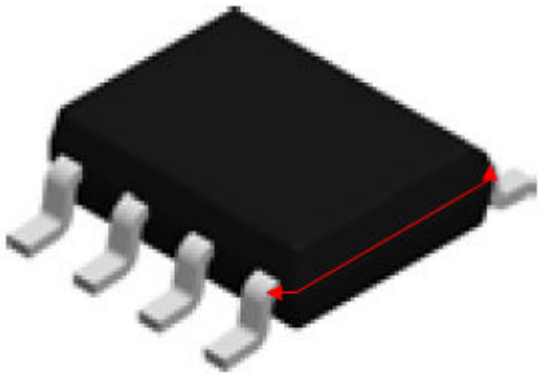

Figure 1-4. Creepage and Clearance Around a Side

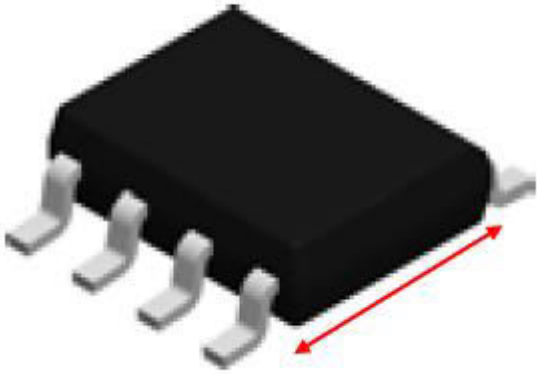

Figure 1-5. Clearance Below the Package in a Straight Line

Clearance is the shortest path between conductive leads across the isolation barrier. Clearance is measured through the air. This path can be the same as shown in Figure 1-4 or, if the leads on both sides are in line of sight, a straight line below the package body as shown in Figure 1-5.

1.5 Mechanical Data

Figure 1-6 shows the SOIC-8 or D Package dimensions.

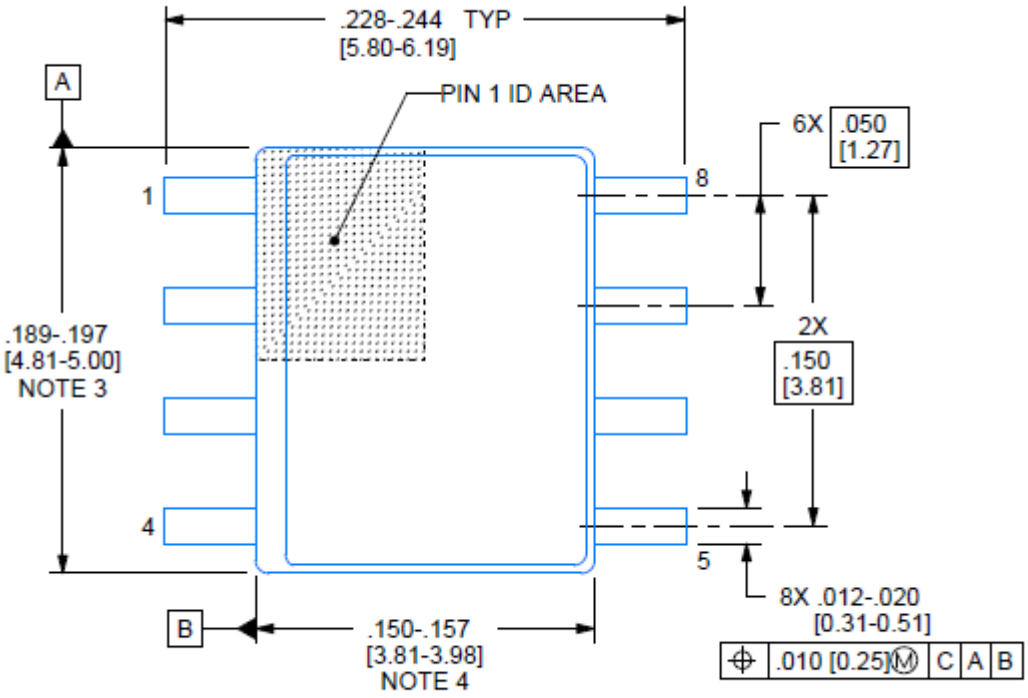

Figure 1-6. Dimensions of SOIC-8 Package

1.6 Isolation Capacitor Technology

The primary isolation barrier in the ISO7021 and ISO7021F consists of two high-voltage isolation capacitors in series. Each capacitor resides inside the plastic package, on the left and right side chips, respectively. Both capacitors are connected to each other through inter-die bond wires. The isolation capacitors are integrated inside each die using TI's proprietary LBC8LViso.2 chip fabrication process technology. Each isolation capacitor has a minimum dielectric thickness of 8.5µm, which is made up of SiO2, SiN, and SiON. The dielectric in each capacitor consists of three inter-metal dielectric (IMD) layers as shown in Table 1-2.

Table 1-2. Inter-metal Dielectric (IMD) Layers

CAP 1 LAYER #	COMPOSITION	TYPICAL THICKNESS (µm)
IMD2	SiO2	2.4
IMD3	SiO2	3.7
IMD4	SiO2, SiN, SiON	3.7

The typical dielectric thickness of each capacitor is 9.8µm. Therefore, with two capacitors in series, each ISO7021 and ISO7021F device has typical dielectric thickness of 19.6µm and minimum thickness of 17µm. The SOIC-8 package lead frame has a pad-to-pad spacing of >0.4mm.

1.7 Assembly Information

This device uses molding compound CEL-8240HF10GK, which is manufactured by Hitachi. The composition of this molding compound is Epoxy Resin-1, Epoxy Resin-2, Phenol resin, Amorphous Silica, and Carbon Black. Minimum thermal conductivity of the compound is 15E-04cal/cm.S.°C. Gold bond wires are supplied by Tanaka;

the bond wires have a diameter of 24.3µm. Similarly, mount compound, or adhesive, is CRM-1076WD which is supplied by Sumitomo.

1.8 ISO7021 and ISO7021F Device Marking Information

Device marking information is provided below.

Table 1-3. Manufacturer Name, Address, and Manufacturing Locations

Manufacturer's Name	Texas Instruments, Inc.
Manufacturer's Address	12500 TI Blvd, J2-1534, Dallas TX 75243 USA
Manufacturing Locations	Texas Instruments Taiwan Limited

Table 1-4 shows the certification information for these devices.

Table 1-4. Certification Information

Certification Number	IECEx CSA 20.0012U and CSANe 20ATEX2090U
Certification Code	 II 1G xxxx Ex ia IIC Ga (1)

(1) XXXX is the 4-digit identification number of the notified body issuing the QAN for this product.

1.8.1 Location and Details of Marking on the IC

The following is the ISO7021 device marking and symbolization instructions in the Texas Instruments Assembly and Test Specification System (ATSS) document.

```
Topside Symbol          : 8D
  +----------------+             \T/ = TI LOGO
  ![] 7021         !              Y  = YEAR
  ![] \T/YMS       !              M  = MONTH
  ![]   LLLLG4     !              S  = ASSY SITE CODE
  ![]              !           LLLL  = LOT TRACE CODE
  +----------------+
  [] = PIN 1 STRIPE              LINE 1 MAXIMUM IS  6 CHARACTERS
                                 NOTE: G4     MUST BE SYMBOLIZED
                                 WITH AN UNDERSCORE, IF PRESENT.

  #SYMBOL ECAT : G4     MUST BE SYMBOLIZED WITH AN UNDERSCORE
  #SYMBOL DEVICE NAME : 7021
```

The following is the ISO7021F device marking and symbolization instructions in Texas Instruments Assembly and Test Specification System (ATSS) document.

```
Topside Symbol          : 8D
  +----------------+             \T/ = TI LOGO
  ![] 7021F        !              Y  = YEAR
  ![] \T/YMS       !              M  = MONTH
  ![]   LLLLG4     !              S  = ASSY SITE CODE
  ![]              !           LLLL  = LOT TRACE CODE
  +----------------+
  [] = PIN 1 STRIPE              LINE 1 MAXIMUM IS  6 CHARACTERS
                                 NOTE: G4     MUST BE SYMBOLIZED
                                 WITH AN UNDERSCORE, IF PRESENT.
```

```
    #SYMBOL ECAT : G4     MUST BE SYMBOLIZED WITH AN UNDERSCORE
    #SYMBOL DEVICE NAME : 7021F
```

2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (May 2020) to Revision A (December 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1

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