

Live Insertion With Differential Interface Products

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ABSTRACT

This document discusses concerns, ramifications, and solutions for applications involving live-insertion of interface circuits. Relevant and sometimes misused terms are defined, including live-insertion, hot-plugging, and glitch-free operation. Elements of the circuit solutions include failsafe receivers, drivers that are high impedance when disabled, and ESD protection.

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1 Introduction

Live insertion, hot plugging and hot swap are all terms that describe adding or removing devices to or from a common data bus without removing power from the entire bus. Depending on the source, each term may take on a different significance related to a level of performance or isolation. In the context of this paper, the term live insertion is used in a general sense meaning both insertion and removal of connections to an active bus and power cycling of connected devices.

Convenience and high availability are two of the requirements that have brought about the need for live insertion. The convenience of live insertion is found in the PC environment where peripheral devices can be added without powering down the computer. Another arena of live insertion is in high-availability systems, such as in telecommunications or data storage environments, where redundancy and live insertion allow the performance of maintenance without powering down or halting system activity.

The scope of live insertion design encompasses power management¹ as well as integrated circuit design, influencing all levels of design from system architecture to component selection. Two primary concerns of designing live insertion devices are part destruction and data corruption. The focus of this document is to look at integrated circuits (IC) solutions that address these concerns and identify Texas Instruments(TI) low-voltage differential signaling (LVDS), RS-485, and controller area network (CAN) interface features that provide these solutions.

2 Part Destruction

The first consideration should be the electrostatic discharge (ESD) experienced during insertion. ESD is the most common cause of part failure and destruction. Figure 1 shows a possible ESD event that could occur during live insertion, between a host and remote system due to connector misalignment or a variance in the connector pin length. This event is not dependent upon a power source, so ESD damage can also occur when no power is present (cold swap). From a system standpoint, the most straightforward way of preventing the event is eliminating any differences in potentials by establishing a ground connection before any other connection is made. The ground connection provides a path for any current that might otherwise pass through an IC. In Figure 2, the ground leads are longer than the other leads, ensuring a ground contact first.

¹Ti offers several power management devices for hot swap applications. For more information regarding hot swap power distribution devices refer to Power Management at TI's homepage, <http://www.ti.com>.

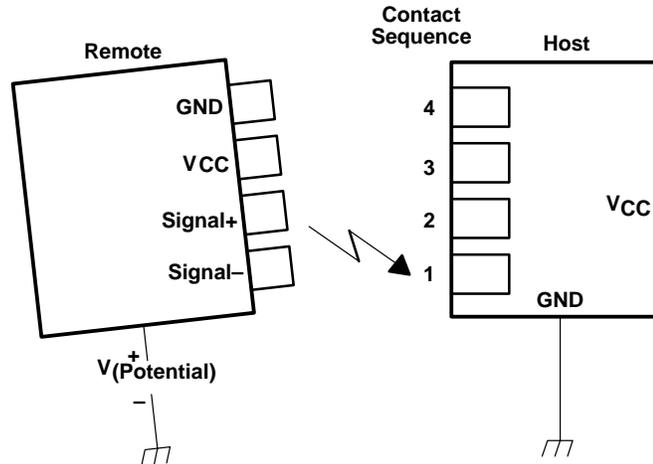


Figure 1. ESD Event

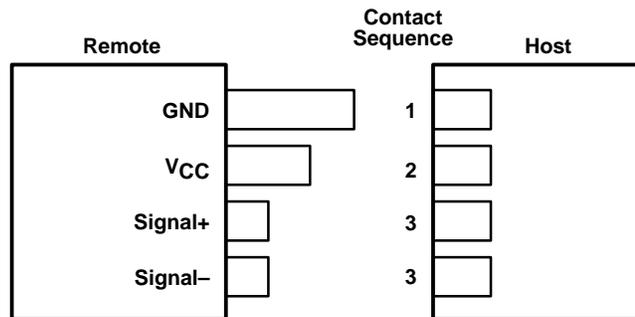


Figure 2. Ideal Contact Sequence

The use of an extended ground pin is not always a design option or useful in high-impedance circuits. In cases where grounding does not remove the accumulated charge(s) it is very important to pay attention to the interface IC and its ESD tolerance. The interface can be a specialized interface IC or integrated in a more complicated structure, such as a field programmable gate array (FPGA). The disadvantage of using an interface integrated with higher-level functions is that, generally, input/output (IO) size limitations prevent high levels of ESD tolerance. Specialized interface ICs are not restricted to standard IO pads and can dedicate more silicon to dissipating destructive transient energy. When weighed against the cost of system downtime or servicing, specialized interface ICs are often more cost effective over the product lifetime.

Protection and specification against all potential noise transients is likely impossible and, at the least, very expensive. A relative measure of the robustness of an interface is its ESD ratings. The ESD capabilities are most often rated in terms of the human body model (HBM) and the charged-device model (CDM). The CDM and HBM are described in JEDEC Standard 22 test method C101 and test method A114–A, respectively and MIL–STD–883C. TI offers many interface products with an HBM rating of 15 kV or higher. Although the HBM is intended as a measure of tolerance to ESD events during handling, high HBM ESD ratings correlate to robustness to other types of transient events including live insertion. These ratings are typically specified for the bus pins with respect to ground.

3 Data Corruption

In addition to part destruction from ESD, another concern in live insertion applications is data corruption. During live insertion, data corruption can occur for a number of reasons; glitches during power up, bus contention, insertion noise, and indeterminate inputs.

A simple solution for preventing data corruption during live insertion is to halt bus activity during live insertion. A drawback to this solution is the need to identify when a node is going to be removed or inserted; but more importantly, the suspended bus activity precludes the use of this solution in high-availability applications. In telecommunications, where redundancy and high availability are critical components, the ability to replace or remove redundant devices without impacting service or corrupting data is key to providing the five 9s of availability (99.999%).

If high availability requirements make halting the bus during insertion unattractive, then the characteristics of the interface devices become critical. Key features to consider in part selection of high availability systems are fail-safe, common-mode noise rejection, high impedance drivers, and glitch-free power up/down.

3.1 Glitch-Free Power Up/Down

After ESD considerations, the next concern is data corruption due to the application of power to an unpowered device. For example, in buses with a single transmitting node, a receiving node may remain powered during live insertion (or power cycling) of the transmitter. Here, the driver may be continuously enabled and an oscillation or glitch on a driver output during power up or down may be interpreted as valid data. In this case, it is important that the driver output change monotonically. The definition of glitch-free drivers is that the output makes only one transition, from high impedance to a low or high state when powering up, and the reverse when powering down. Figure 3 shows the glitches in a CMOS device during power up and power down, while Figure 4 demonstrates the glitch-free operation of the SN65LVDS050. Ch4 is the Vcc of the device, Ch1 and Ch3 are the differential driver outputs, and M1 is the differential voltage, Ch1–Ch3. A more detailed explanation of how glitches occur can be found in SLLA065, *A Comparison of LinBiCMOS and CMOS Process Technology in LVDS Integrated Circuits*.

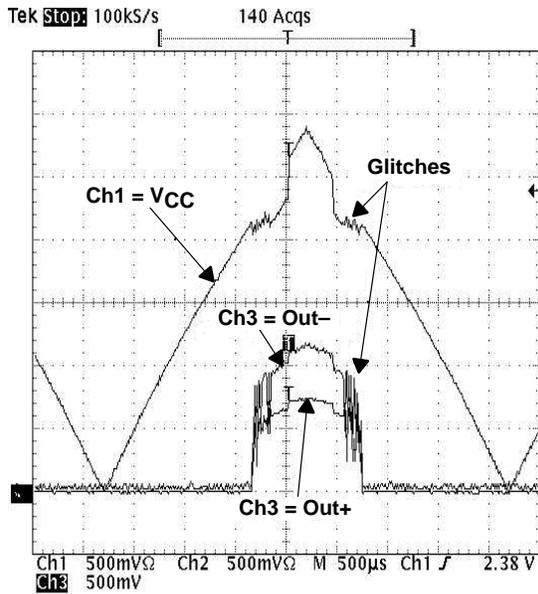


Figure 3. Glitches in Power Up/Down

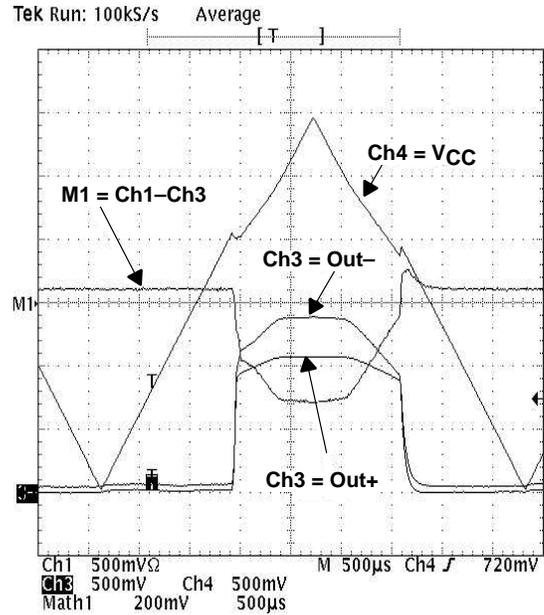


Figure 4. SN65LVDS050 Glitch-Free Feature

3.2 Driver Disable: Eliminating Bus Contention

Unlike the single driver systems, which benefit from the glitch-free feature, multipoint systems require multiple drivers with enable functions in order to prevent data corruption. In multipoint systems a possible scenario of data corruption during live insertion is when a node being inserted exerts a logic level on the bus while the bus is being driven to the opposite level by another node. This is referred to as bus contention.

Bus contention can be demonstrated in the simple bus circuit shown in Figure 5. One end of a bus is being driven by a transceiver, device A. The bus is terminated at both ends and Ch1 and Ch2 monitor each conductor at the end of the bus opposite driver A. When another transceiver (device B) is inserted onto the bus, and before the local controller can set control and data inputs, the inserted device transitions from a high impedance state to a logic low.

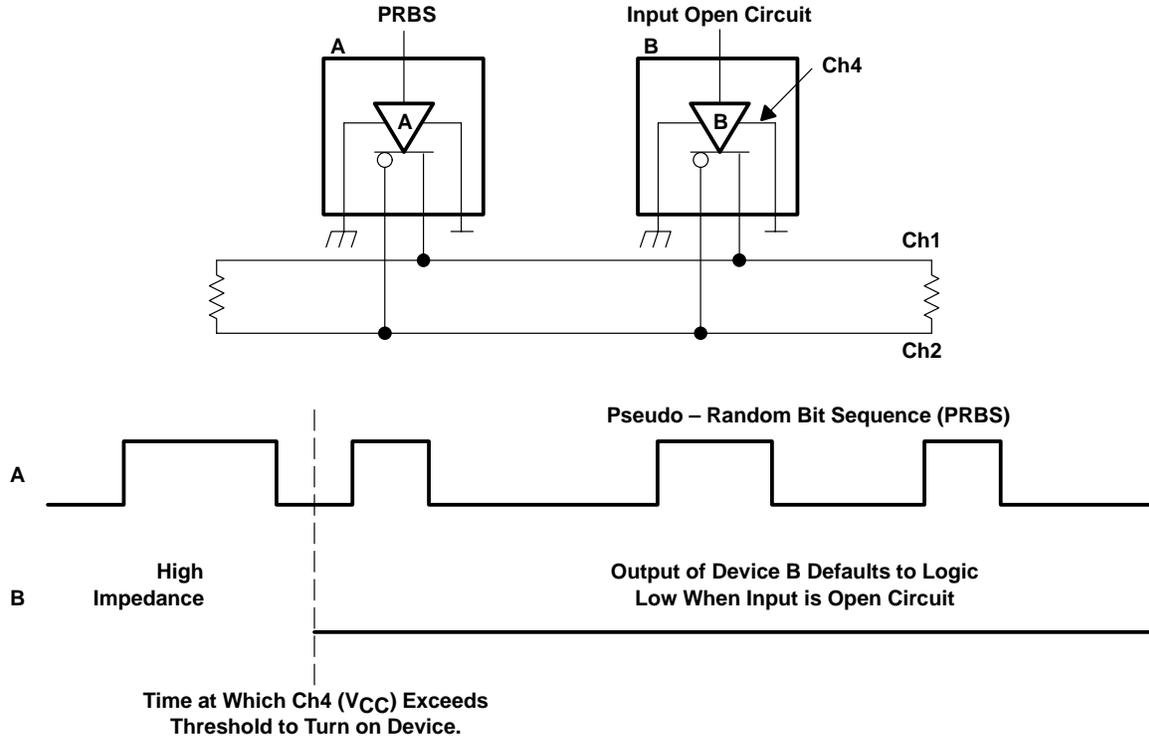


Figure 5. Bus Configuration

There is contention, as shown in Figure 6, when device B tries to drive the bus low and device A drives the bus high. This contention occurs immediately after Vcc of the inserted device (Ch4) reaches the power-on reset threshold. Figure 6 also shows the increased voltage differential when both are driving the same logic state.

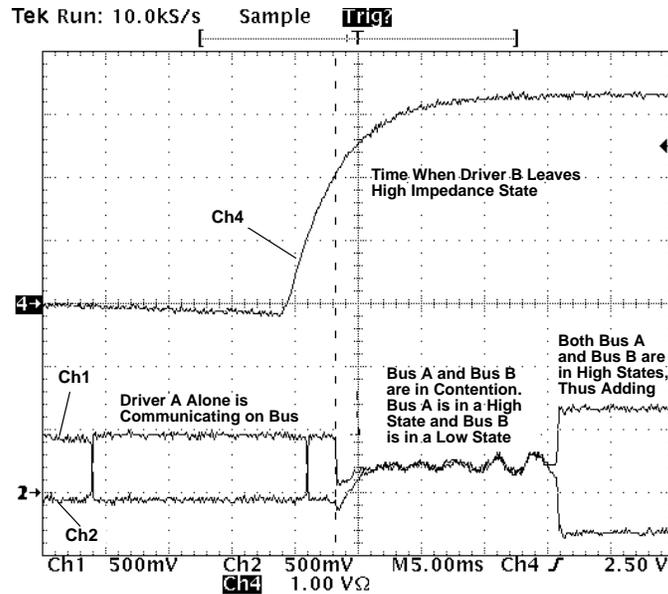


Figure 6. Bus Contention During Insertion

Keeping the transceiver outputs (of the device being inserted) in a high-impedance state during insertion and local controller initialization is required to prevent bus contention. TI transceivers provide several features to help prevent bus contention during this transition period. First, most driver enables are active high and have an internal pull-down resistor to disable the outputs with no input. Second, power-on/reset circuits maintain a V_{CC} threshold as high as possible such that inputs are ignored and outputs kept in a high impedance state until this V_{CC} threshold is attained. The assumption is that the device controlling the enable pins of the transceiver has become stable before the V_{CC} threshold is reached. If this is not the case, power management devices can be used to control when V_{CC} is supplied to the transceiver. In either case, predictable output behavior from the interface circuit is desirable.

NOTE: Characteristics of the interface circuit should be verified in its data sheet.

Figure 7 is the result from a setup similar to Figure 5, but with the driver disabled when the transceiver is inserted. Bus contention is also possible after insertion, however bus arbitration is a function of the controller and not the interface devices.

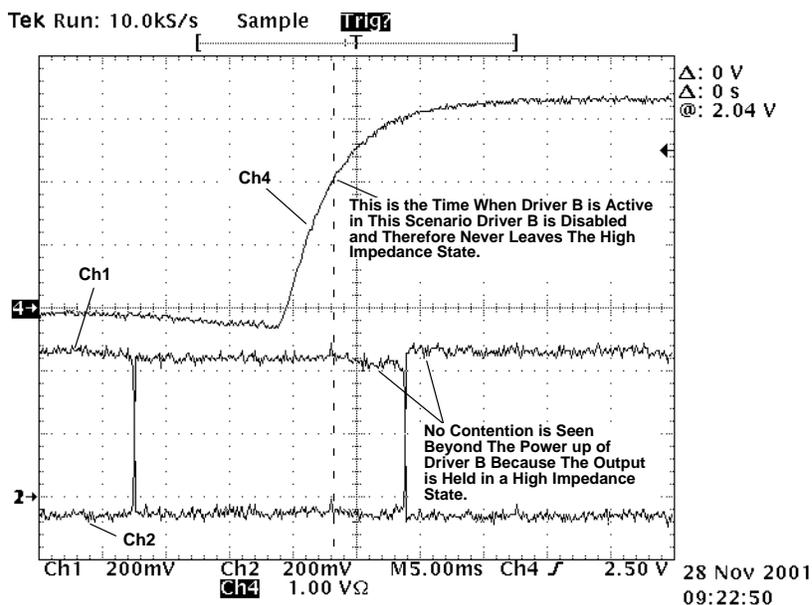


Figure 7. Driver Disabled During Insertion

3.3 Rejection of Insertion Noise (Common-Mode Rejection)

Insertion noise, due to bus-pin capacitance, can corrupt data in two ways. First, when inserted onto an active bus, the capacitance can draw current that is being used to transmit a signal, resulting in noise or ringing on the line. Second, the total capacitance of the node (pin, connector, trace, IC) influences the characteristic impedance of the bus ($Z=L/C$) and will result in noise on the line (reflections).

In a single-ended environment the noise from an insertion can corrupt the signal and justify the need for extra circuitry to precharge the bus-pin capacitance. However, in differential applications, this noise is seen equally on both sides of the differential pair, assuming that the bus pins connect nearly simultaneously and do not disturb the differential signal. The common-mode rejection, inherent to differential receivers, rejects the noise that is common to both conductors, thus allowing for live insertion without additional design considerations for precharging or other compensations. For a more in depth look at common-mode noise and rejection refer to TI Application Note SLLA057, *A Statistical Survey of Common Mode Noise*.

3.4 Failsafe Receivers

In most data buses, there are periods when there is no input provided to the line receivers. A predictable response to this condition is termed *failsafe*. The benefit of failsafe receivers is the provision of a deterministic output instead of a random logic state or oscillation between states due to noise on the line. During live insertion, all drivers are often disabled, allowing the bus to settle to some voltage. If this voltage is near the receiver input voltage threshold, random noise may cause the receivers to switch. The failsafe features of TI's LVDS, RS-485, and CAN products vary in complexity. The most basic failsafe feature is the output of a deterministic logic state when the inputs to the receiver are open circuited. Other failsafe structures deal with input voltages within the input voltage threshold range. The most advanced failsafe operation is the patented active failsafe provided in the SN65LVDS33 and SN65LVDS34. The active failsafe handles conditions of open- and short-circuited inputs. See reference 6 for detailed information about failsafe and the active failsafe feature.

4 Conclusion

When choosing an interface device for live insertion applications the following should be taken into consideration:

1. ESD Protection—TI offers many interface products with 15-kV or higher HBM ESD rating. Although the HBM is intended as a measure of tolerance to ESD events during handling, high HBM ESD ratings correlate to robustness to transient events including live insertion.
2. Glitch-free power up/down—Oscillations (glitches) can be seen on the outputs of a driver while the device is being inserted (power up) or removed (power down) and the driver tries to operate in suboptimal state. TI offers many interface products that provide glitch-free power up and power down operation.
3. High Impedance State—The TI transceivers provide enable features to maintain a high impedance state and prevent bus contention.
4. Common-Mode Rejection (Differential Signaling)—The common-mode rejection inherent to differential line receivers (and the TI LVDS, RS-485, and CAN products) greatly reduces false triggering or data corruption due to the insertion noise.
5. Failsafe Receivers—The response of line receivers to loss of input should be considered during design. TI offers a variety of line receivers with failsafe features. These include open-circuited and short-circuited inputs.

5 References

1. *Hot Swapping Signals*, EDN Magazine, July 5, 2001
2. *ESD Program Management*, Ted Dangelmayer, Van Nostrand Reinhold, 1990
3. SDYA012, *Live Insertion*, October 1996
4. SLLA057, *A Statistical Survey of Common Mode Noise*, December 1999
5. SLLA065, *A Comparison of LinBiCMOS and CMOS Process Technology in LVDS Integrated Circuits*, March 2000
6. SLLA082B, *Active Failsafe in TI's LVDS Receivers*, October 2001

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