Interfacing Different Logic With LVDS Receivers

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ABSTRACT

This application report provides explanations and design considerations for interfacing RS–422, differential current mode logic (CML), differential emitter coupled logic (ECL), and single-ended drivers with low-voltage differential signal (LVDS) receivers.

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1   Introduction

Some situations require interfacing different logic levels. One example is the use of devices with different I/Os. With so many different devices and interfaces in existence, it is difficult to avoid the requirement to interface to different logic levels. Another example is the use of 3.3-V devices to receive –5-V or 5-V logic levels. (see *LVDS Receivers Solve Problems in Non-LVDS Applications*, Analog Applications Journal, Data Transmission, February 2000). This second example is becoming more common as subsystems and peripheral devices move away from 5-V and –5-V parts to 3.3-V parts, but the need to interface to legacy devices still remains.

2   Single-Ended Logic

LVDS receivers compare incoming signals and determine if a logic state change has been made. One of the major benefits of receiving signals differentially is the canceling of the ground noise that is observed (equally) on both inputs. This differential receiver can also be used as a high-speed comparator. While this does not utilize the inherent ground noise immunity of LVDS, this allows a differential receiver to be interfaced with a single-ended driver.
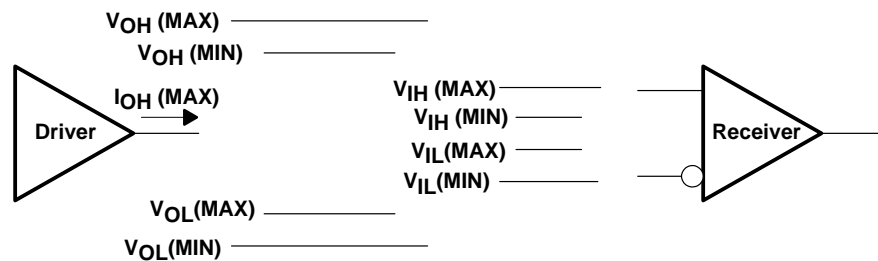

Figure 1. I/O Parameters

When interfacing a driver to a receiver, the parameters of the driver and the receiver define the structure of the interface. Figure 1 shows the I/O parameters that are considered in setting up an interface between a driver and a receiver. The first and most obvious question to answer is: are the output ranges of the driver within the input ranges of the receiver? With a standard TIA/EIA–644 receiver, the small voltage swings and differential voltage requirements are usually incompatible with non-LVDS drivers. Therefore, some type of resistor divider is required. The resistor divider must meet two requirements:

1. The resistance of the voltage divider must not cause the driver output current to exceed the specification for maximum output voltage.

2. The divider must divide the input voltage to a level that is acceptable to the receiver.
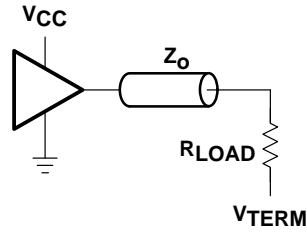
Figure 2. Equivalent Load

$$\frac{\left(V_{OH}(MAX) - V_{TERM}\right)}{R_L} \leq I_O(MAX) \tag{1}$$

Figure 2 and equation 1 are used to verify that the driver can drive the resistor divider. The Thevenin equivalent voltage (V_{TERM}) seen at the termination is usually 0 V (GND). Whether equation 1 can be satisfied with 0 V or another voltage level (for V_{TERM}) determines which resistor divider configuration to use in Figure 3. If a nonzero V_{TERM} is required, then equation 2 is used to solve for the resistor divider values:

$$V_{TERM} = V_{CC} \times \frac{(R2 + R3)}{(R1 + R2 + R3)} \tag{2}$$
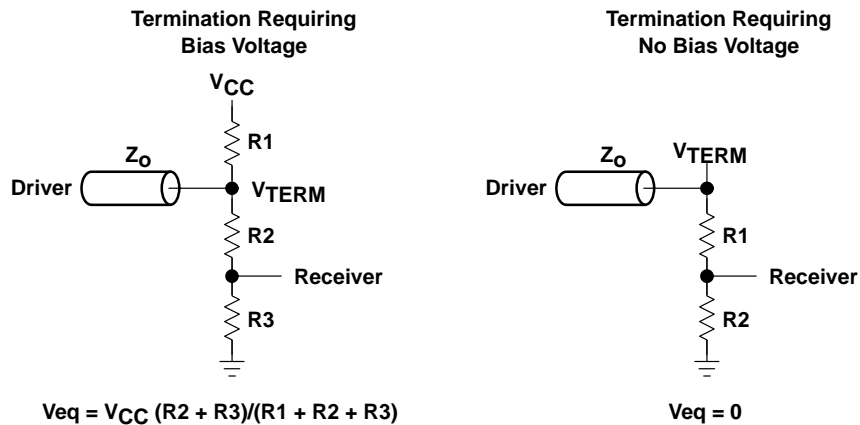

Figure 3. Resistor Divider Configurations

The gain provided by the resistor divider is defined by equations 3a and 3b:

a) $\quad GAIN = \dfrac{R3}{R2 + R3}$

b) $\quad GAIN = \dfrac{R2}{R1 + R2}$

$$\tag{3}$$

The desired gain is defined by the output requirements of the driver and the input requirements of the receiver. Assuming the input requirements for the receiver are taken from the TIA/EIA-644 standard, the magnitude of the differential input range is 100 mV to 600 mV. Since the voltage of the inverting input is going to be set to a constant value at the center of the noninverting voltage swing, the voltage swing of the noninverting input can range from 200 mV to 1200 mV. If the noninverting input has a voltage swing of 1200 mV centered about 600 mV and the inverting input is at a constant voltage of 600 mV, then the differential input voltage magnitude is 600 mV. The EIA–644 standard also specifies a valid input range of 0 V to 2.4 V; therefore, neither inverting nor noninverting input voltages can exceed this range. The following inequalities limit the values that can be selected for the gain based upon the TIA/EIA-644 input standard and the driver output levels (V_{OH} and V_{OL}). Once the value for the gain is established, equation 3b can be used to calculate the resistor values of R1 and R2, or equations 2 and 3a can be used to calculate R1, R2, and R3.

$$V_{OH}(Max) \times GAIN \leq 2.4 \text{ V}$$
$$V_{OL}(Min) \times GAIN \geq 0.0 \text{ V}$$
$$[V_{OH}(Max) - V_{OL}(Min)] \times GAIN \leq 1.2 \text{ V}$$
$$[V_{OH}(Min) - V_{OL}(Max)] \times GAIN \geq 0.2 \text{ V}$$

Another possible requirement for the resistor divider is impedance matching. Impedance matching is used when the media between the driver and the receiver acts like a transmission line. The media must be considered a transmission line when two times the propagation delay from the driver to the resistor divider is greater than one tenth of the rise time of the device ($2 \times t_{pd} > 0.1 t_r$). When this is true, then the equivalent impedance of the resistor divider (R_L of Figure 2) must also be equal to the characteristic impedance of the transmission line.

a) $R1 \parallel (R2 + R3) = Z_0$

(4)

b) $R1 + R2 = Z_0$

Regardless of the configuration chosen, the desired voltage at the inverting input (node B of Figure 4) is the center of the voltage swing at the noninverting input. This desired voltage is obtained with a simple resistor divider from a voltage source (V_{CC}). Equation 5 shows the relationship between the resistors at the inverting and noninverting inputs.

$$\frac{\left(V_{OH}(MAX) + V_{OL}(Min)\right) \times Gain}{2} = V_{CC} \times [R5/(R4 + R5)]$$

(5)

Figure 4 shows a single-ended driver interfacing a Texas Instruments (TI) LVDS repeater through a resistor network. The purpose of implementing the single-ended to LVDS interface is to allow the LVDS to distribute the signal and not the originating single-ended logic level.
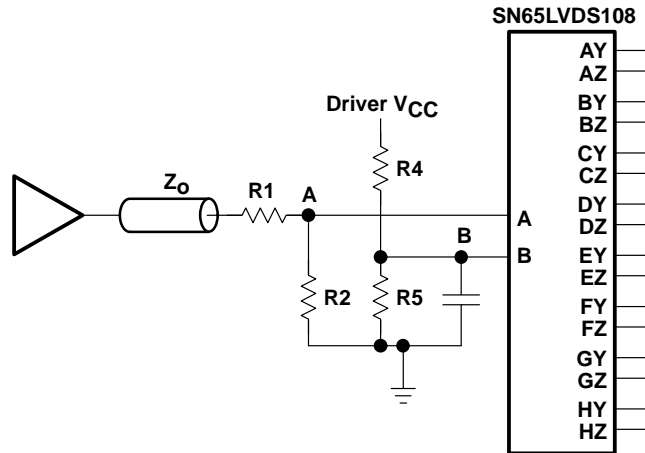
SN65LVDS108

Figure 4. Single-Ended Driver to LVDS Receiver

The resistor values in Figure 4 do not need to satisfy equation 4b (impedance matching), since the transmission line length from the driver to the resistor R1 is assumed to be electrically small. This means that R1 and R2 are only dependent on equation 3b (gain). Table 1 shows the output parameters of a 5-V driver.

Table 1. Example of Single-Ended Driver Outputs

DRIVER	I_O(MAX)	V_{OH} (Max)	V_{OH} (Min)	V_{OL}(Max)	V_{OL}(Min)
5-V (CMOS)	9 mA	5.5 V	0.7 V_{CC}	0.3 V_{CC}	0.0 V

Using the values in Table 1 and the input specifications of the SN65LVDS108, the following bounds can be applied to the gain.

$0.1 \leq$ Gain ≤ 0.66

Table 2. Example of Single-Ended Resistor Values

DRIVER TYPE	GAIN	R1 (Ω)	R2 (Ω)	R4 (Ω)	R5 (Ω)
5-V (CMOS)	0.5	680	560	10 k	6.2 k

Table 2 shows values for R1, R2, R4, and R5 for a gain of 0.5. Since equation 4b does not apply, the actual values can be varied as long as the proper relationship between the resistors is maintained. When impedance matching is required, R1 and R2 are not as flexible. Impedance matching becomes more of an issue in differential systems, since communication over longer distances and with faster edge rates (rise and fall times) is more common.

3   Differential Logic

The equations and resistor dividers used for single-ended logic can also be applied to differential interfaces. Now that both inputs of the receiver use the same termination scheme, the benefit of receiving signals differentially is utilized by the interface.

3.1   ECL to Standard LVDS

When talking about ECL devices, including negative ECL (NECL), positive ECL (PECL), and low-voltage 3.3 V PECL (LVPECL), the load seen by the driver is usually 50 Ω biased to 2 Vdc below the device (driver's) V_{CC}. The termination is due to the nature of the driver (emitter follower). The termination load and voltage are depicted in Figure 5.
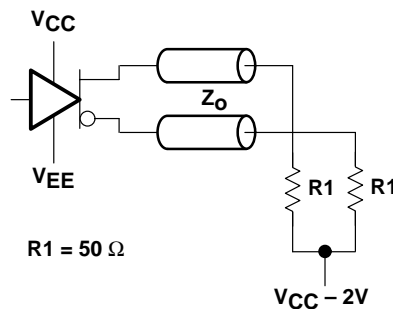

Figure 5.   ECL Termination

Often, the bias voltage level for the characteristic load is not available and is attained through a Thevenin equivalent circuit (resistor divider as shown in Figure 3). Figure 6 is a Thevenin equivalent circuit intended to provide the characteristic load and to translate the ECL output levels at Va and $\overline{Va}$ to the LVDS level desired at Vb and $\overline{Vb}$.

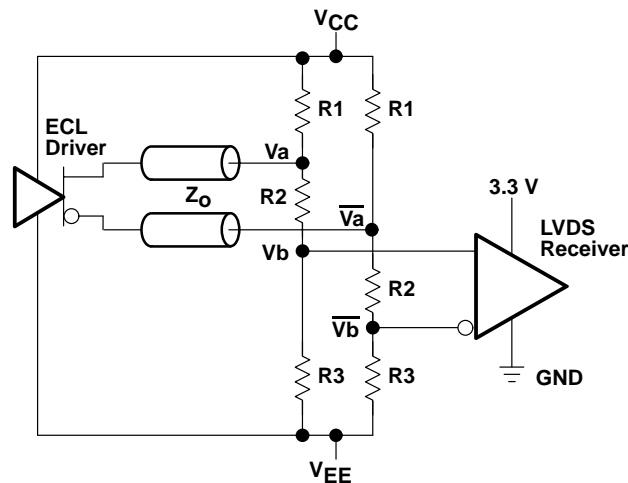**Figure 6.   Differential ECL Interface to Standard LVDS**

Since a bias termination is used with ECL, the biased structure in Figure 3 is used and equations 2, 3a, and 4a are applied. The input requirements are assumed to be TIA/EIA–644 (the doubling effect of using the receiver as a comparator does not apply). The minimum and maximum levels for LVPECL, PECL, and NECL devices are given in Table 3.

Table 3. LVPECL, PECL, and NECL Outputs

	LVPECL	PECL	NECL
V$_{OH}$ (Max)	2.42 V	4.120 V	−0.880 V
V$_{OH}$ (Min)	2.275 V	3.975 V	−1.025 V
V$_{OL}$ (Max)	1.68 V	3.380 V	−1.620 V
V$_{OL}$ (Min)	1.49 V	3.190 V	−1.810 V
I$_O$ (Max)	50 mA (continuous)	50 mA (continuous)	50 mA (continuous)

The gain of LVPECL and PECL can be bound to the following values:

LVPECL $\equiv 0.168 \leq$ GAIN ≤ 0.645

PECL $\equiv 0.168 \leq$ GAIN ≤ 0.583

The calculated resistor values are rounded to the standard values given in Table 4.

Table 4. Standard Resistor Values

DRIVER	V$_{CC}$ (V)	V$_{EE}$ (V)	R1:R2:R3 (Ω)
LVPECL	3.3	GND	127: 33: 51
PECL	5.0	GND	82: 75: 51

Calculating gain for the NECL case reveals that there is no possible value of gain that can be applied to the outputs to produce TIA/EIA–644 inputs. There is no gain value that minimizes the voltage swing to within the TIA/EIA–644 standard and moves the offset of the signal from negative voltage to within the positive range of the standard. Most LVDS receivers require some type of capacitive coupling to adjust the common-mode voltage seen at the receiver inputs after the resistor divider has adjusted the voltage swing of the NECL outputs. The diagram in Figure 7 is an example. Resistors R1, R2, R3, and R4 provide the Thevenin equivalent voltage and the resistance seen by the driver. The R5 and R6 resistors divide the 3.3 V in order to create the bias voltage for the LVDS receiver.
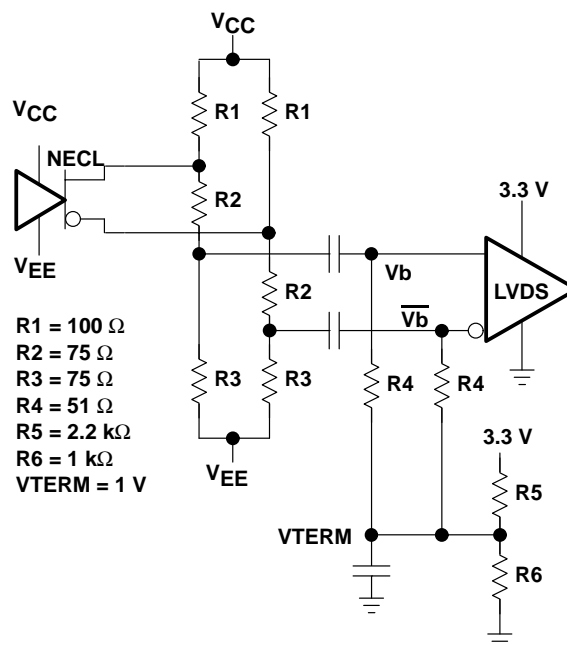

Figure 7. NECL to LVDS With Capacitive Coupling

The resistor values for Figure 7 must satisfy the following equations:

$$50 = (R1 \| (R2 + R3 \| R4)) \tag{6}$$

$$\frac{\left(V_{CC} - 2 - V_{EE}\right)}{\left(V_{CC} - V_{EE}\right)} = \frac{(R2)}{(R1 + R2)} \tag{7}$$

$$Gain = \frac{R3}{R2 + R3} \tag{8}$$

$$Vterm = (3.3 \ V) \times \frac{R5}{R4 + R5} \tag{9}$$

Besides the obvious disadvantage of increasing the parts count, capacitive coupling also introduces intersymbol interference (ISI) when dealing with non-dc balanced transmissions. An alternative to this coupling is the use of receivers that accept a wide range of common-mode inputs, eliminating ISI problems and minimizing the number of parts required to interface various types of ECL to LVDS.

3.2 ECL to the SN65LVDS33/34

The SN65LVDS33/34 dual/quad receiver provides a wide common-mode capability and a maximum differential input voltage magnitude which exceed the TIA/EIA–644 specifications. The valid input range is increased to –4 V to 5 V and the differential input magnitude can vary from 100 mV to 3 V. These extended ranges provide wider bounds for the gain.

$V_{OH}(Max) \times GAIN \leq 5 \ V$

$[V_{OL}(Min) \times GAIN \geq -4.0 \ V$

$[V_{OH}(Max) - V_{OL}(Min)] \times GAIN \leq 3.0 \ V$

$[V_{OH}(Min) - V_{OL}(Max)] \times GAIN \geq 0.1 \ V$

The LVPECL, PECL, and ECL to SN65LVDS33/34 gain is limited to the following values:

$LVPECL \equiv 0.168 \leq GAIN \leq 2.07$

$PECL \equiv 0.168 \leq GAIN \leq 1.21$

$NECL \equiv 0.168 \leq GAIN \leq 2.21$

With the SN65LVDS33/34, the bounds for LVPECL, PECL, and NECL gain all include unity gain (GAIN=1). Choosing a gain value of one eliminates the need for the R2 resistor found in Figure 6 and simplifies the circuit to that shown in Figure 8.
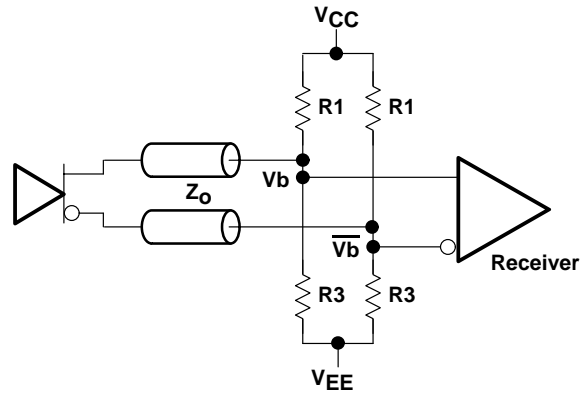
Figure 8. ECL to SN65LVDS33/34

Elimination of the R2 resistors also reduces the complexity of equations 2 and 4a. The resistor values are shown in Table 5. The eye patterns of the SN65LVDS33/34 output with the LVPECL and NECL drivers are shown in Figures 9 and 10, respectively.

Table 5. Standard Resistor Values for PECL and LVPECL to SN65LVDS33/34 Translation

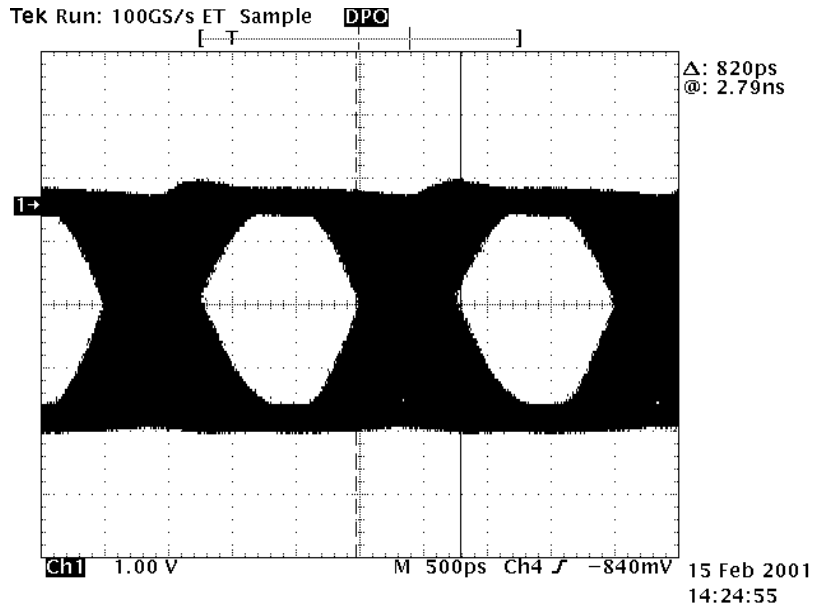| DRIVER	V_{CC} (V)	V_{EE} (V)	R1:R3 (Ω)
LVPECL	3.3	GND	125: 82.5
PECL	5.0	GND	82.5: 125
NECL	GND	−5.0	82.5: 125

Figure 9. LVPECL to SN65LVDS33/34 at 500 Mbps; Receiver Output (CH1)
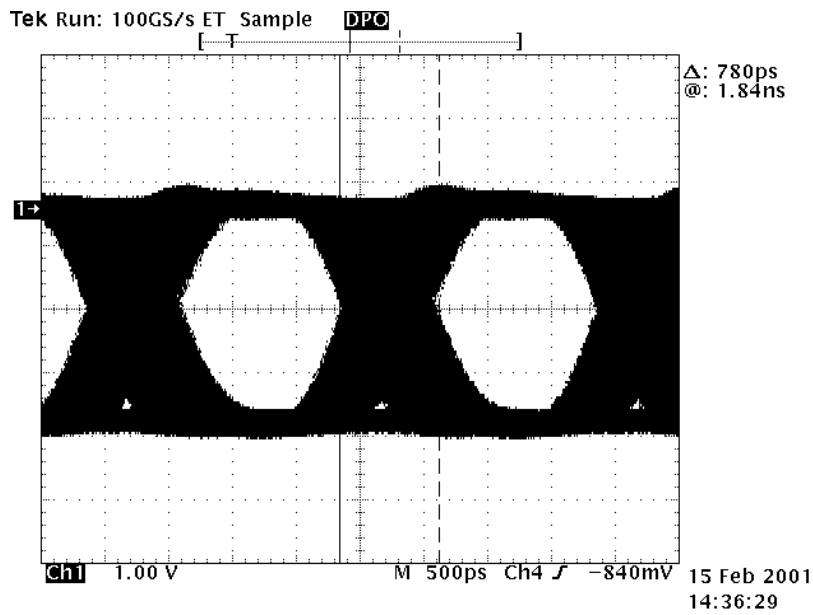

Figure 10. NECL to SN65LVDS33/34 at 500 Mbps; Receiver Output (CH1)

3.3   ECL Receipt by a 3.3-V Remote System

The previous example assumes that the driver voltage supplies are available for the termination network and the only common-mode voltage is the ECL offset voltage. Another consideration is when only the 3.3-V supply for the LVDS receiver is available and ground noise exists between the ground planes of the receiver and the driver.

The idea of receivers accepting inputs from devices with a different V_{CC} is becoming more popular as designers move to incorporate low voltage devices, such as LVDS receivers, in remote systems. This movement to incorporate low voltage devices poses two problems for the resistor networks previously discussed. First, the +5 and −5 voltages for the PECL and NECL networks are simply not available. The only voltage supply available is the 3.3 V required by the LVDS receiver. In the case of LVPECL, where the V_{CC} is the same for both the driver and receiver, a second problem is seen: potential differences between grounds. With a ground potential difference between the receiver and the driver, the driver does not see the V_{CC}−2 characteristic load voltage required.

The ground noise problem is alleviated by the wide common-mode capabilities of the SN65LVDS33/34. The solution to the unavailability of voltages is an ac termination. Figures 11 and 12 depict the use of the SN65LVDS33/34 when the driver and receiver have different ground potentials and are separated by about five meters of CAT–5 cable. Figure 13 shows an eye pattern for the NECL to LVDS configuration. Table 6 shows that the SN65LVDS33/34 can tolerate a ground noise magnitude of 2.6 V for LVPECL, 1.1 V for PECL, and 2.3 V for NECL.

As mentioned earlier, the SN65LVDS33/34 receiver exceeds the TIA/EIA−644 requirement and a resistor divider is not necessary. With no resistor divider, R1 in Figures 11 and 12 simply needs to match the characteristic load impedance of 50 Ω. R3 provides a resistor path to ground for the ECL driver. When designing with a preexisting source termination, the important parameter is the output voltage. If the voltage levels exceed the inputs of the receiver, then a resistor divider is required at the receiver. The R2 resistor is a small value and is intended to minimize any possible common-mode current reflections.
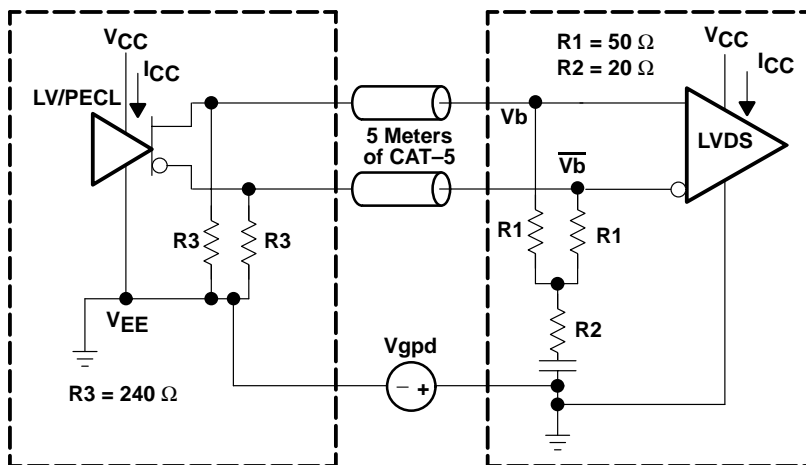

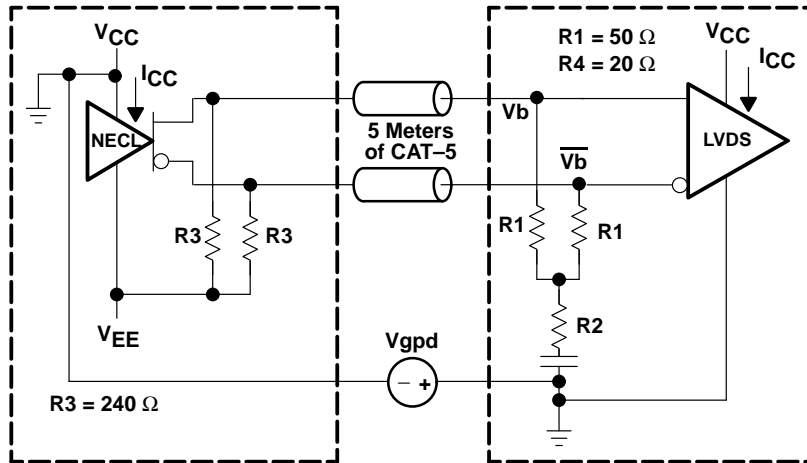**Figure 11. LVPECL and PECL to Remote SN65LVDS33/34**

Figure 12. NECL to Remote SN65LVDS33/34

Table 6. LVDS Inputs With Respect to Receiver Ground

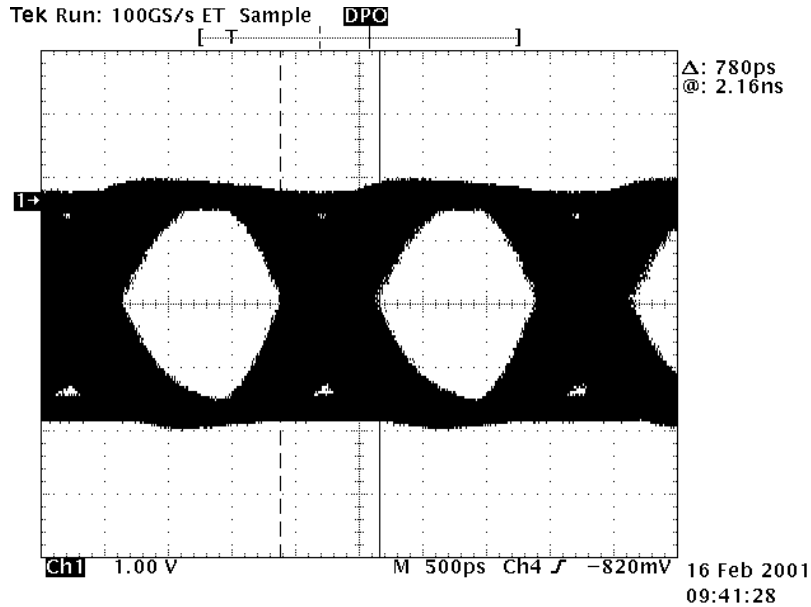| DEVICE DRIV-ER	GROUND POTENTIAL DIFFERENCE (Vgpd)	Vb HIGH (V)	Vb LOW (V)
LVPECL	–2.64 V	5.0	4.24
LVPECL	0 V	2.36	1.60
LVPECL	5.60 V	–3.24	–4.0
PECL	–1.12 V	5.0	4.50
PECL	0 V	3.88	3.38
PECL	7.38	–3.5	–4.0
NECL	–5.87 V	5.0	4.17
NECL	0.0 V	–0.87	–1.70
NECL	2.3 V	–3.17	–4.0

Figure 13. NECL to Remote SN65LVDS33/34 at 500 Mbps; Receiver Output (CH1)

Designers are progressing towards low voltage signaling such as LVDS. The TI LVDS wide common-mode receivers allow designers to easily bring PECL and NECL into 3.3-V designs without having to supply 5-V or –5-V.

3.4 CML to Standard LVDS

ECL devices are generally referred to as current mode logic (CML) devices. The main differences between ECL and CML, from an external point of view, are the bias termination (which CML does not require) and the voltage swing. ECL typically has a voltage swing of about 800 mV, while the CML voltage swing is about half that value. At 400 mV, the voltage swing of CML is well within the EIA–644 specification of 100 mV to 600 mV differential voltage range. Unfortunately, the actual voltage levels of 5 V CML are beyond the 2.4 V specified in the LVDS standard. Also, the voltage swing is relatively small and voltage division can create a differential voltage below the 100 mV minimum input differential voltage. As in the case of NECL to standard LVDS, the only alternative is the use of ac coupling. Figure 14 shows an example of an LVDS receiver receiving a CML signal using ac coupling.
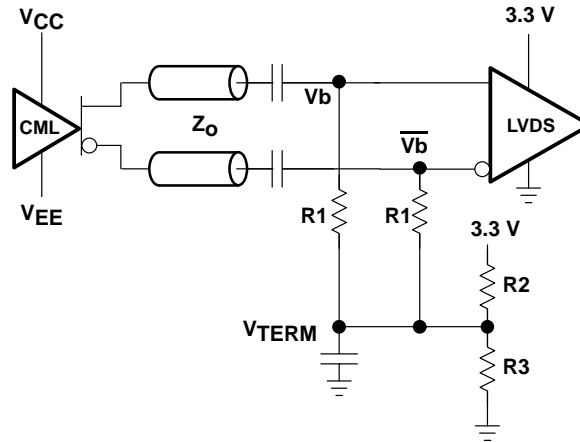
Figure 14. CML to Standard LVDS

The R1 resistors match the characteristic impedance of the transmission line (with a short distance, R1 must have a minimum resistance to limit output current). The termination voltage (Vterm) for biasing the coupling capacitors provides inputs that are within the LVDS standard. In Figure 14, the resistor values of R1, R2, and R3 are 50 Ω, 2200 Ω, and 1000 Ω, respectively. Therefore, with an output swing of 400 mV from the +5 V CML driver, both inputs at the receiver are a 400 mV voltage swing about 1 V.

3.5 CML to SN65LVDS33/34

As mentioned before with ECL, ac coupling has its shortfalls, especially when dealing with non-dc balanced data. A more robust solution is the use of wide common-mode devices. With a wide common-mode device, the coupling capacitors to level shift the driver outputs and the voltage divider (3.3V, R1, R2) are not required, simplifying the circuit to that of Figure 15.
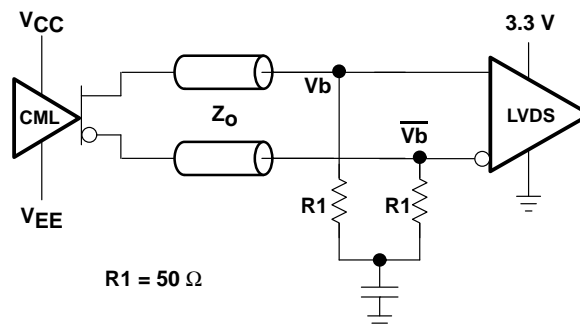

Figure 15. CML to SN65LVDS33/34

3.6   422 to SN65LVDS33/34

Another common differential logic level is RS–422 (422). 422, like ECL, uses larger voltage swings than LVDS. 422 differs from ECL in that 422 is much slower and the 422 driver termination does not require a bias termination. As in the ECL examples, the TI wide common-mode receivers can receive 422 signals without the need for a 5-V supply, and also provide some immunity to ground noise.

For the 422 device chosen and the resistor load in Figure 16, the common-mode output level can be a maximum value of 3 V, and the differential output magnitude can range from 2 V to 5 V. Since the differential output magnitude can exceed the 3-V range of the receiver, the interface network is a resistor divider. Figure 16 shows the configuration of the resistor divider for the 422 to LVDS translation.
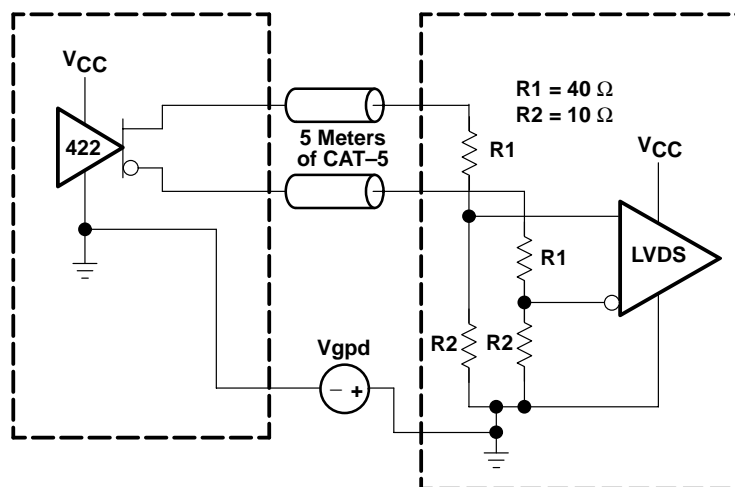

Figure 16.   422 to LVDS

Equations 3b and 4b are used to calculate the values of resistors R1 and R2. The range of possible gain values is:

$$0.05 \leq \text{GAIN} \leq 0.6$$

With a Z_0 of 50 Ω and a gain of 0.2, resistors R1 and R2 are 39 Ω and 10 Ω, respectively. Just as in the +5 V PECL to standard LVDS case, a +3.3 V LVDS receiver can be used to interface a +5 V 422 driver.

The significance of the wide common-mode device is great. The common-mode device satisfies the output extremes of NECL, PECL, and CML, without excessive component addition. This gives designers flexibility to replace a legacy receiver with a wide-common mode LVDS part and still maintain operation. The designer can later replace the driver with an LVDS driver; reusing both the transmission line and the bias network as a termination network for the now LVDS circuit. (The resistor values for the interface circuits provide a differential equivalent termination of 100 Ω.)

4   Conclusion

Interfacing other logic levels to LVDS is simplified with the use of wide common-mode devices from TI, such as the SN65LVDS33/34. These wide common-mode LVDS devices enable designers to incorporate LVDS receivers with other logic devices and begin the transition from older logic devices to LVDS with greater ease and less cost than with standard TIA/EIA–644 LVDS receivers.

5   References

1. *LVDS Receivers Solve Problems in Non-LVDS Applications*, Analog Applications Journal, Data Transmission, February 2000
2. *Using an LVDS Receiver With RS–422 Data*, TI literature number SLLA031
3. *Electrical Characteristics of Low Voltage Differential (LVDS) Interface Circuits*, TIA/EIA–644

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