EVM User's Guide: TRF-LSC-AFE7950EVM

TRF-LSC-AFE7950 Evaluation Module

Description

The TRF-LSC-AFE7950EVM evaluation module is used to evaluate the performance of TI's AFE79xx family of integrated RF sampling transceivers with TI's TRF1208 single-ended-to-differential amplifier on RX, and TRF1108 differential-to-single-ended amplifier on TX. The AFE79xx devices support up to four transmit, four receive, and two feedback channels (4T4R2F) and integrates a phase-locked loop (PLL) and voltage-controlled oscillator (VCO) for generating data-converter clocks. The AFE79xx integrates eight JESD204B- and JESD204C-compatible serializer or deserializer (SerDes) transceivers. These transceivers are capable of running up to 29.5Gbps to transmit and receive digital data through the onboard FPGA mezzanine card (FMC) connector.

The EVM includes the LMK04828 clock generator to provide reference clocks and SYSREF to the analog front end (AFE) and capture card (field-programmable gate array, FPGA). The evaluation module (EVM) uses a single 5.5V input and includes complete power-management circuitry. External clocking options include support for feeding the reference clock (for the on-chip PLL). The design interfaces with the TI pattern and capture card solution (TSW14J56EVM or TSW14J57EVM), as well as many FPGA development kits.

Get Started

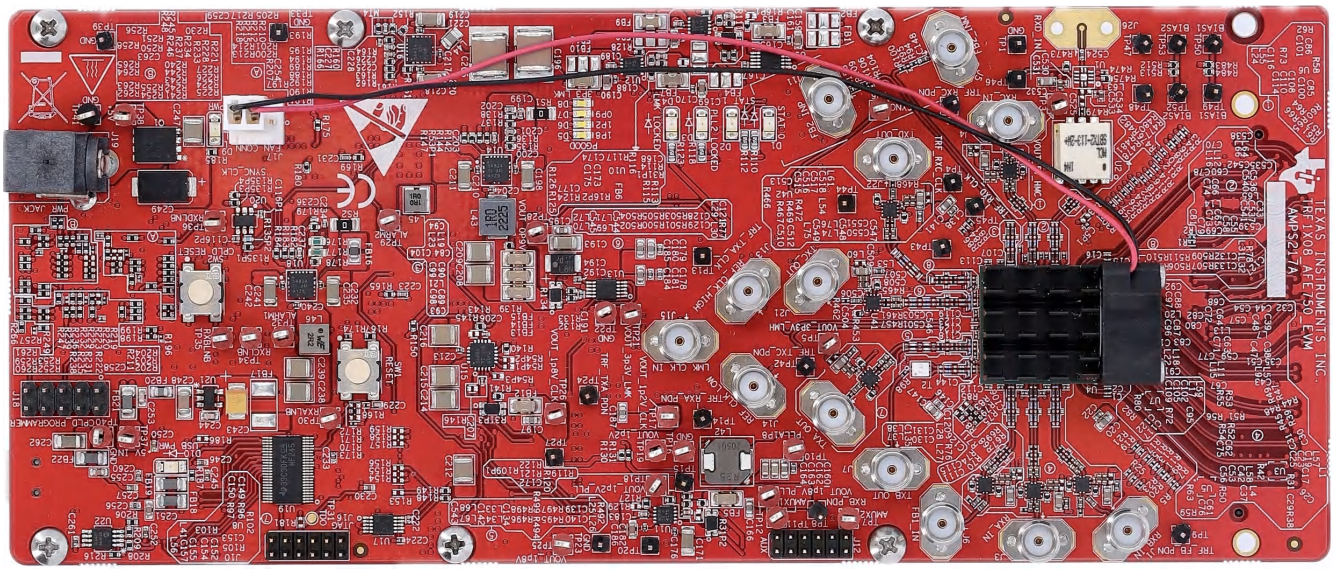
1. Order the TRF-LSC-AFE7950EVM
2. Order TSW14J56EVM OR TSW14J57EVM
3. Download the latest software and libraries.
4. Download the comprehensive reference design files.
5. For latest info please refer to AFE79XX-HSC-DESIGN folder.

Features

- Operates on single 5.5V supply
- Includes onboard clock generation
- RF front end with > 8GHz S2D and D2S amplifiers

Applications

- Seeker front end
- Radar
- Defense radio
- Tactical communications infrastructure
- Wireless communications test



TRF-LSC-AFE7950EVM Board

1 Evaluation Module Overview

The TRF-LSC-AFE7950EVM includes a clocking and power solution, and runs on a single 5.5V supply. Figure 1-1 shows that the RF inputs and outputs using SMA connectors are on the top side of the EVM. Use a 10MHz reference clock through the SMA J15 (LMK_CLKIN) connector to lock the onboard voltage-controlled crystal oscillator (VCXO) with the LMK04828. Typically, lab equipment has a 10MHz oscillator output to synchronize multiple lab systems. The onboard LMK04828 accepts the 10MHz clock from the external lab equipment to maintain synchronization and coherency of the data capture and generation to the TRF-LSC-AFE7950EVM.

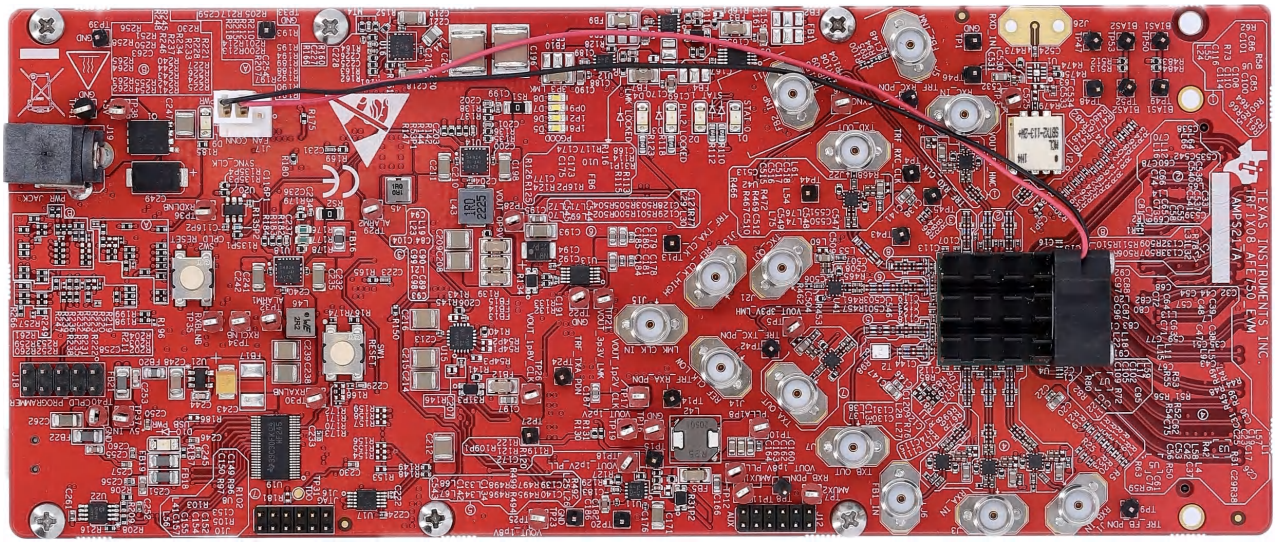


Figure 1-1. TRF-LSC-AFE7950EVM Top View

To feed an external reference clock to lock the PLLs in the AFE79xx, use SMA J13 (REF_CLK_HIGH) or SMA J14 (REF_CLK_LOW). The USB connector and the 5.5V connector are on the right side of the board.

Figure 1-2 shows the bottom view of the TRF-LSC-AFE7950EVM.

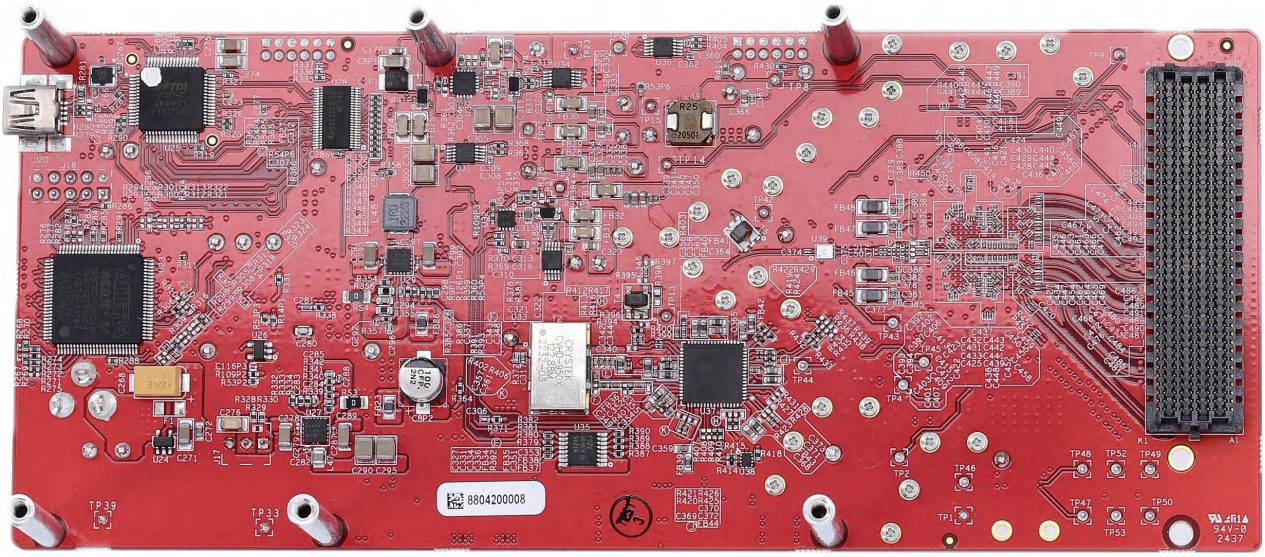


Figure 1-2. TRF-LSC-AFE7950EVM Bottom View

The capture card used with the TRF-LSC-AFE7950EVM is typically the TSW14J56EVM or TSW14J57EVM. The TSW14J56EVM supports a SerDes speed up to 12.5Gbps and the TSW14J57EVM supports up to 15Gbps. The choice between the TSW14J56EVM or TSW14J57EVM depends on the AFE79xx JESD204 configuration and the associated SerDes rate.

1.1 Introduction

The TRF-LSC-AFE7950EVM evaluation module support up to four transmit, four receive, and two feedback channels (4T4R2F) tuned to various frequencies in the L, S, and C bands.

CAUTION

Hot surface. Contact can cause burns. Do not touch.

WARNING

Moving parts. Do not touch the spinning disk or motor during operation.

1.2 Kit Contents

The package includes:

- TRF-LSC-AFE7950EVM
- USB Type Mini-B cable
- Power cable

The package does not include:

The TSW14J56EVM or TSW14J57EVM capture card used in this document is not included in this kit. Order this capture card from https://www.ti.com/tool/TSW14J57EVM.

1.3 Specification

Figure 1-3 shows the signal chain of the board.

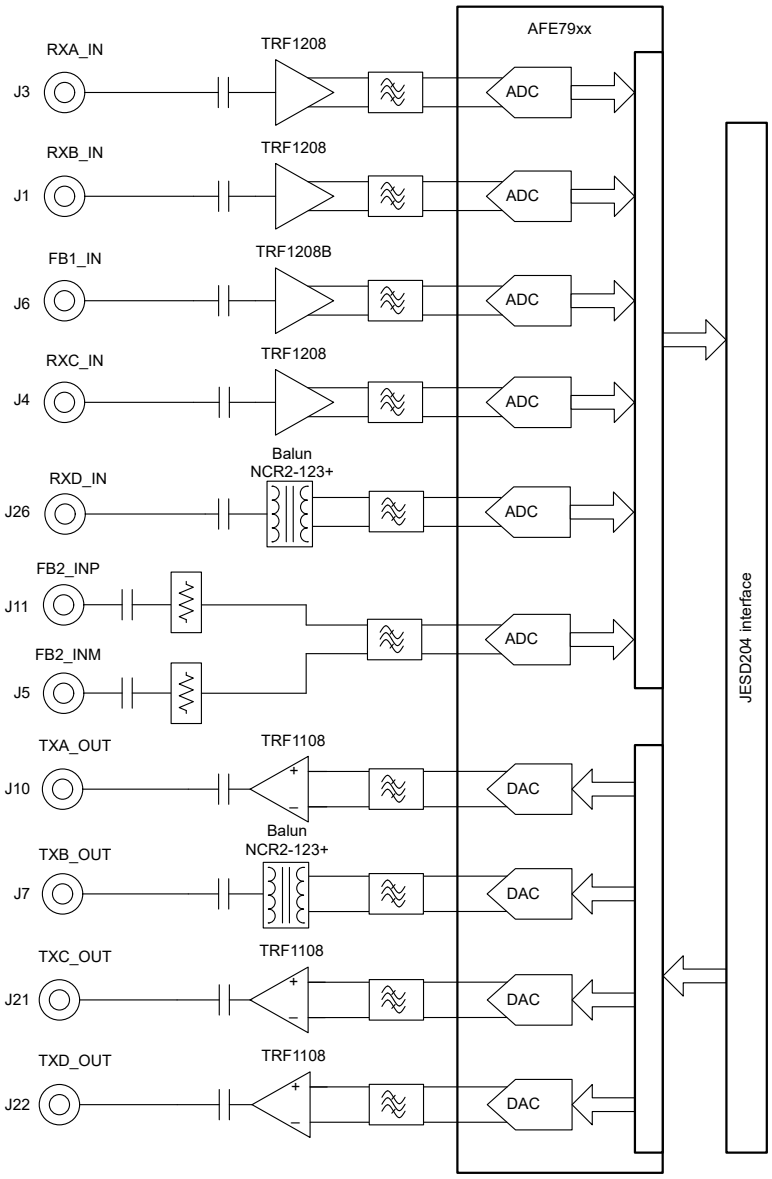


Figure 1-3. TRF-LSC-AFE7950EVM Block Diagram

1.4 Device Information

The AFE7950 is a high-performance, wide-bandwidth multichannel transceiver, integrating four RF sampling transmitter chains, four RF sampling receiver chains, and two RF sampling feedback chains (six RF sampling ADCs total). With operation up to 12GHz, this device enables direct RF sampling in the L-, S-, C-, and X-band frequency ranges without the need for additional frequency conversions stages.

The TRF1208 device is a fully differential amplifier that drives the ADC of receive paths (in S2D configuration). The TRF1108 device is a differential-to-single-ended (D2S) RF amplifier driven by the DAC of the transmit path.

The LMK0482x family is an ultra-low-noise, JESD204B-compliant clock-jitter cleaner with integrated VCO.

2 Hardware

2.1 Power Requirements

Follow these steps to set up the power supply:

1. Connect 5.5V power supply to the power jack (PWR_JACK) connector (J19) of the TRF-LSC-AFE7950EVM.
2. Check that the D9 (PWR) LED light is on. The power supply draws approximately 550mA to 650mA.
3. Connect a USB type mini-B cable from the PC to the USB port (J20) of the TRF-LSC-AFE7950EVM.
4. Check that the D10 (USB_PWR) LED light is on. The LED light strength depends on the USB cable length. If the LED light is not on, then use a shorter USB cable. TI tested a three-foot USB cable in this setup.
5. The power-supply sequencer on the TRF-LSC-AFE7950EVM has a power status for each rail. If the power good (PGOOD) is logic high, then the corresponding power supply rail is powered correctly. The respective LED lights is on. Check that the following LEDs lights are on.
   - D5 (1P8) LED
   - D6 (1P2) LED
   - D7 (0p9) LED
   - D8 (3p3_LMK) LED

2.2 Setup

RF test setup requires RF signal generators, spectrum analyzer, attenuator pads, power combiners, cables, and so forth. Use the appropriate setup based on the type of test. The TRF1208 Evaluation Module user's guide shows examples of the RF test setup.

2.3 Interfaces

Follow these steps to connect the TRF-LSC-AFE7950EVM and TSW14J56EVM:

1. Connect FMC connector U40 of TRF-LSC-AFE7950EVM to FMC connector J4 of TSW14J56EVM.
2. With the power supply in power-down mode, connect a 5.5V, 4A maximum power supply to the J11 *+5 V IN* connector of the TSW14J56EVM.
3. Connect a USB 3.0 cable from the PC to the J9 connector of the TSW14J56EVM.
4. With the power supply in power-down mode, connect a 5.5V, 5A maximum power supply to the J19 *CONN JACK PWR* connector of the TRF-LSC-AFE7950EVM.
5. Connect a USB 2.0 cable from the PC to the J20 connector of the TRF-LSC-AFE7950EVM.
6. Optionally, connect the 10MHz lab equipment reference to the J15 (LMK_CLK_IN) connector.

3 Software

The high-speed data converter pro software (DATACONVERTERPRO-SW) controls the TSW14J5x. In this user's guide, DATACONVERTERPRO-SW is called HSDC PRO, and the two terms are interchangeable. Download version 5.0 or greater from www.ti.com/tool/dataconverterpro-sw.

The Latte software configures the TRF-LSC-AFE7950EVM. The latest version of Latte is available for download from TI's MySecure website. Request the software after signing in to myTI on the log-in page. The installer file is named *AFE79xx_EVM_GUI_vxxxxxx*, where *xxxxxx* is the version number.

3.1 Software Installation

1. Install the HSDC PRO software. Follow all the instructions within the installer execution process.
   - The default HSDC PRO software path is:
     C:\Program Files (x86)\Texas Instruments\High Speed Data Converter Pro
2. Install AFE79xxEVM_GUIvxxxxx.exe. Follow all the instructions within the installer execution process shown in Figure 3-1. The following applications are installed:
   - Latte 5.x.x
   - AFE79xx Latte Library Vx.xx
     - Both the base Latte software and the AFE79xx Latte library update as needed throughout the product development process.
   - National Instruments LabVIEW™ Runtime Engine 2014
   - Associated HSDC PRO .ini files required for the TRF-LSC-AFE7950EVM.

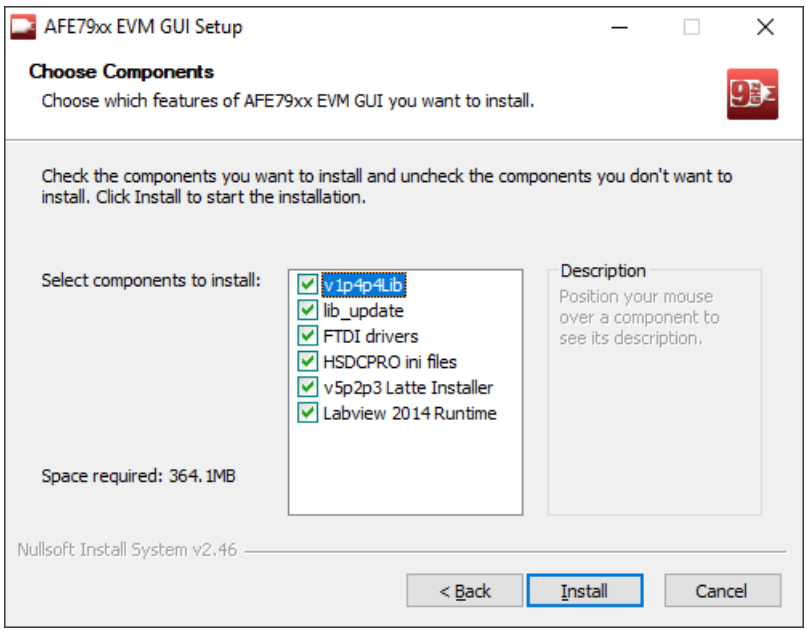


Figure 3-1. Latte Installer Options

3. The default Latte software directory installs at *C:\Users\User ID\Documents\Texas Instruments\Latte*. Replace *User ID* with the proper Windows® log-in ID.

3.2 Software Description

3.2.1 HSDC Pro Overview

For information on HSDC Pro software use, download the *High-Speed Data Converter Pro GUI User's Guide*.

3.2.2 Latte Overview

Launch the Latte GUI from the desktop shortcut or from *All Programs* > *Texas Instruments*. Figure 3-2 shows the Latte GUI.

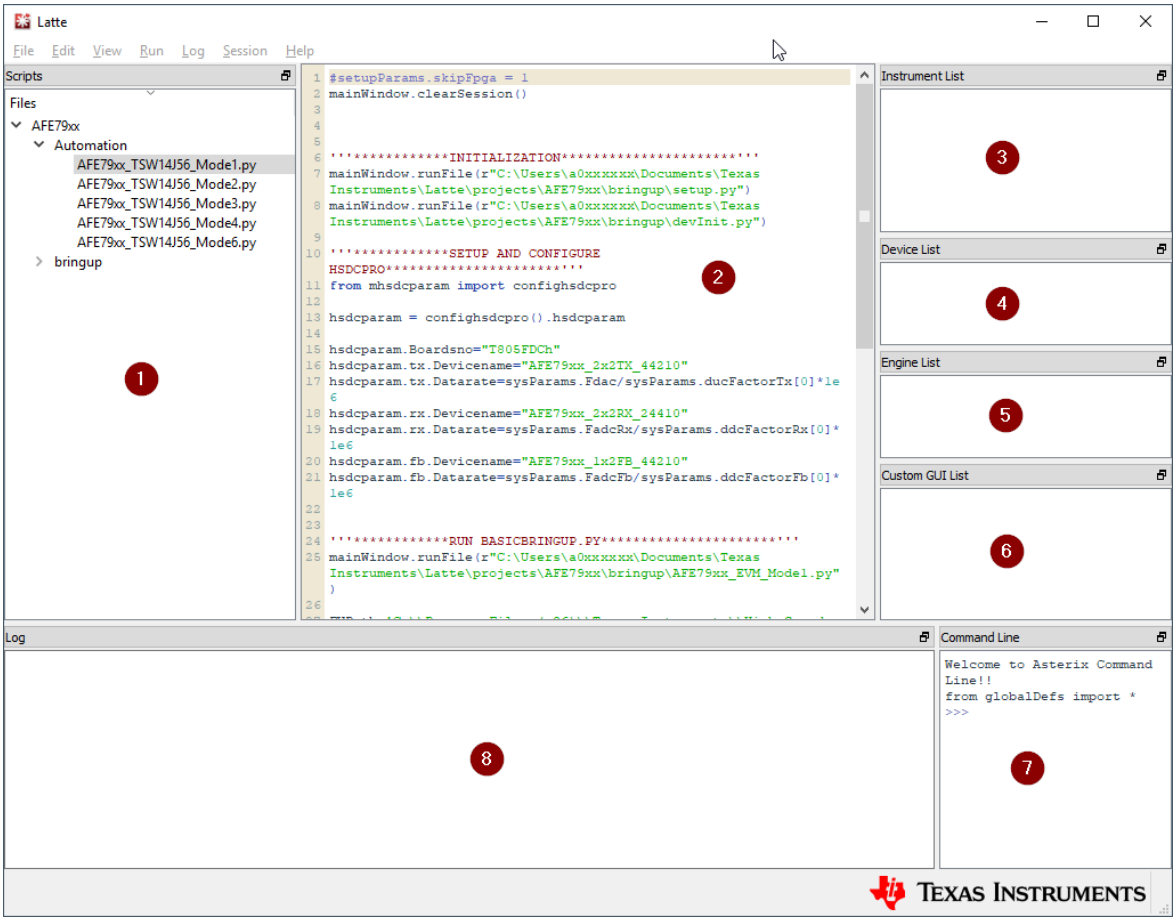


Figure 3-2. Latte GUI

Figure 3-2 shows how the Latte GUI is split into eight windows (labeled 1 to 8) with the following functionality:

- **Window 1:** This window (also called *Scripts*) shows the list of python scripts available that generate the register commands to configure the TRF-LSC-AFE7950EVM. The script files are located in the *..\Documents\Texas Instruments\Latte\projects\AFE79xx\bring-up* folder. Modify and create new scripts as necessary, which appear in this subwindow when Latte is restarted.
- **Window 2:** This window (also called *Editor*) shows the code in the script currently selected and is used to modify and save the code as necessary.
- **Windows 3 to 6:** These windows are updated as the scripts run to configure the TRF-LSC-AFE7950EVM, and are mostly informational.
- **Window 7:** This window (also called *Command Line*) is used to enter and run individual commands. Examples of such commands include changing TX, RX, FBRX DSA, NCOs, and so forth.
- **Window 8:** This window (also called *Log*) displays messages during execution of scripts to display the current status. This window is also used for troubleshooting.

3.2.2.1 Latte Shortcuts

Run Script file:To run a script file, first select the file in the *Scripts* window, and then press F5 (or select *Run* and then *Buffer* in the menu bar).

Run part of script: To run part of a script file, select the lines in the *Editor* window, and then press F7 (or select *Run* and then *Run Selection* in the menu bar).

Stop Execution: To stop the current execution, press F10 (or select *Run* and then *Stop* in the menu bar).

Clear Session: To clear the current session and reset the Latte GUI to the initial state, press Ctrl+T (or select *Session* and then *Clear Session* in the menu bar). This process is equivalent to a restart and is used to restart a session without closing the GUI.

4 Implementation Results

4.1 Evaluation Setup TRF-LSC-AFE7950EVM Automatic Configuration

This section guides the user through the sequence of steps to automatically bring up the TRF-LSC-AFE7950EVM through the automation python routine. The example used in this section is the default TRF-LSC-AFE7950EVM Mode 1. Table 4-1 lists the default Mode 1 configuration overview.

Table 4-1. TRF-LSC-AFE7950EVM Mode 1 Configuration Overview

Mode	Default Programming
TX (transmitter)	4 TXDACs are enabled, DSA = 0, LMFSHd_2TX = 44210, 6 × interpolation, 491.52MSPS data rate
RX (receiver)	4 RXADCs are enabled, DSA = 0, LMFSHd_2RX = 24410, 12 × decimation, 245.76MSPS data rate
FBRX (feedback receiver)	Two FBADCs are enabled, DSA = 0, LMFSHd_1FB = 22210, 6 × decimation, 491.52MSPS data rate
SerDes	Eight lanes running at 9830.4Mbps
Data converter clock rates	F_{RXADC} = 2949.12MSPS, F_{FBADC} = 2949.12MSPS, F_{TXDAC} = 8847.36MSPS
Status	RX AGC is disabled, RX, TX DSA step impairments are uncorrected, DAC in interleaved mode

Table 4-2, Table 4-3, and Table 4-4 list the TSW14J5x .ini files used to evaluate the RXADC, FBADC, and the TXDAC portions of the AFE79xx. The tables also list the associated channel mapping with respect to the TRF-LSC-AFE7950EVM.

Table 4-2. RXADC TSW14J56EVM / TSW14J57EVM INI Mapping (AFE79xx_2x2RX_24410)

ADC Channel Number in HSDC PRO ADC Panel(1)	TRF-LSC-AFE7950EVM Connector	Associated AFE79xx Input
1,2	J3, RXA_IN	1RX
3,4	J1, RXB_IN	2RX
5,6	J4, RXC_IN	3RX
7,8	J26, RXD_IN	4RX

(1) For complex quadrature output (I/Q) of the RXADC, the odd number is the real channel, while the even number is the imaginary channel.

Table 4-3. FBADC TW14J5x INI Mapping (AFE79xx_1x2FB_44210)

ADC Channel Number in HSDC PRO ADC Panel(1)	TRF-LSC-AFE7950EVM Connector	Associated AFE79xx Input
1,2	J6, FB1_IN	1FB
3,4	J5 and J11, FB2_IN	2FB

(1) For complex quadrature output (I/Q) of the FBADC, the odd number is the real channel, while the even number is the imaginary channel.

Table 4-4. TXDAC TSW14J5x INI Mapping (AFE79xx_2x2TX_44210)

DAC Channel Number in HSDC PRO DAC Panel(1)	AFE79xx EVM Connector	Associated AFE79xx Input
1,2	J10, TXA_OUT	1TX
3,4	J7, TXB_OUT	2TX
5,6	J21, TXC_OUT	3TX
7,8	J22, TXD_OUT	4TX

(1) For complex quadrature output (I/Q) of the TXDAC, the odd number is the real channel, while the even number is the imaginary channel.

4.1.1 Recommended Test Environment

The recommended test environment for the TRF-LSC-AFE7950EVM is as follows:

- Power supply at 5.5V, 5A maximum for the TRF-LSC-AFE7950EVM
- Power supply at 5.5V, 4A maximum for the TSW14J56EVM
- Power supply at 12V, 3A maximum for the TSW14J57EVM (optional evaluation). See the AFE79XX-HSC-DESIGN folder
- A PC that supports USB 3.0 for fast file transfer from ADC capture and DAC pattern loading
- High-quality RF signal generator that supports RF frequency of interest for evaluation. The example setup uses Keysight PSG series of signal generator.
- High-quality RF spectrum analyzer that supports RF frequency of interest for evaluation. The example set-up uses Rohde and Schwarz FSQ-26 series of spectrum analyzer.

4.1.2 Required Hardware

The required hardware for the TRF-LSC-AFE7950EVM is:

- TSW14J56 EVM (optional: TSW14J57EVM)
- TRF-LSC-AFE7950EVM
- USB 3.0 cable
- USB 2.0 Mini-B cable
- Two power-supply cables

Two bench power supplies are required to power the TRF-LSC-AFE7950EVM and TSW14J5xEVM. A personal computer (PC) is required to program the EVM and capture card. See also Section 4.1.1. All lab-equipment requirements (such as signal source, signal analyzer, and so forth) are left to user discretion.

Note

Typically, the bench power supply with a rating of 5.5V is used to power the TRF-LSC-AFE7950EVM. The nominal EVM power supply voltage is 5V. The additional 0.5V overhead is added to compensate for the power cable loss because the TRF-LSC-AFE7950EVM and TSW14J56/TSW14J57 are configured to full operating mode to accommodate the voltage drop associated with power cable loss.

4.1.3 Steps to Start Automatic Configuration

1. Start the HSDC PRO software by going to *Start* > *Texas Instruments* > *High Speed Data Converter Pro*. Figure 4-1 illustrates that the HSDC PRO application started properly. Take note of the *Serial Numbers* of the TSW14J56EVM after the device is connected.

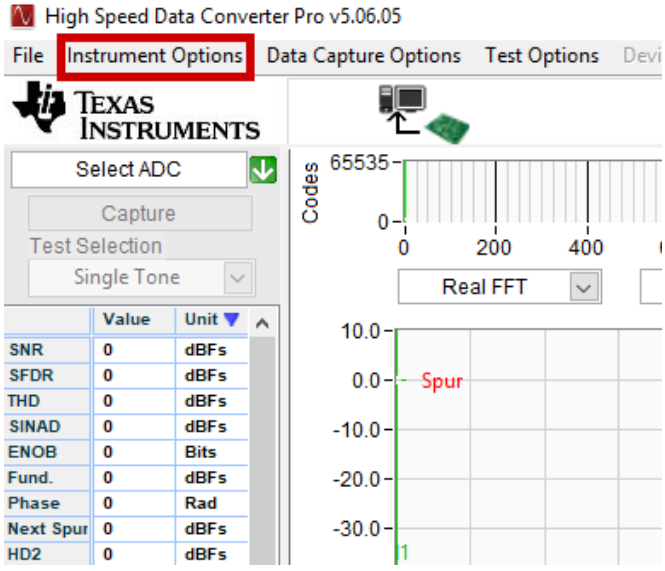


Figure 4-1. Connecting to TSW14J56 From HSDC PRO

2. Press the *OK* button to proceed the connection of the TSW14J56 EVM to the PC.

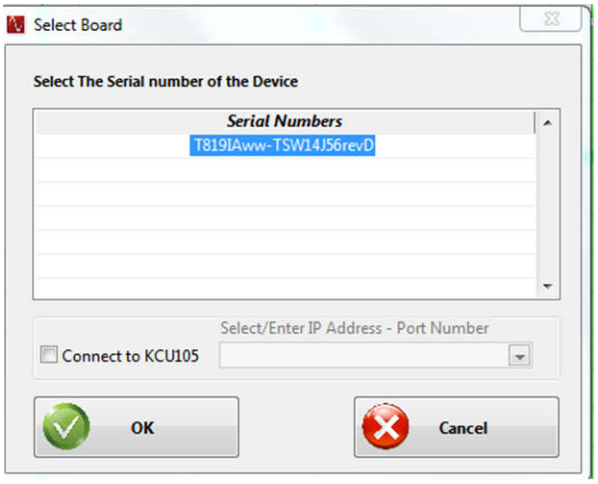


Figure 4-2. HSDC PRO Connect to Board

3. Start the Latte software by going to *Start* > *Texas Instruments* > *Latte*. Ensure that the Latte software starts properly.
4. On the left side of the Latte application, within the *Scripts* window, expand *AFE79xx* > *Automation* > *AFE79xx_TSW14J56_Mode1.py*. Figure 4-3 shows the python script.

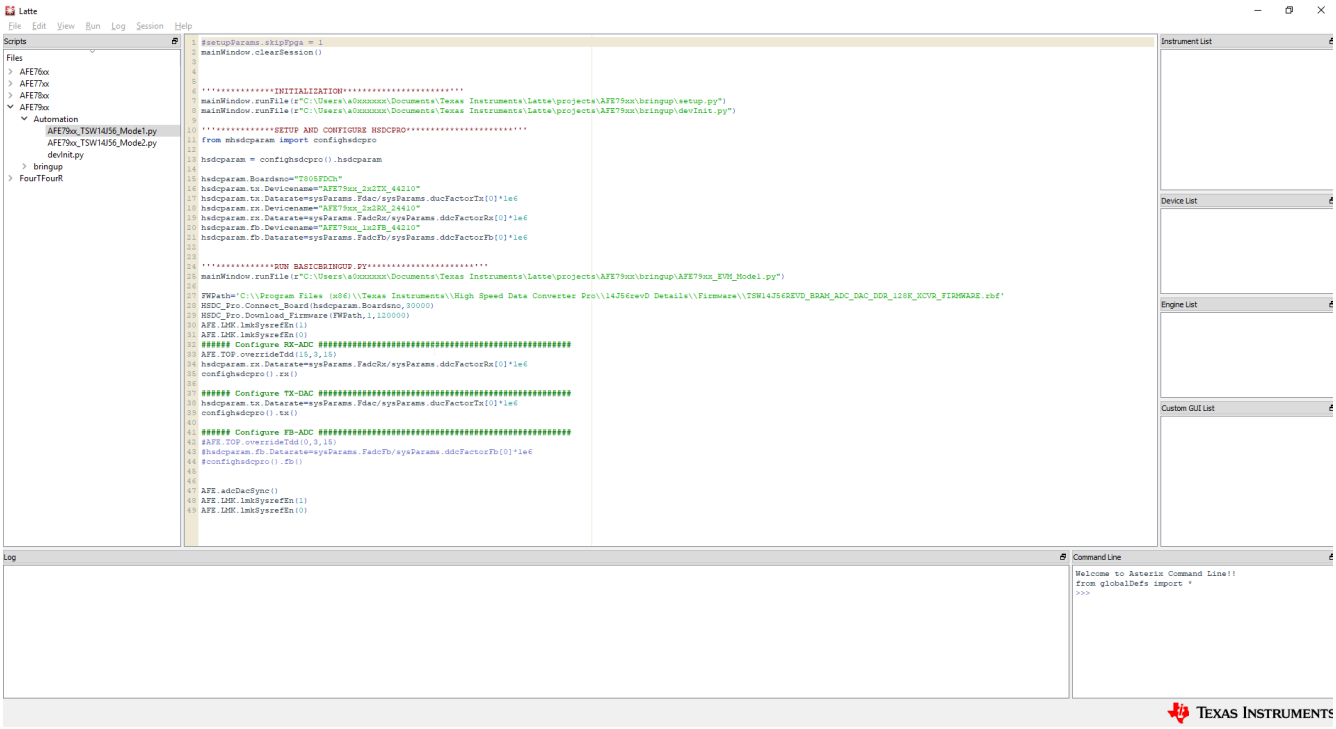


Figure 4-3. AFE79xx Mode 1 Automatic Configuration Script

5. Change three parameters within the AFE79xx_TSW14J56_Mode1.py per the directory used by the HSDC PRO and Latte software.
6. Figure 4-4 shows where to change items 1 and 2 to reflect the location of the Latte install directory for the setup.py and devInit.py. Typically, the area where *a0xxxxxx* is replaced with the Windows user ID login.

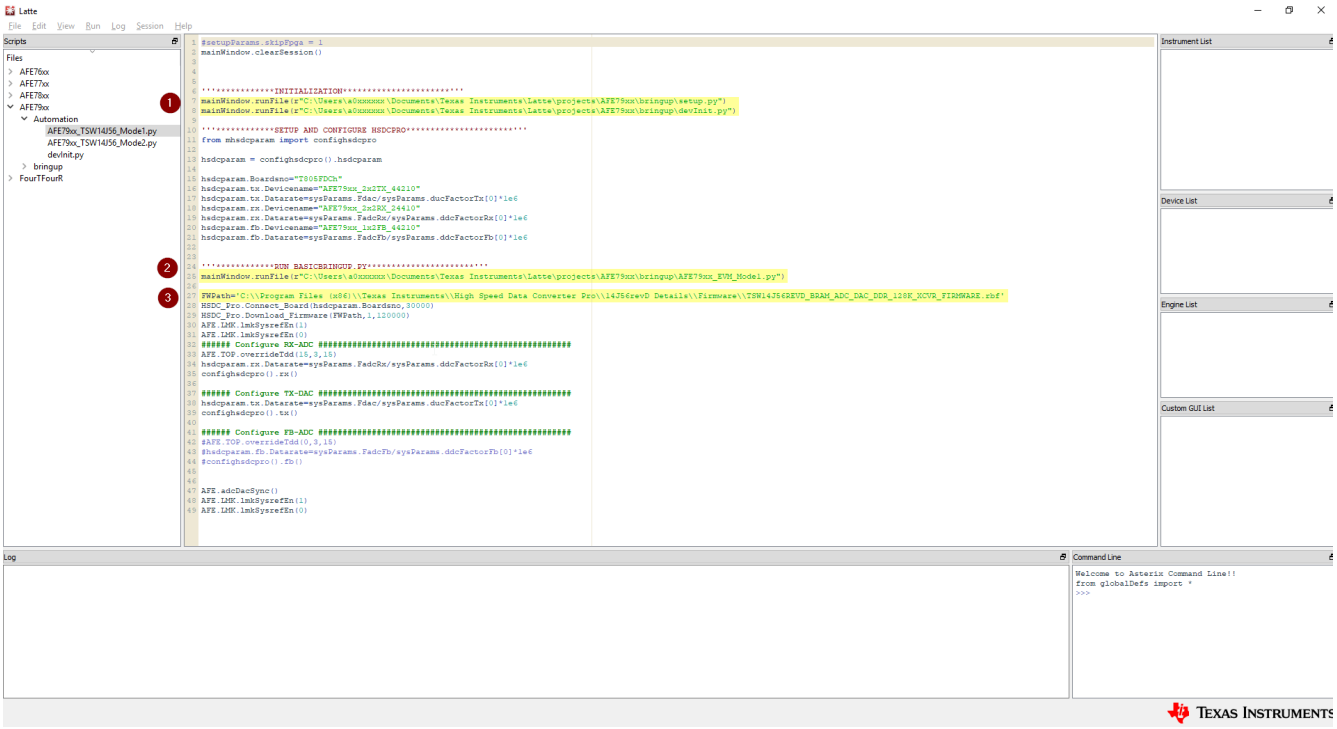


Figure 4-4. Directory Parameter to be Changed in the Automation Script

7. Figure 4-4 shows where to change item 3 to reflect the location of the *High-Speed Data Converter Pro* directory for the TSW14J56 firmware.
8. Figure 4-5 shows where to enter the serial number of the TSW14J56 EVM per the highlighted line.

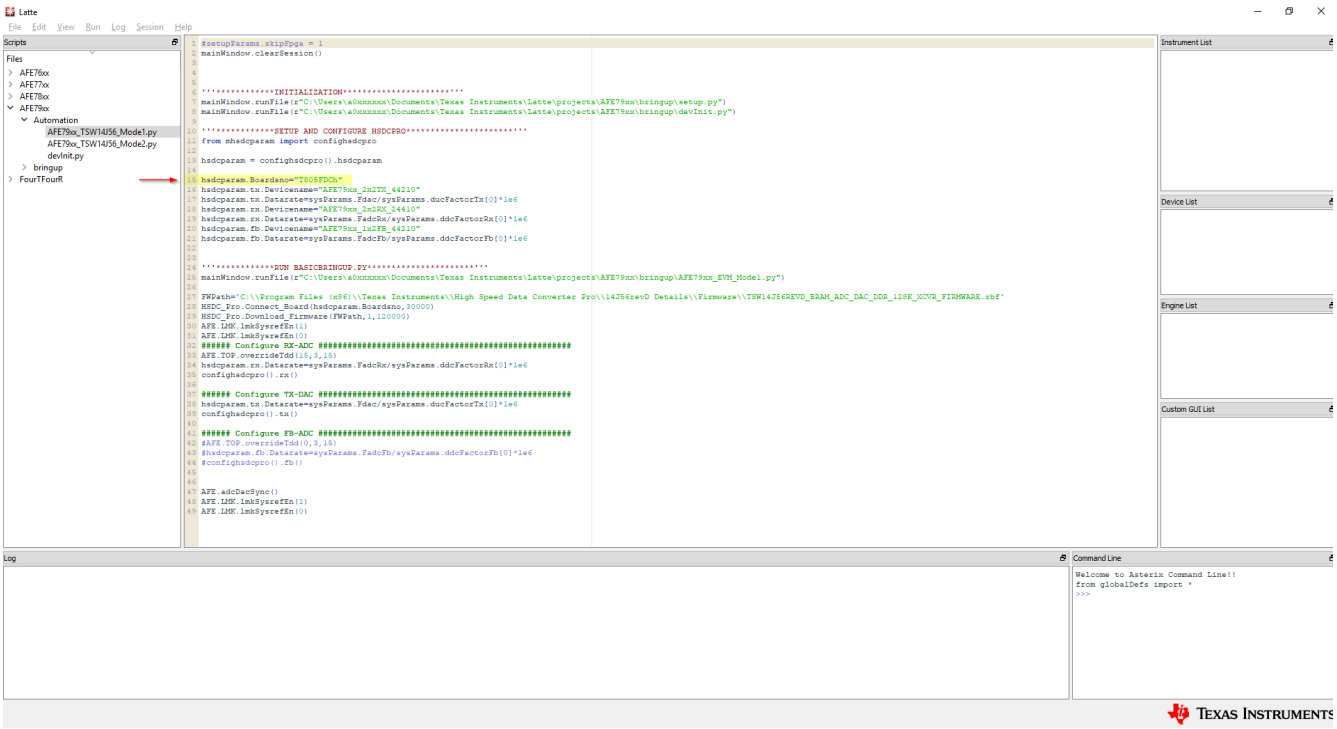


Figure 4-5. TSW14J56 EVM Serial Number Location

9. With the AFE79xx_TSW14J56_Mode1.py highlighted, press the F5 button to execute the script. The script automates both the HSDC PRO and Latte software to automatically bring up the JESD204B link.
10. Figure 4-6 and Figure 4-7 show the expected following two error messages after the script runs.

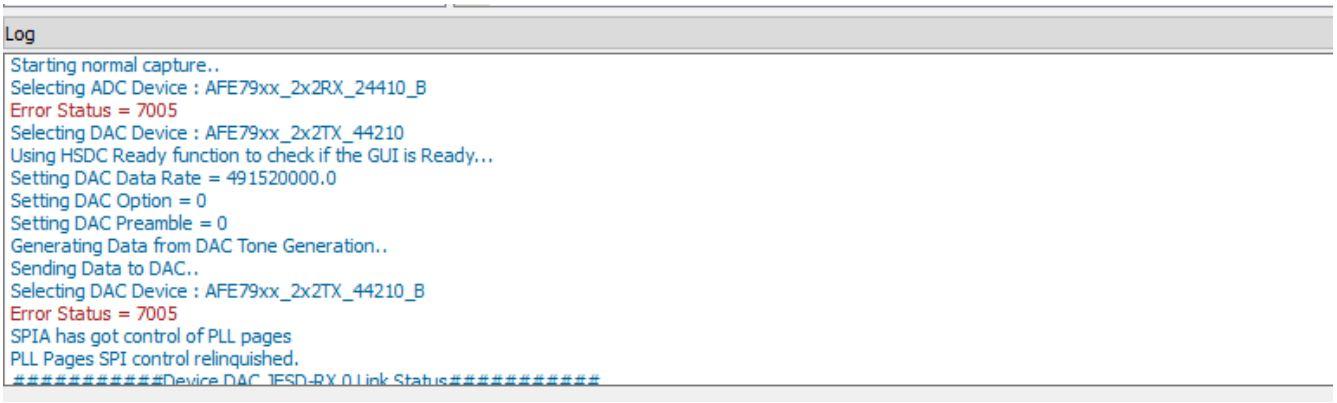


Figure 4-6. Latte Error 1

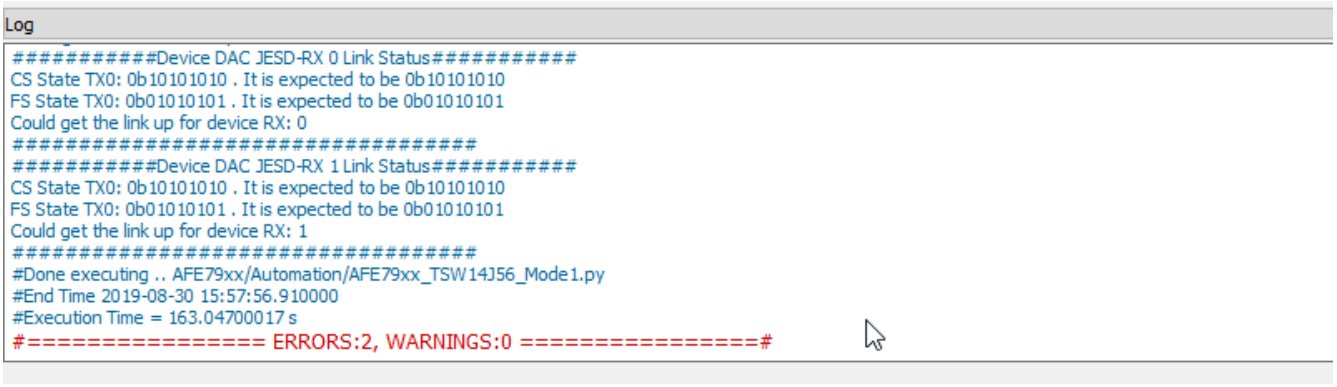


Figure 4-7. Latte Error 2

11. The default TRF-LSC-AFE7950EVM has the following RF frequency matching network:
    a. RXA (TRF1208): 1.8GHz–2.3GHz
    b. RXB (TRF1208): 4.8GHz–5.5GHz
    c. RXC (TRF1208): 7.3GHz–7.8GHz
    d. RXD (Balun): None
    e. FB1 (TRF1208): 5.8GHz–6.2GHz
    f. FB2 (Differential connectors): 6GHz
    g. TXA (TRF1108): 1GHz–5GHz
    h. TXB (Balun): 3.9GHz–4.3GHz
    i. TXC (TRF1108): 700MHz–8GHz
    j. TXD (TRF1108):2.5GHz–4.5GHz
12. The example script to change the NCO to match the default RF frequency matching network is the following:

```
AFE.updateTxNco(0,200,0,0)
AFE.updateTxNco(1,5000,0,0)
AFE.updateTxNco(2,7500,0,0)
AFE.updateTxNco(3,3000,0,0)
AFE.updateRxNco(0,2100,0,0)
AFE.updateRxNco(1,5200,0,0)
AFE.updateRxNco(2,7800,0,0)
AFE.updateRxNco(3,6000,0,0)
AFE.updateFbNco(0,6000,0)
AFE.updateFbNco(1,6000,0)
```

13. Figure 4-8 shows where to enter the commands in the command line prompt or execute AFE79xx_DC101_NCO_Setup.py (under the *AFE79xx* > *Automation* folder) in the Latte using the F5 key.

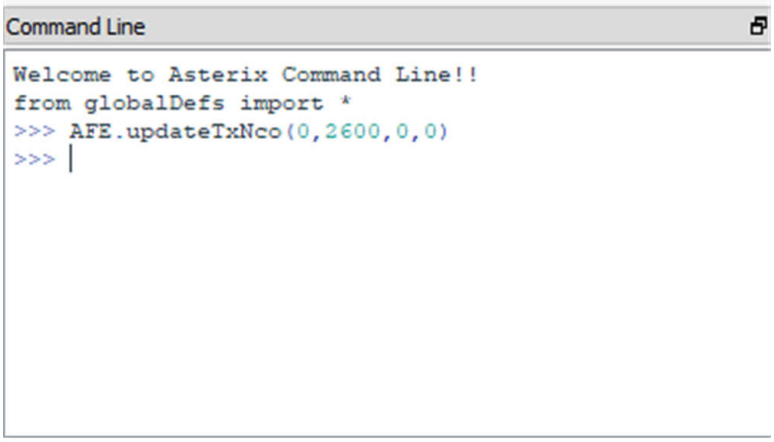


Figure 4-8. Latte Command Prompt for Updating TXNCO

4.1.4 TXDAC Evaluation

Connect the spectrum analyzer to J10 (TXA), J7 (TXB), J21(TXC), or J22 (TXD) to monitor the TXDAC output. After the connection is made, the DAC patterns are able to be changed, or custom DAC patterns are able to be loaded through external files (see also Section 4.1.7.1).

4.1.5 RXADC and FBADC Evaluation

1. Before starting the RXADC and FBADC performance capture, set up the HSDC PRO test option. Go to *Test Options* to enter the *Filter Parameters* menu. By default, there are 25 bins to remove on either side of fundamental and 25 bins near dc to remove. Per Figure 4-9, change the number of bins to remove on either side of fundamental to 100 bins.
   a. With a data rate of 245.76MSPS for RXADC at 16384 sample points, 1.5MHz of bins on either side of the fundamental are removed.
   b. With a data rate of 491.52MSPS for FBADC at 16384 sample points, 3.0MHz of bins on either side of the fundamental are removed.
   c. The number of bins to remove is a standard recommendation from TI. This recommendation removes the effect of the ADC sampling clock in-band phase noise from affecting the broadband noise used to calculate the SNR through the FFT engine. Adjust the number of bins based on the end-application standard.

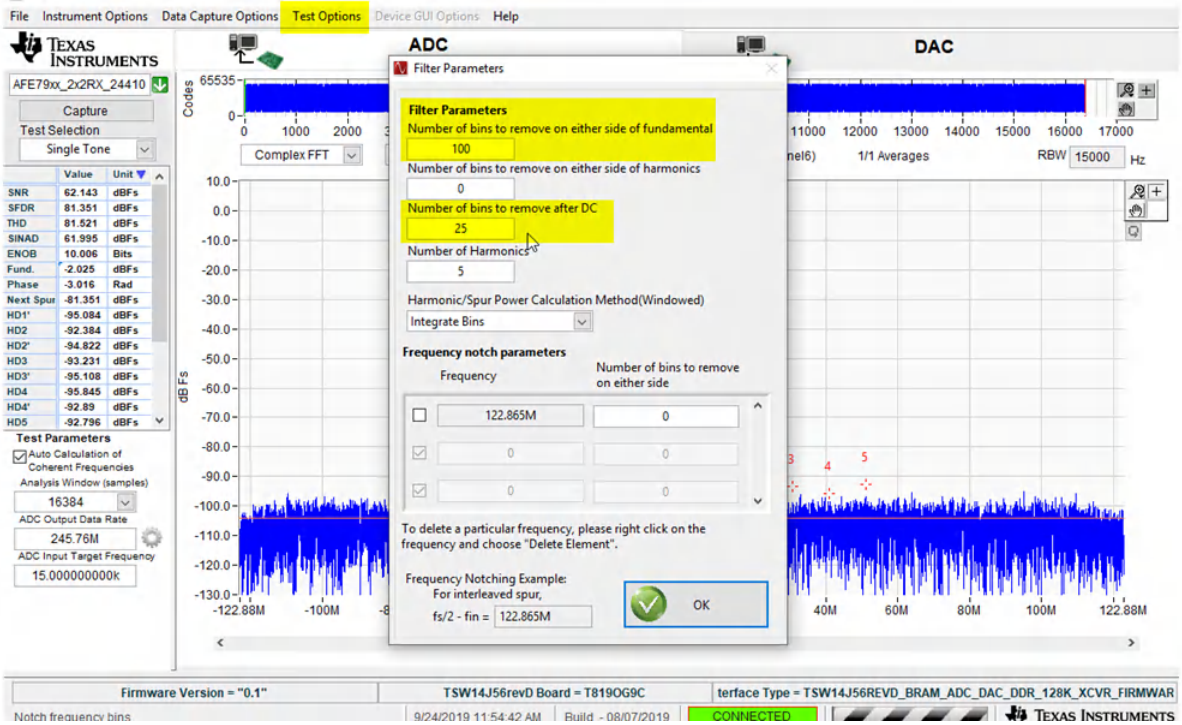


Figure 4-9. HSDC PRO ADC Performance FFT Binning Configuration

2. Connect the RF signal generator output to J3 (RXA_IN), J1 (RXB_IN), and J4 (RXC_IN) to capture the RF input to the ADC. On the HSDC PRO application, press the *Capture* button to capture the ADC data.

3. Feed in a tone of 10MHz offset from the channel frequency. For example, feed 2210MHz to RXA_IN, 5010MHz to RXB_IN, and 6010MHz to FB1_IN. Set the signal level to get approximately –4 dBFS at the ADC output. The gain is different for various channels; therefore, the signal generator output levels are different.
   a. RXA_IN is channel 1 and 2 in FFT channel selection
   b. RXB_IN is channel 3 and 4 in FFT channel selection
   c. FB1_IN is channel 1 and 2 in FFT under FB mode channel selection
4. Similarly, feed 7510MHz to RXC_IN and 6010MHz to FB2_IN. Set the signal level to get approximately –4dBFS at the ADC output.
   a. RXC_IN is channel 5 and 6 in FFT channel selection
   b. FB2_IN is channel 3 and 4 in FFT under FB mode channel selection
5. For the feedback ADC, execute the following commands or execute AFE79xx_FB_Capture.py through the F5 key.
   a.
```
###### Configure FB-ADC
####################################################
AFE.TOP.overrideTdd(0,3,0)
hsdcparam.fb.Datarate=sysParams.FadcFb/sysParams.ddcFactorFb[0]*1e6confighsdcpro().fb()
```

4.1.6 TRF-LSC-AFE7950EVM Manual Configuration

This section guides the user through the sequence of steps to manually bring up the TRF-LSC-AFE7950EVM. The automatic setup process is broken down in this section to allow the user to understand the process and make modifications accordingly.

4.1.6.1 TSW14J5x DAC Pattern Setup

Configure the HSDC PRO GUI to send a DAC pattern from the TSW14J5x board. If needed, see Section 4.1.7.1 and Section 4.1.7.2.

Note

Send a digital-to-analog converter (DAC) pattern to the TRF-LSC-AFE7950EVM before configuring the EVM to provide the proper training SERDES signal for the adaptation algorithm of the AFE79xx SerDes RX equalizer. The DAC pattern can be sent from the TSW14J5x board controlled through the HSDC PRO GUI.

4.1.6.2 Connect Latte to Board

This step establishes a connection between the PC running Latte and the TRF-LSC-AFE7950EVM.

1. In the *Scripts* window, select *setup.py* and press F5 to run the program.
2. Check the *Log* window to ensure there are no errors. The following line is displayed four times: *Kintex RegProgrammer – USB Instrument created*.
3. Missing or obsolete drivers for the FT4232H chip in the TRF-LSC-AFE7950EVM is a common error source. Use the device manager to verify a connection between the PC and the EVM by checking the USB instantiations.
4. Update the PC with the appropriate drivers, if necessary.

4.1.6.3 Compile Libraries

In this step, the library of scripts packaged with the Latte GUI is compiled and takes approximately half a minute to run.

1. In the scripts window, select *devInit.py*.
2. Press F5 to run the program.
3. Check the Log window for status and errors.

4.1.6.4 Program TRF-LSC-AFE7950EVM

In this step, the AFE79xx on the TRF-LSC-AFE7950EVM is programmed.

1. Click on the script named *AFE79xx_EVM_Mode1.py* and press F5. No errors are expected; ignore warnings regarding SPI control, relinquish, and reset property. This step takes a few minutes.
2. Check the *Log* window to monitor any errors. This step completes the TRF-LSC-AFE7950EVM configuration. Current consumption into the TRF-LSC-AFE7950EVM is approximately 4A.
3. An LOS error indicates that the SerDes RX is electrically idle, in which case, the TX output is not normal. To resolve this error, resend the data (the DAC pattern) and reconfigure the TRF-LSC-AFE7950EVM (that is, run *basicbring-up.py* again).
4. GPIO warnings or SYSREF errors typically indicate supply voltage or current limitations. Verify the power supply to the TRF-LSC-AFE7950EVM, and ensure a 5.5V supply voltage and a 5A current limit are used. Restart the Latte GUI and rerun the scripts.

4.1.6.5 Modify Configuration

The examples in the previous sections show how to configure the AFE79xx with the default mode set in Latte scripts. The mode can be changed by modifying a set of parameters.

4.1.7 Setup the TSW14J5x With the HSDC PRO

This chapter is intended to serve as a quick-start guide for users not familiar with the TSW14J5x and the HSDC PRO GUI. See the *High Speed Data Converter Pro GUI User's Guide* for more details.

4.1.7.1 DAC Pattern Setup and Send

This section lists the steps to create and send a DAC pattern from the TSW14J5x board.

1. Click on the HSDC PRO DAC tab. Figure 4-10 shows a brief description of the DAC tab.

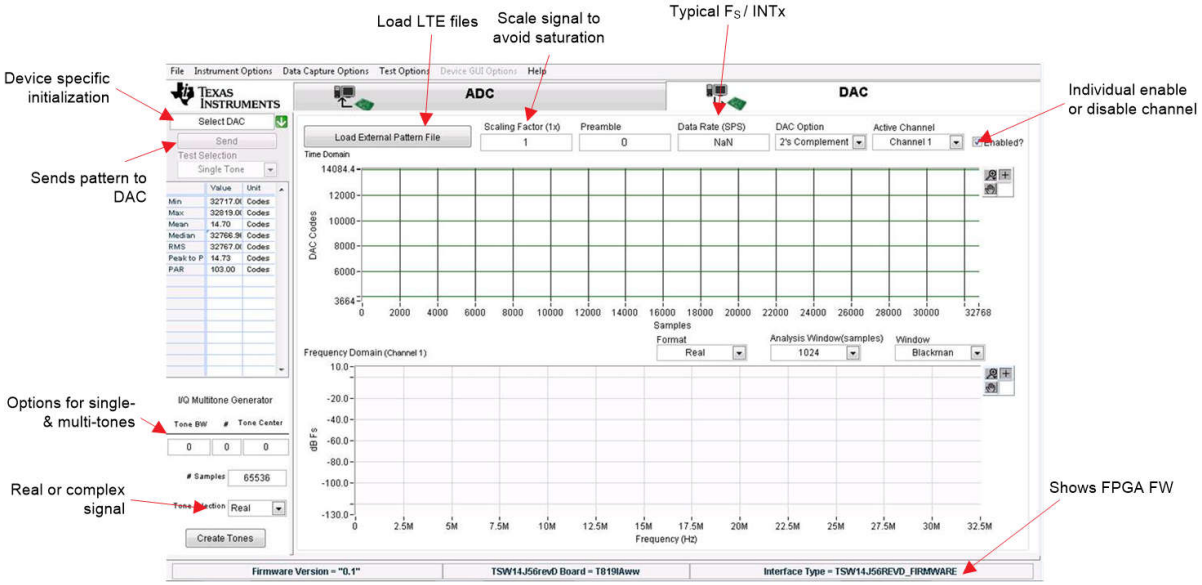


Figure 4-10. HSDC PRO DAC Tab Overview

2. Figure 4-11 shows a pictorial representation to create and send a sinusoid.

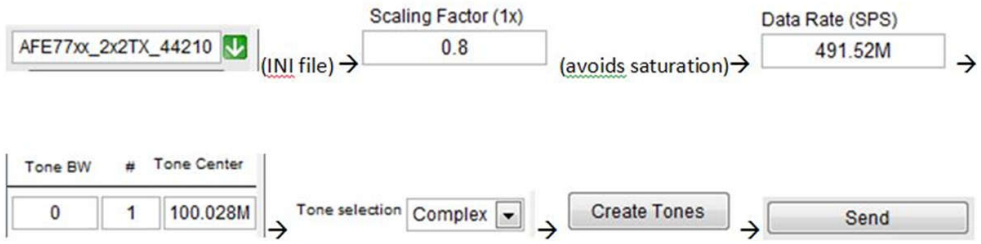


Figure 4-11. Setup a Sinusoid

3. How to create and send a sinusoid is outlined in the following steps:
   a. Select *AFE79xx_2x2TX_44210* in the device-specific initialization option. Click *Yes* if prompted to download the firmware (FW). The default option is to run the board in the transceiver mode of operation, which enables simultaneous operation of the TX and the RX and FBRX. The FW used in transceiver mode has the letters *XCVR* in the name.
   b. Enter *491.52 M* as the data rate and *0.9* for a scaling factor.
   c. Create a sinusoid by entering the frequency in the *Tone Generator* section of the HSDC PRO window.
   d. Press *Send* to transmit the DAC pattern to the TRF-LSC-AFE7950EVM. Figure 4-12 shows the resulting message with the lane rate and reference clock expected in the FPGA. Click OK.

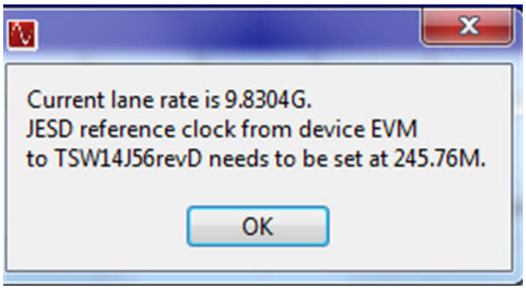


Figure 4-12. HSDC PRO Lane and Reference Clock Rate Pop-Up

Figure 4-13 shows an example setup with a 100MHz sinusoid.

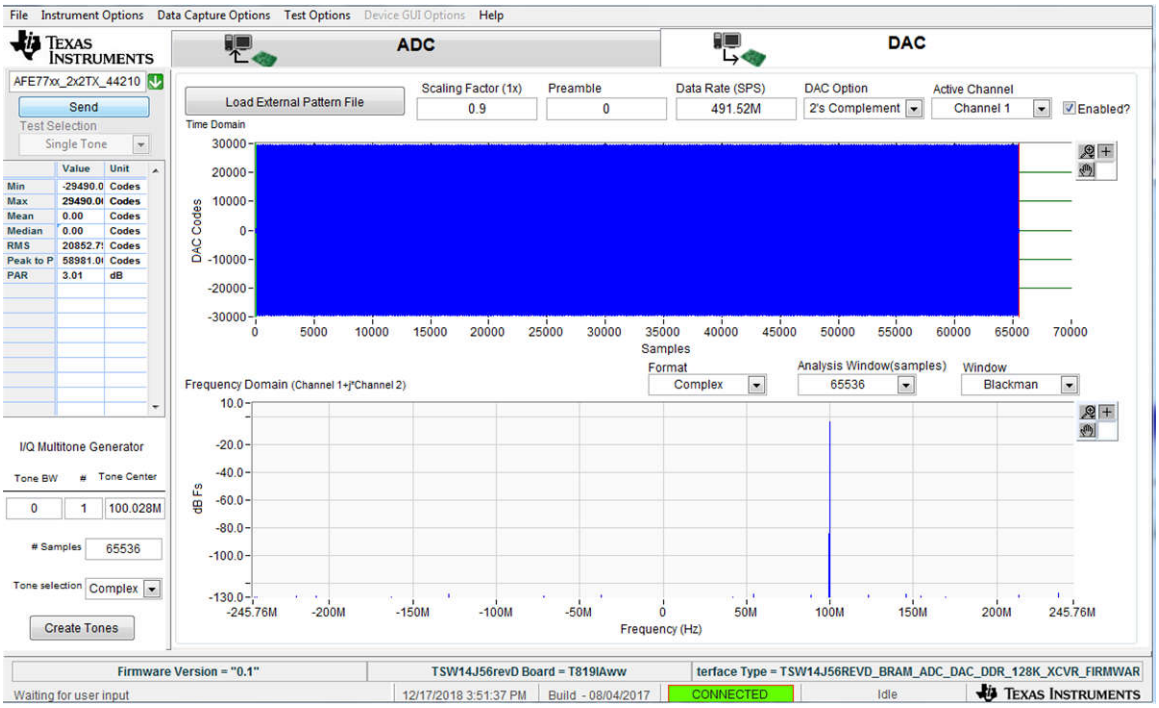


Figure 4-13. HSDC PRO CW

Alternatively, load a pattern file (for example, LTE) and send using the *Load External Pattern File* button.

The DAC setup is now complete.

4.1.7.2 DAC Synchronization Check

The steps to check the DAC synchronization are as follows:

1. LED D2 on the TSW14J56 board blinks to indicate a successful JESD204 link on the DAC side.
2. If the LED is not blinking, then send the DAC pattern again.

4.1.7.3 ADC Data Capture

The steps to capture the ADC output are as follows:

1. Click on the HSDC PRO *ADC* tab. Figure 4-14 shows a brief description of the ADC tab.

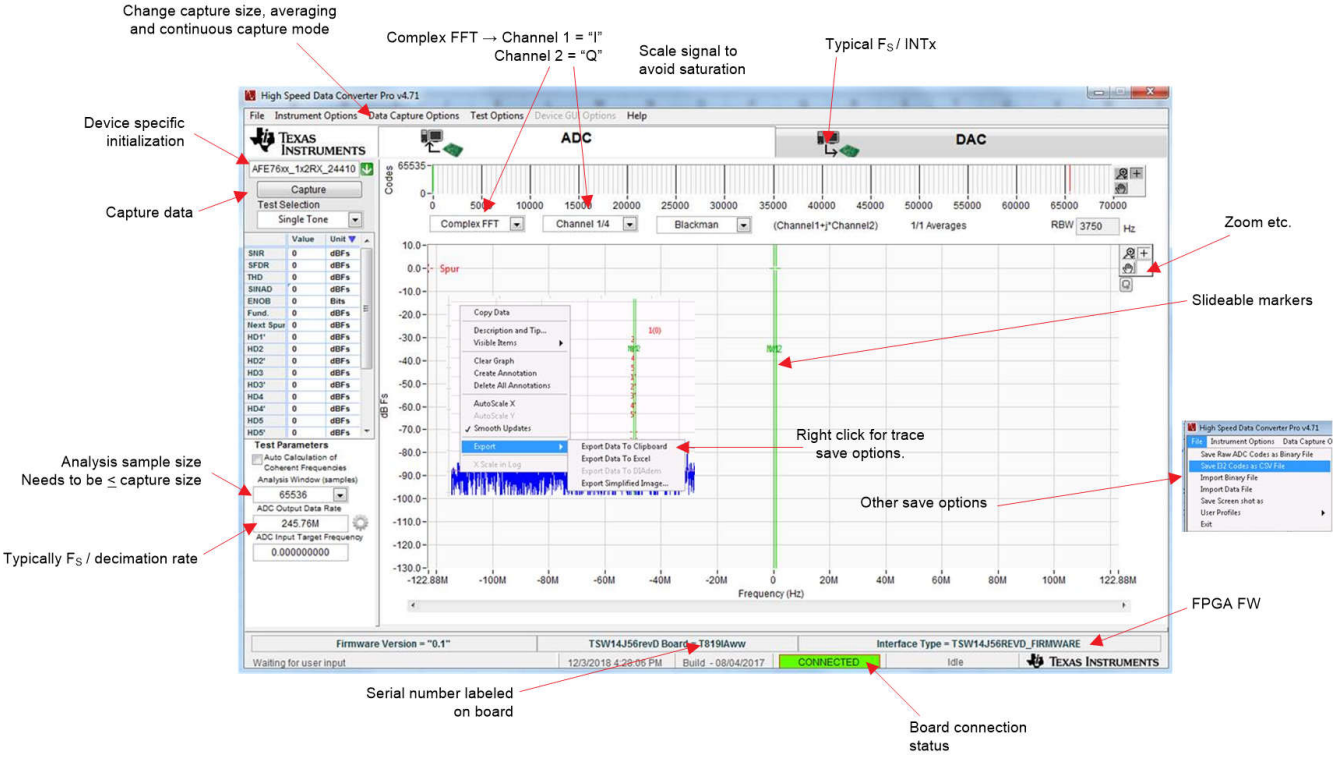


Figure 4-14. HSDC PRO ADC Tab Overview

2. Select *AFE79xx_2x2RX_24410* as the device.
3. Go to *Data Capture Options* in the menu bar and choose the *Capture* option. Set samples (per channel) to 16384. Click the *OK* button.
4. Select *16384* in the *Analysis* window located in the lower-left section of the GUI.
5. Enter *245.76 M* for ADC output data rate.
6. Click the *Capture* button.

The capture size is set to a lower value (such as 16K) because of the limited BRAM memory available in the FPGA.

4.1.7.4 ADC Synchronization Check

After a successful capture on the ADC side, LED D4 on the TSW14J56EVM board blinks to indicate a successful JESD204 link on the ADC side. The FFT output is also seen in the HSDC PRO ADC tab. A timeout on the ADC capture indicates a unsuccessful bringup of the AFE79xx. Try again after rerunning the AFE79xx configuration.

4.2 Status Check and Troubleshooting Guidelines

This section provides a general guideline on the status indicators of the TRF-LSC-AFE7950EVM and the respective troubleshooting guidelines.

4.2.1 EVM Status Indicators

At this point, green LED D3 is lit. D3 indicates that PLL loop 2 of the TRF-LSC-AFE7950EVM is locked. Optionally, LED D4 indicates that PLL loop 1 of the TRF-LSC-AFE7950EVM is locked. If there are external equipment providing a 10MHz reference to the TRF-LSC-AFE7950EVM for lab-equipment synchronization, then LED D4 is lit. The EVM still functions without PLL loop 1 running, but PLL loop 2 is necessary for a successful bringup.

- If PLL loop 1 is not running, then check the 10MHz reference. This check is necessary to achieve signal coherency with the signal generators and spectrum analyzer.
- If PLL loop 2 is not locked, then contact TI applications for additional support.

4.2.2 TSW14J56 EVM

D1 and D3 are not lit for the TSW14J56EVM. D2 and D4 flash. These requirements are necessary for the JESD204B transceiver mode to work. D2 flashing indicates the TXDAC-JESD204B link is established, while D4 flashing indicates the RXADC or FBADC JESD204B link is established.

The TRF-LSC-AFE7950EVM data transmission on the DAC and data capture on the ADC is enabled at this point. The RXNCO, FBNCO, and TXNCO are now adjustable.

RXDSA, FBDSA, and TXDSA are also adjustable.

```
##RXDSA Adjustment
                    AFE.DSA.setRxDsa(chNo,dsaSetting)  ##chNo: ranges 0-3. dsaSetting: DSA
setting in dB
                    ##FBDSA Adjustment
                    AFE.DSA.setFbDsa(chNo,dsaSetting)  ##chNo: ranges 0-1. dsaSetting: DSA
setting in dB
                    ##TXDSA Adjustment
                    AFE.DSA.setTxDsa(chNo,dsaSetting)  ##chNo: ranges 0-3. dsaSetting: DSA
setting in dB
```

4.3 Performance Data and Results

See the Design and Support files page.

5 Hardware Design Files

5.1 Schematics

To download the schematics, see the Design files page.

5.2 PCB Layouts

To download the PCB guidelines and example layouts, see the Design files page.

5.3 Bill of Materials (BOM)

To download the bill of materials (BOM), see the Design files folder.

6 Additional Information

6.1 Trademarks

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3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

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Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

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4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

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