User's Guide
SLAU616A–January 2015–Revised January 2016

ADS54J54 Evaluation Module

This document outlines the basic steps and functions that are required to ensure the proper operation of the Texas Instruments (TI) ADS54J54 Evaluation Module (EVM). The EVM includes an ADS54J54EVM, a cable for connection to an external 5-VDC power supply, and a mini-USB cable. This EVM is designed to be used with the TI TSW14J56EVM JESD204B capture card using an FMC connector interface or FPGA development boards, such as the Xilinx KC705 or Altera Arria V. The ADS54J54EVM contains an ADS54J54 (14-bit) four-channel, 500-MSPS ADC. The EVM also contains a TI LMK04828 clock jitter cleaner. When used with the TSW14J56EVM, JESD204B standard output data from the EVM is captured and sent to a host PC for analysis. This guide helps users to quickly evaluate the performance of the ADS54J54EVM board by capturing and displaying waveforms using the TSW14J56 with the High Speed Data Converter Pro GUI software. The EVM schematics, BOMs, and layout files are found in the design package under the ADS54J54EVM tool folder on www.ti.com.

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1 Introduction

1.1 Overview

The ADS54J54EVM is an evaluation module (EVM) used to evaluate Texas Instruments' ADS54J54 ADC and the LMK04828 clock jitter cleaner devices. The ADS54J54 (14-bit) is a four-channel, 500-MSPS ADC with buffered analog inputs and outputs featuring a JESD204B interface. The EVM has transformer-coupled analog inputs accommodating a wide range of signal sources and frequencies. The LMK04828 provides an ultra-low-jitter and phase-noise sample clock along with system reference clocks and a device sample clock for the mating FPGA capture board, for a complete JESD204B subclass 1 clocking solution.

The ADS54J54 and LMK04828 are controlled through an easy-to-use software GUI enabling quick configuration for a variety of uses.

The TSW14J56EVM connects directly to the ADS54J54EVM. The High Speed Data Converter Pro software GUI processes the data from the TSW14J56EVM to quickly assess the performance of the ADS54J54. The FMC output interface connector of the EVM has also been verified to be compatible with both the Xilinx KC705 and Altera Arria V evaluation platforms.

1.2 Block Diagram

The block diagram for the ADS54J54EVM is shown in Figure 1. The various inputs, outputs, and jumpers of the ADS54J54EVM are described in Table 1.

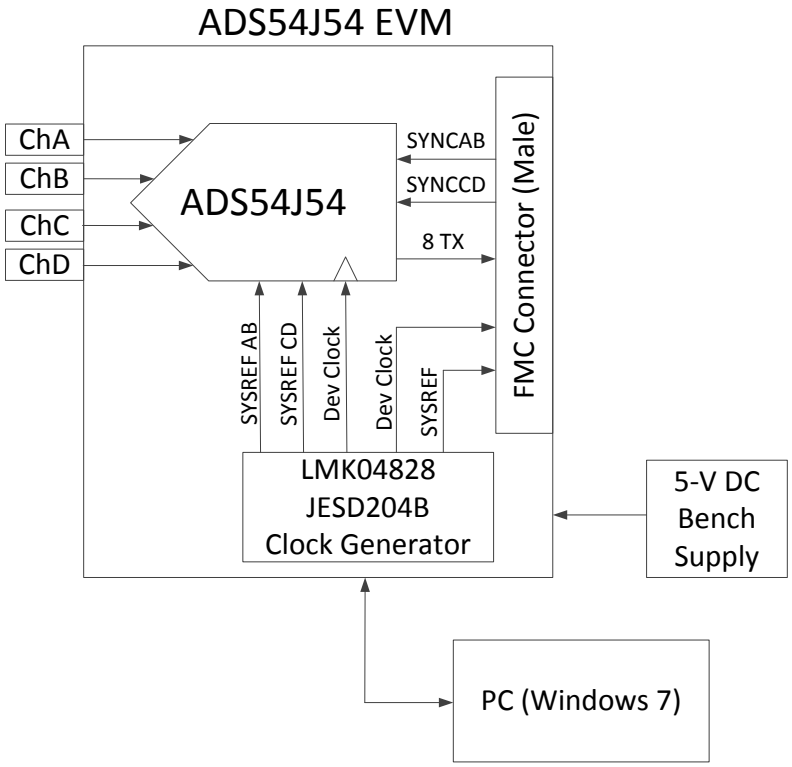

Figure 1. Block Diagram of the ADS54J54EVM

Table 1. Input and Output Connectors and Jumper Descriptions of the ADS54J54EVM

Component	Description
J1 (AINP)	Analog input for channel A, single-ended or positive side of differential. (Negative side of differential on J11, normally not installed.)
J2 (BINP)	Analog input for channel B, single-ended or positive side of differential. (Negative side of differential on J12, normally not installed.)
J23 (CINP)	Analog input for channel C, single-ended or positive side of differential. (Negative side of differential on J25, normally not installed.)
J22 (DINP)	Analog input for channel D, single-ended or positive side of differential. (Negative side of differential on J24, normally not installed.)
J19 (EXT_ADC_CLK)	Single-ended ADC clock input
J20 DCLK	Optional device clock output, single-ended transformer coupled
J8 (+5V)	Positive power connection (5 V)
J9 (GND)	Negative power connection (GND)
J13 (Main PWR)	5-V input from +5-V bench supply (cable supplied)
J14 (REF OSC_IN)	External reference option for LMK04828, REFOUT1 source on J16 and CPLD_CLK
J16 (REFOUT1)	10-MHz CMOS level reference output or frequency of REF OSC_IN if option selected
J6 (USB)	USB connection
J3	JESD204B FMC interface connector
J5 (TRIG_IN)	External trigger input for ADS58J89 burst mode. Not used for ADS54J54.
J26 (TRIG_OUT)	Trigger output, buffered version of ADS58J89 burst mode trigger, normally connected to trigger input of TSW14J56 capture card. Normally not used for ADS54J54.
J7 (LMK CLKIN1_P)	CLKIN0 input for LMK04828. Option to provide an external clock source to the LMK in place of on-board 100-MHz VCXO.
J10 (CLKOUT6P)	DCLKOUT6p from LMK04828. Default is LVPECL at 250 MHz.
J15 (CLKOUT6N)	DCLKOUT6n from LMK04828. Default is LVPECL at 250 MHz.
J17 (CLKOUT7P)	SDCLKOUT7p from LMK04828. Default is LVPECL at 6.25 MHz.
J4 (CLKOUT7M)	SDCLKOUT7m from LMK04828. Default is LVPECL at 6.25 MHz.
J18 (PROG CPLD)	JTAG interface for CPLD U3
SW1 (ADC_RESET)	Switch to reset the ADC using the RESET input pin
SW2 (TRIGGER)	Pushbutton trigger source for ADS58J89 burst mode. Not used for ADS54J54.
JP6 (XO_PWR)	Provides power to VCXO Y2 or oscillator Y3
SJP3 (REF_SEL)	Selects input or external reference source for LMK, J16 and CPLD. Default is internal (on-board) 10-MHz oscillator.
JP2 (CDC_CLK)	Reference clock buffer output enable
JP5 (REF_PWR)	Power enable for 10-MHz reference oscillator
SJP1 (REF_EN)	Enable for 10-MHz reference oscillator
SJP4-SJP11	USB/FMC Interface select. Default is using USB.
JP4 (ENABLE)	U11 enable. Install jumper to disable switcher U11. Default is uninstalled.
JP1 (PWRGD)	Test point for power good output pin from U11.

2 Software Control

This section provides installation instructions for the ADS54J54 GUI and descriptions of the various controls.

2.1 Installation Instructions

1. Download the software from the ADS54J54EVM resource page: http://www.ti.com/tool/ads54j54evm.
2. Extract the files from the zip file named *ADS54J54 EVM SPI GUI vXpY installer.zip* where *XpY* represents the version number.
3. Run *setup.exe* and follow the installation prompts.
4. Start the GUI by going to **Start Menu** → **All Programs** → **Texas Instruments ADCs** → **ADS54J54 EVM GUI**.
5. When plugging the board into the computer for the first time through the USB cable, you are prompted to install the USB drivers.
   - Microsoft® Windows® XP: If Windows XP does not automatically install the drivers, follow the prompts on the screen to do so. Do not let Windows XP search Microsoft Update for the drivers, but do let Windows XP install the drivers automatically.
   - Windows 7: After installing the GUI, Windows 7 should automatically be able to install the drivers for the ADS54J54EVM with no user input.

2.2 Software Operation

The software GUI allows full programming control of the ADS54J54 and LMK04828 devices. Figure 2 shows the GUI front panel which contains a block diagram of the ADS54J54. Clicking on the various tabs of the ADS54J54 EVM SPI GUI allows configuration of the settings contained within that tab. Detailed descriptions for each tab of the GUI are given in this section. Please refer to the ADS54J54 data sheet (SLASE67) for more detailed explanations of the register fields.

2.2.1 Top-Level GUI Controls

Figure 2 shows the top-level view of the GUI which contains the block diagram of the ADS54J54. Controls for the ADS54J54 are under the *ADS54J54* tab while controls for the LMK04828 are under the *LMK04828* tab. The *Low Level View* tab allows detailed bit-level access to all SPI registers of both the ADS54J54 and LMK04828. At all times, the status of the USB link between the PC and the EVM is indicated by an LED indicator. A green indicator means the USB link is active. A red LED indicates the USB link must be reset. The *Reconnect FTDI* button will attempt to reestablish the USB link between the PC and the EVM. For the GUI to operate correctly, it is important that the ADS54J54 and LMK04828 each be reset by clicking on the respective reset control. The reset control will reset all the internal SPI registers to their default power-on state, and then set the device in 4-wire SPI mode of operation. The USB interface on the EVM requires the ADS54J54 and LMK04828 to be in 4-wire SPI mode for the SPI readback function to work. If power is disrupted to the EVM at any time, a reset for each device is required.

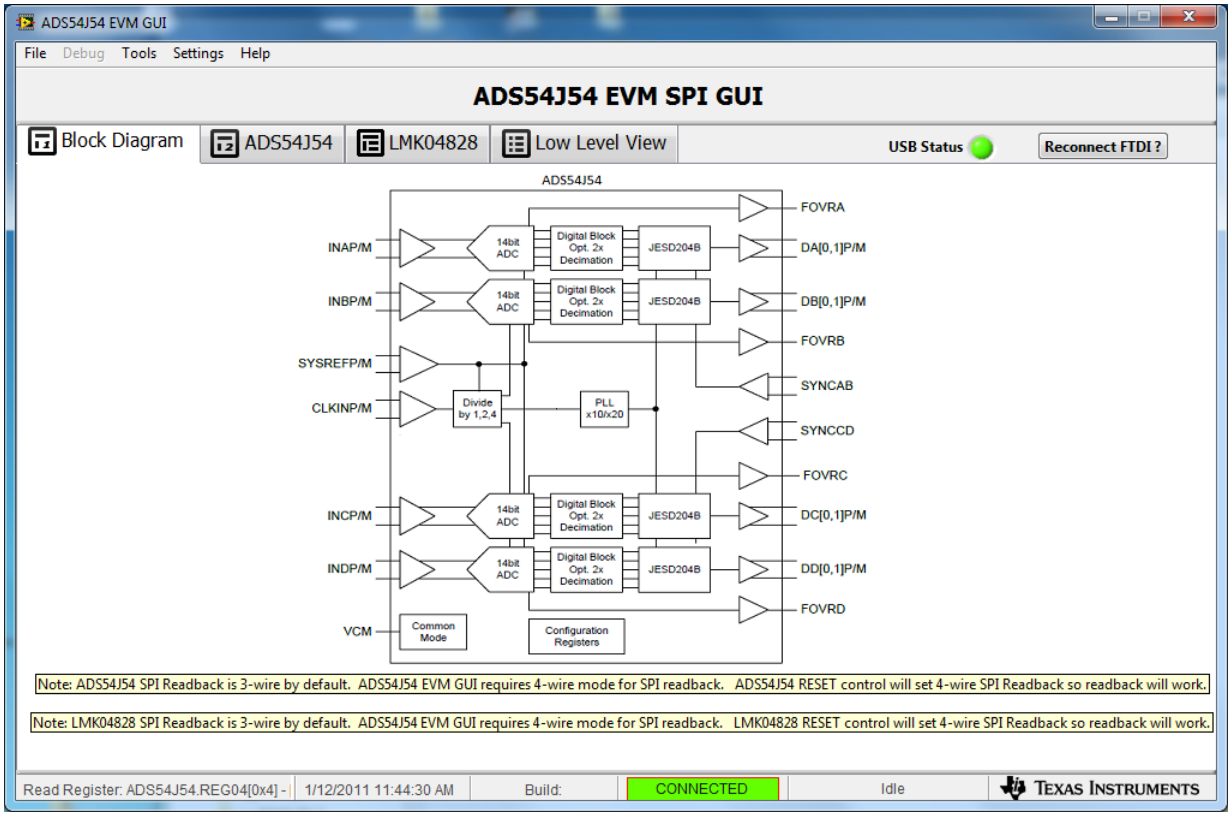

Figure 2. Top-Level Block Diagram Window of the ADS54J54 GUI

2.2.2 ADC Controls

Clicking on the *ADS54J54* tab in Figure 2 takes the user to a bank of tabs for control of the ADS54J54, one of which is the *ADC Controls* tab, as shown in Figure 3. The *ADC Controls* tab controls various ADC functions such as the over-range detection, test patterns, output modes, input clocking modes, and power down controls. Table 2 describes the controls seen in this window. The higher level tabs remain visible at all times so that the user may quickly move to controls for the LMK04828 or to low-level register controls.

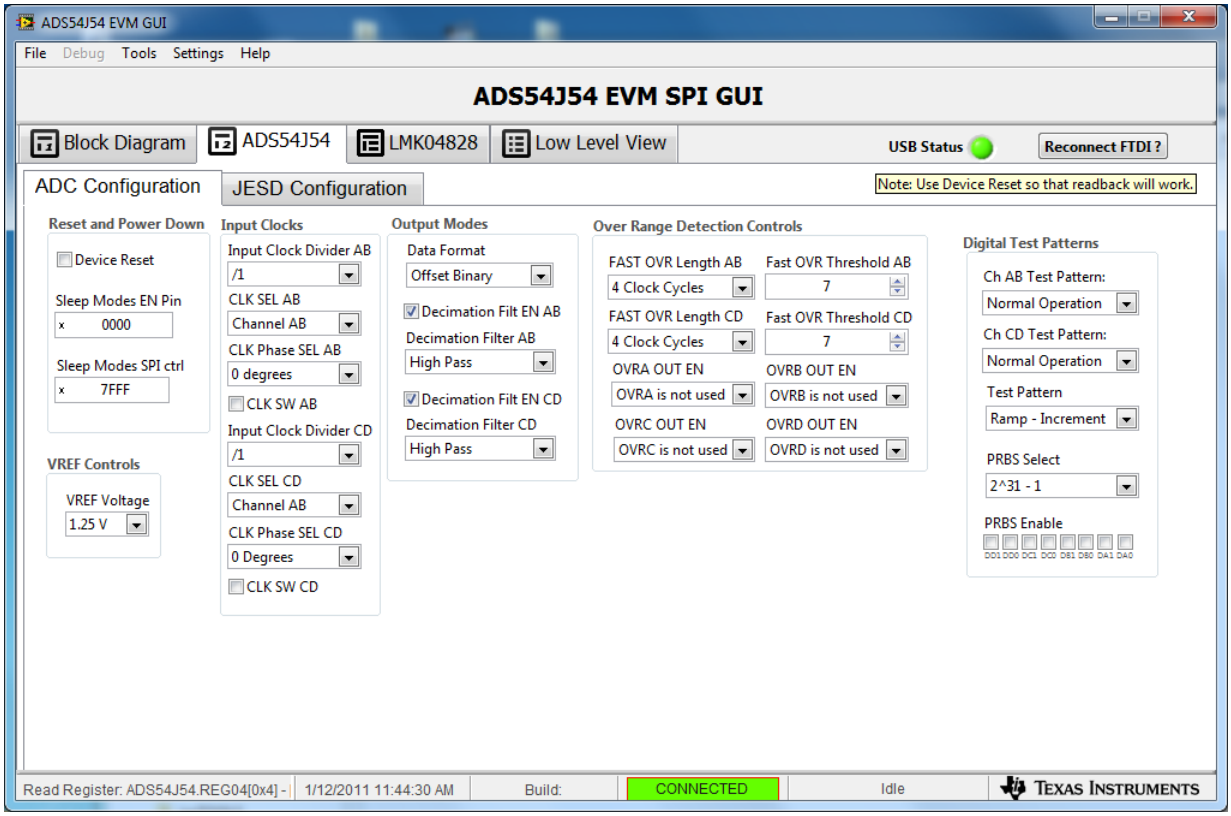

Figure 3. ADS54J54 Controls Tab

Table 2. ADS54J54 Controls Tab Descriptions

Control	Description
Device Reset	Resets the ADS54J54 SPI registers and sets the device in 4-wire SPI mode
VREF Voltage	Selects the reference voltage and thus, the full scale voltage
Input Clock Divider AB and CD	Selects an input divider of /1, /2, or /4 for channels A and B or channels C and D, respectively
CLK SEL AB and CD	Selects the clock input for channels A and B or for channels C and D, respectively
CLK Phase SEL AB and CD	Selects the phase relationship of the clock input for channels A and B or for channels C and D, respectively
CLK SW AB and CD	Used in conjunction with changing the clock phase relationship of channels A and B or channels C and D.
Data Format	Selects offset binary or two's complement data format
Decimation Filter EN AB and CD	Enables the decimation filter for channels A and B or channels C and D
Decimation Filter AB and CD	Selects whether the decimation filter will be high-pass of low-pass
Fast OVR Length AB and CD	Selects how long the OVR output is active upon overrange detection
Fast OVR Threshold AB and CD	Sets how close to full scale the input can be before the fast overrange will detect overrange
OVRx OUT EN	Selects the function of the fast OVR pin for each of the four channels

Table 2. ADS54J54 Controls Tab Descriptions (continued)

Control	Description
Ch AB and CD Test Pattern	Selects an output test pattern or normal sample data for channels A and B or channels C and D
Test Pattern	Selects the specific test pattern to be output when test pattern is selected
PRBS Select	Selects the length of the PRBS test pattern
PRBS Enable	Selects the PRBS test pattern to be output on individual serial lane outputs

2.2.3 JESD204B Controls

Clicking on JESD204B Configuration opens the *JESD204B Configuration* controls tab, shown in Figure 4. Use the ADS54J54 data sheet (SLASE67) for reference to assist with the descriptions of these various controls. The ADS54J54 EVM SPI GUI comes with a number of configuration files that will set the EVM into a known and tested configuration that works with the TSW14J56 capture card. Full control of the JESD204B configuration is possible with the use of this tab of controls. Of primary importance are the JESD204B parameters L, M, F, and K. The parameter M refers to the number of data converters in a JESD204B link, and since the ADS54J54 is a four channel device, then M is assumed to be 4. The parameter L refers to the number of lanes used. The ADS54J54 may use one lane per channel when in 2x decimation mode to output 250 Msps or use 2 lanes per channel when outputting sample data at 500 Msps. L may then be either 4 or 8. The parameter F is the number of octets (an octet is half of a sample transmitted per lane). The parameter K is a number of 'frames' of sample data bundled into a multiframe of length K frames, and this sets the period of the SYSREF clock signal. The TSW14J56 capture card (or other FPGA receiving JESD204B serial sample data from the EVM) must be configured with the same parameters as the ADS54J54.

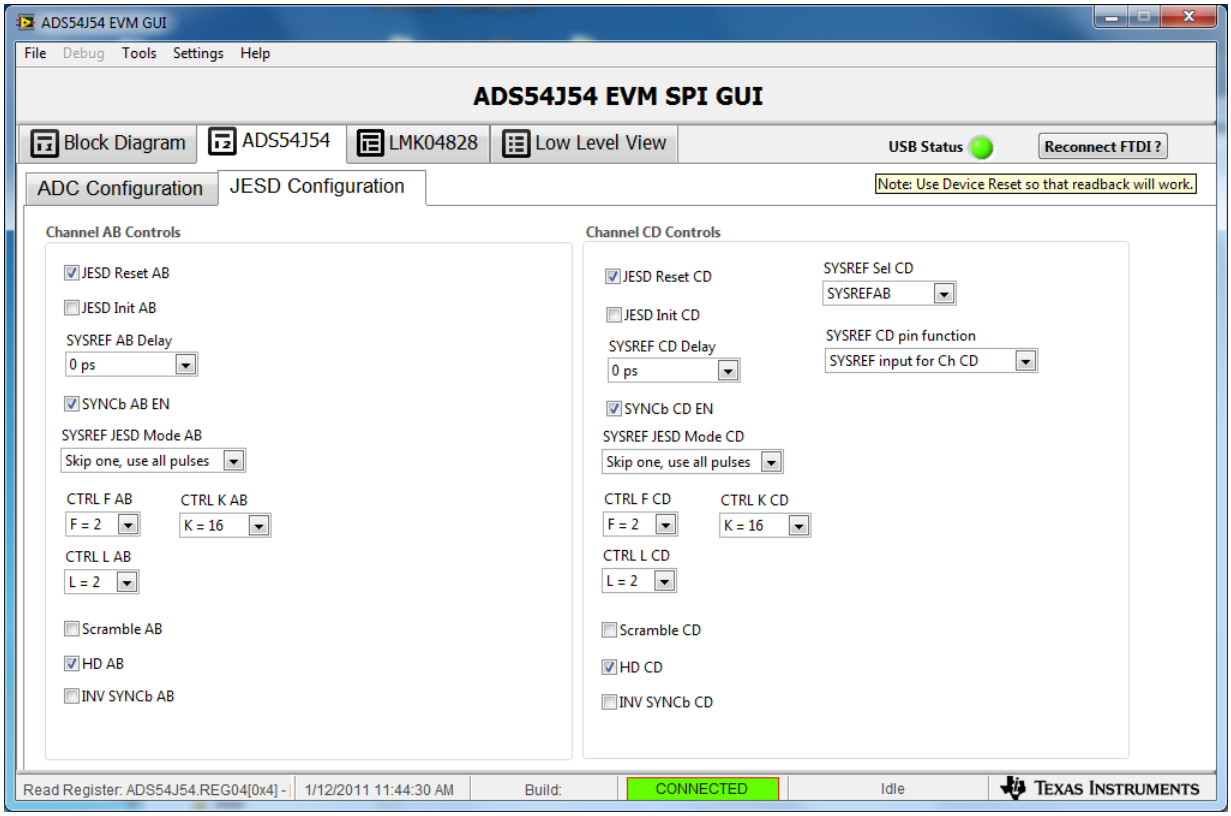

Figure 4. JESD204B Configuration Tab

2.2.4 LMK Controls

Click the *LMK04828* tab located in the top tab bar of the GUI. The bank of LMK04828 control tabs is selected as shown in Figure 5. There are four lower level tabs for control of the LMK04828. The LMK04828 is a dual-PLL clock device so there is a tab for setting controls for the first PLL and a tab for setting controls of the second PLL. There is a tab for setting controls related to the programming of the JESD204b SYSREF and SYNC signals. There is a tab for individual control of each of the 14 clock outputs of the LMK04828. The first PLL is represented in the PLL1 Configuration tab. The first PLL essentially takes a low-frequency reference and multiplies this up to an internal reference frequency. The second PLL has a very clean narrow-bandwidth VCO of either 2.5 or 3.0 GHz that is locked to the internal reference frequency from PLL1 and from this VCO the output clocks are generated.

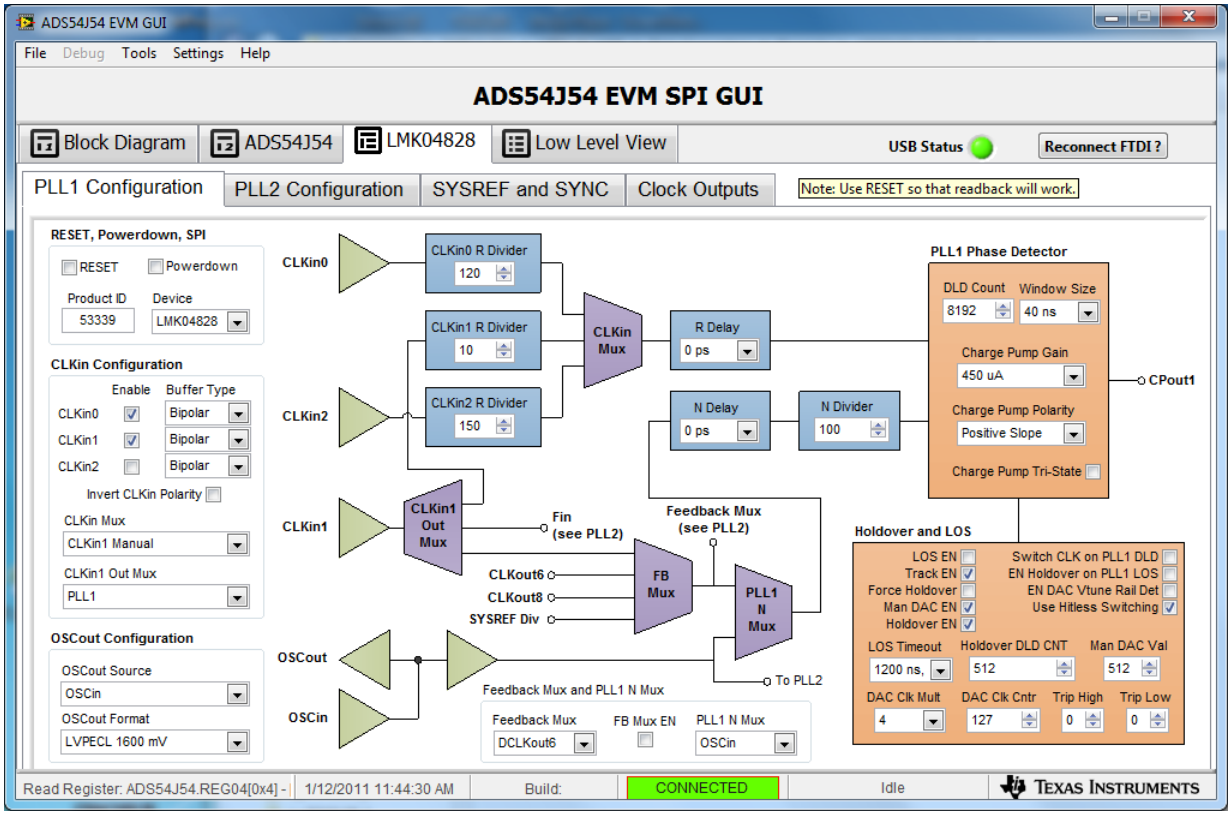

Figure 5. LMK04828 PLL1 Configuration Tab

2.2.4.1 PLL1 Configuration

Much of this panel is organized in block diagram format to help visualize the function of the controls. The function of PLL1 is to take an external reference clock, such as the 10-MHz reference from an oscillator on the EVM, and generate a clean, low-jitter intermediate-frequency clock for use by the second PLL loop. There are numerous integer divider values that may be used to create this intermediate frequency from the external reference. This tab also contains the reset and power down controls for the whole LMK04828 device. Consult the LMK04828 data sheet (SNAS605) and design tools for more information regarding the proper settings for configuring PLL1, particularly for the proper settings for the PLL1 phase detector and charge pump values.

2.2.4.2 PLL2 Configuration

Clicking *PLL2 Configuration* opens the PLL2 Configuration tab as shown in Figure 6. Much of this panel is organized in block diagram format to help visualize the function of the controls. In this tab there is the control to select whether an external VCO is used or an internal VCO of frequency 2.5 GHz or 3.0 GHz. Several integer divider ratios can be set to lock the VCO to the frequency from PLL1, labeled as OSCin. After configuring PLL2 to select a VCO and locking it to the input reference resulting in the desired VCO frequency, this VCO frequency is then used to generate 14 clock outputs which are normally used as 7 pairs of device clock and SYSREF system reference clocks. One of the device clock/SYSREF pairs is connected to the FMC connector to source DCLK/SYSREF to the FPGA on the TSW14J56 capture card. Another DCLK/SYSREF pair is used to clock the ADS54J54. The other 5 pairs of clocks are normally powered down but may be configured as additional clock outputs. The block diagram at the bottom of the PLL2 Configuration tab illustrates some of the operations that might be applied to the 7 DCLK/SYSREF pairs, such as divider ratios or delay adjustments. The next two tabs provide the controls to select all these available features that may be used to condition the DCLK/SYSREF pairs for a specific use. The LMK04828 datasheet is indispensable in understanding the function of each of these many controls and how these controls should be set for a specific use of the EVM.

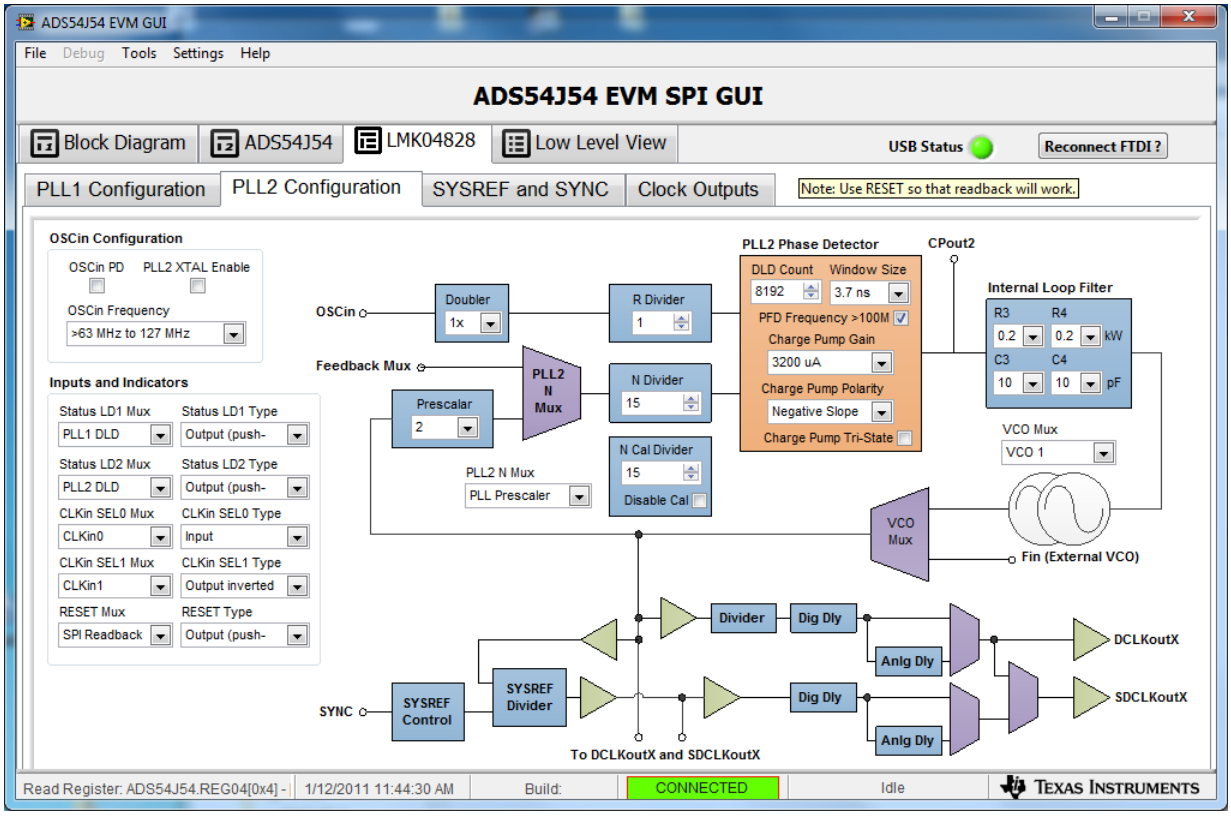

Figure 6. LMK04828 PLL2 Configuration Tab

2.2.4.3 Clock Output Controls

Clicking *Clock Outputs* opens the LMK04828 Clock Outputs tab, shown in Figure 7. This tab is organized into 7 sections representing the 7 pairs of DCLK/SYSREF that the LMK04828 can generate. For each of the 7 pairs of DCLK/SYSREF, there are a number of controls that apply to both outputs, such as the option to power down the pair of signals completely, if not needed. For both DCLK and SYSREF, there is an option to select what type of output driver is to be used, such as LVDS or LVPECL. There are controls to enable things like delay or inversion. For the DCLK, there is a control to select a divider ration to divide the PLL2 VCO clock down to the desired output frequency. For example, if the ADS54J54 EVM is to be operated at 500 Msps, then the configuration file supplied with the GUI will select the 3.0-GHz VCO and select a divider ratio of 6 to generate a 500-MHz DCLK. If the TSW14J56 capture card is used, the TSW14J56 needs to see a DCLK reference that is one-twentieth the line rate of the serial data stream so the divider ratio chosen is 12 to generate a 250-MHz DCLK to the FMC connector. These two divider ratios can be seen in Figure 7.

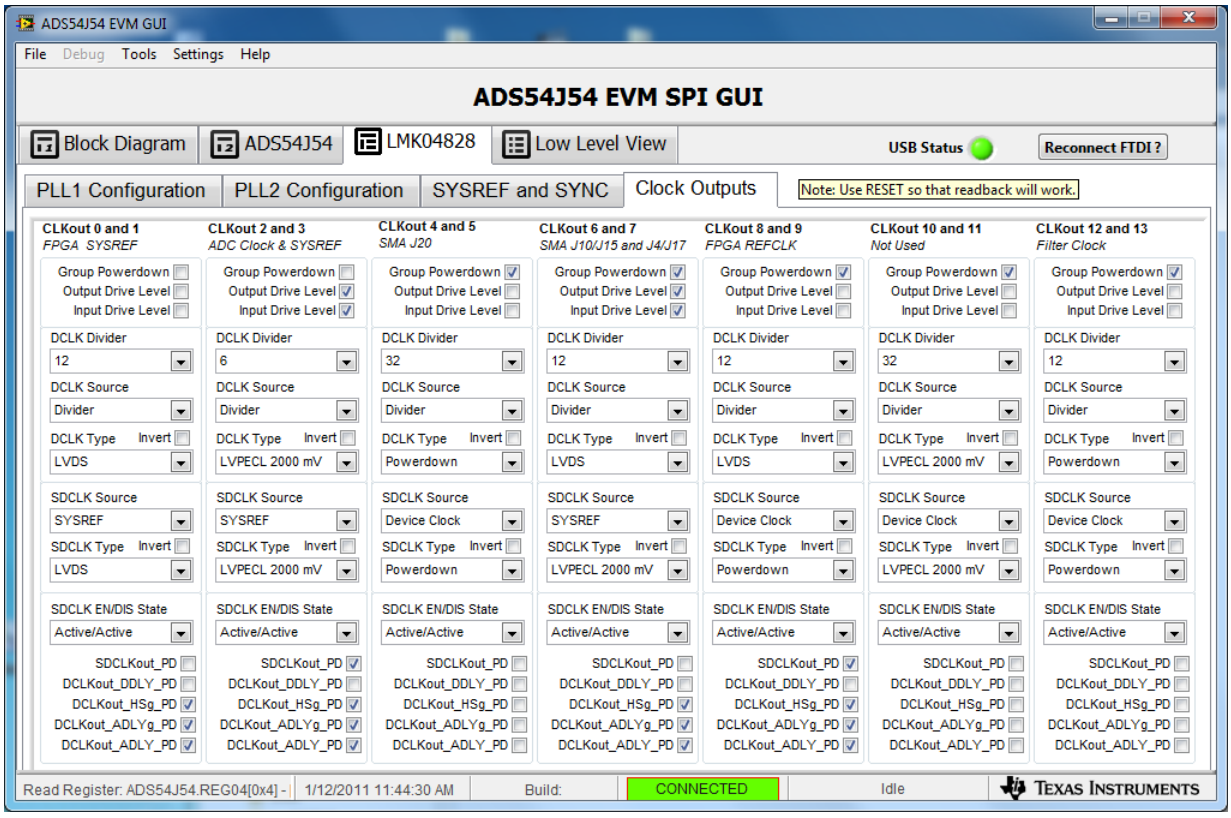

Figure 7. LMK04828 Clock Outputs Tab

2.2.4.4 SYSREF and SYNC Controls

Clicking *SYSREF and SYNC* opens the LMK04828 SYSREF and SYNC tab, shown in Figure 8. This tab has controls specific to the generation of the SYSREF outputs of the LMK04828. Along the top of the tab are controls that are common to all 7 of the SYSREF outputs, such as the SYSREF divider. Once the JESD204B link is configured for a specific line rate and all JESD204B parameters such as L, M, F, and K are chosen, then the SYSREF divider should be set to match the SYSREF rate to the Local MultiFrame Clock period, or LMFC period. For the default configuration of the ADS54J54 EVM as configured by the ADS54J54_500M_LMF881 config file, the device is set up for 2 lanes per channel, 1 octet per lane, with a K value of 32. The resulting SYSREF divider value is 1920 as shown in Figure 8, matching the SYSREF rate to the LMFC rate of the ADS54J54 and TSW14J56 capture card configurations. Along the bottom of the tab are controls that are specific to each of the 7 SYSREF outputs, such as delay settings.

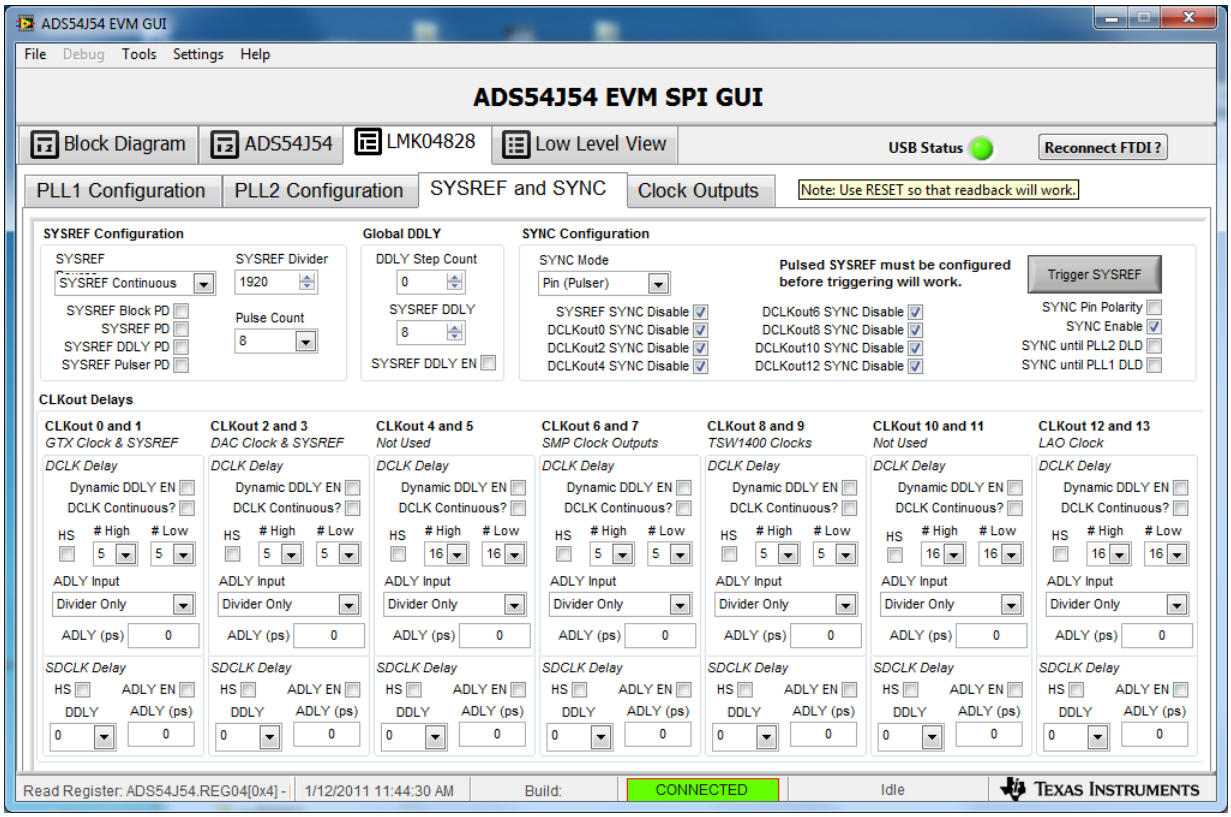

Figure 8. LMK04828 SYSREF and SYNC tab

2.2.4.5 Low Level View

Clicking *Low Level View* opens the ADS54J54 EVM SPI GUI Low Level View tab, shown in Figure 9. This tab allows for direct read/write access to each bit of each SPI address for both the ADS54J54 and the LMK04828. This is also the tab used to load a previously saved configuration file or to save a new configuration file once a specific EVM configuration is properly set up. There are several ways to accomplish a read or write to a specific register. Highlighting a particular *Register Name* will cause the bits of that register to display on the right side of the window. If there is a bit in that register that has a datasheet definition, then that definition is shown in the GUI. In the example shown in the figure, bit 4 of address 0x00 is the bit to choose between 3-wire SPI or 4-wire SPI for the LMK04828. To set a bit to a '1', check the box for that bit in the W column, then click *Write Register*. The GUI will write that register and then immediately read back that register. If the write was successful, then the R column should reflect what was just written from the W column. Another way to do an SPI access is to enter the address in the *Address* control at the bottom of the window and then click the *Write Register* or *Read Register* below it. Be sure to select the correct 'Block' first. If there are more than one devices with SPI access such as on this EVM, then there is a 'Block' for each device. The ADS54J54 EVM SPI GUI has a *Block* of ADS54J54 addresses and a *Block* of LMK04828 addresses.

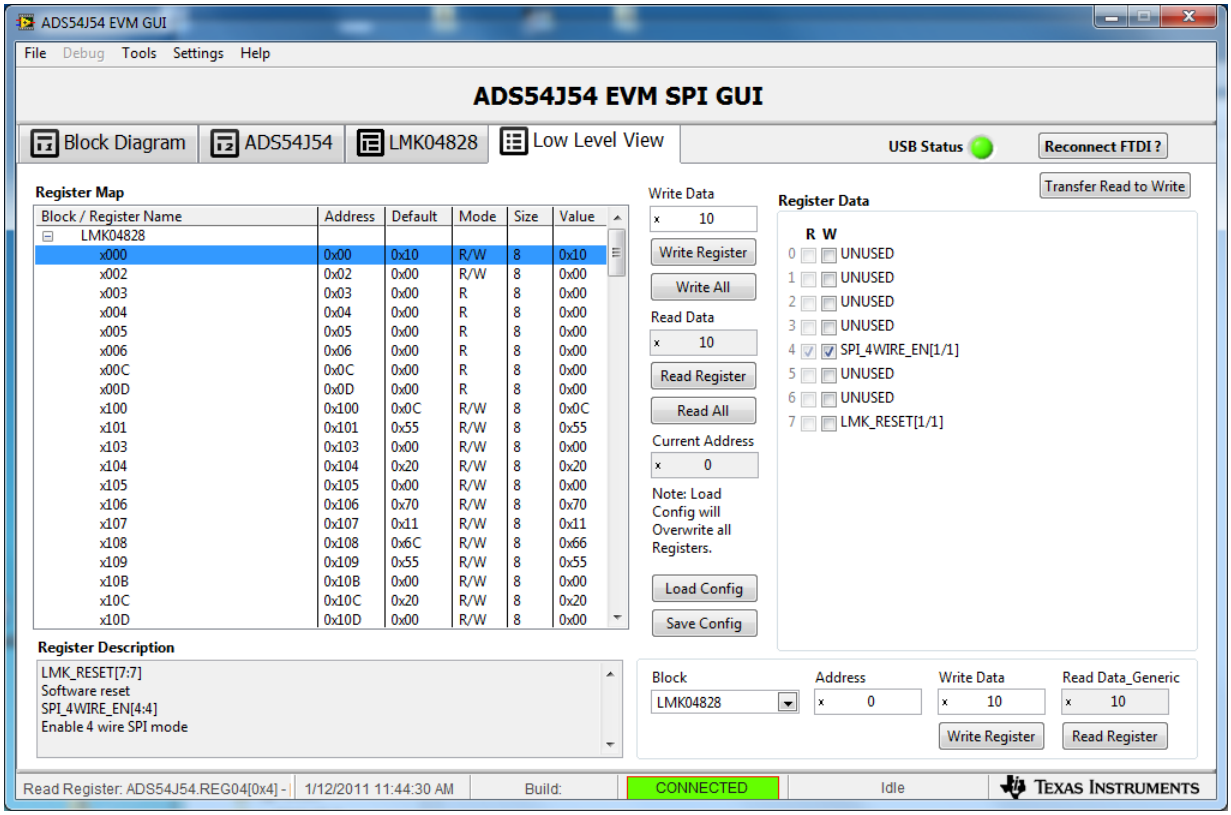

Figure 9. Low Level Controls Tab

3 Basic Test Setup

This section outlines basic testing of the ADS54J54EVM.

3.1 Test Block Diagram

The test setup for the ADS54J54EVM is shown in Figure 10. The TSW14J56 Capture Card is used to capture data from the ADS54J54 EVM, which is then transferred to the computer for analysis in the HSDC Pro software. The analog signal into a channel of the ADS54J54 can be from any high-quality low-jitter analog signal source. The clock source is from the LMK04828, but the board provides an option to use an external clock source, such as a HP8644B for the ADC sample clock. Note that a narrow bandpass filter is recommended on the analog source, which is necessary to remove as much phase noise from the signal source so as to achieve the best performance. The performance can be increased using external clock mode as this allows for the use of a filter on the clock source.

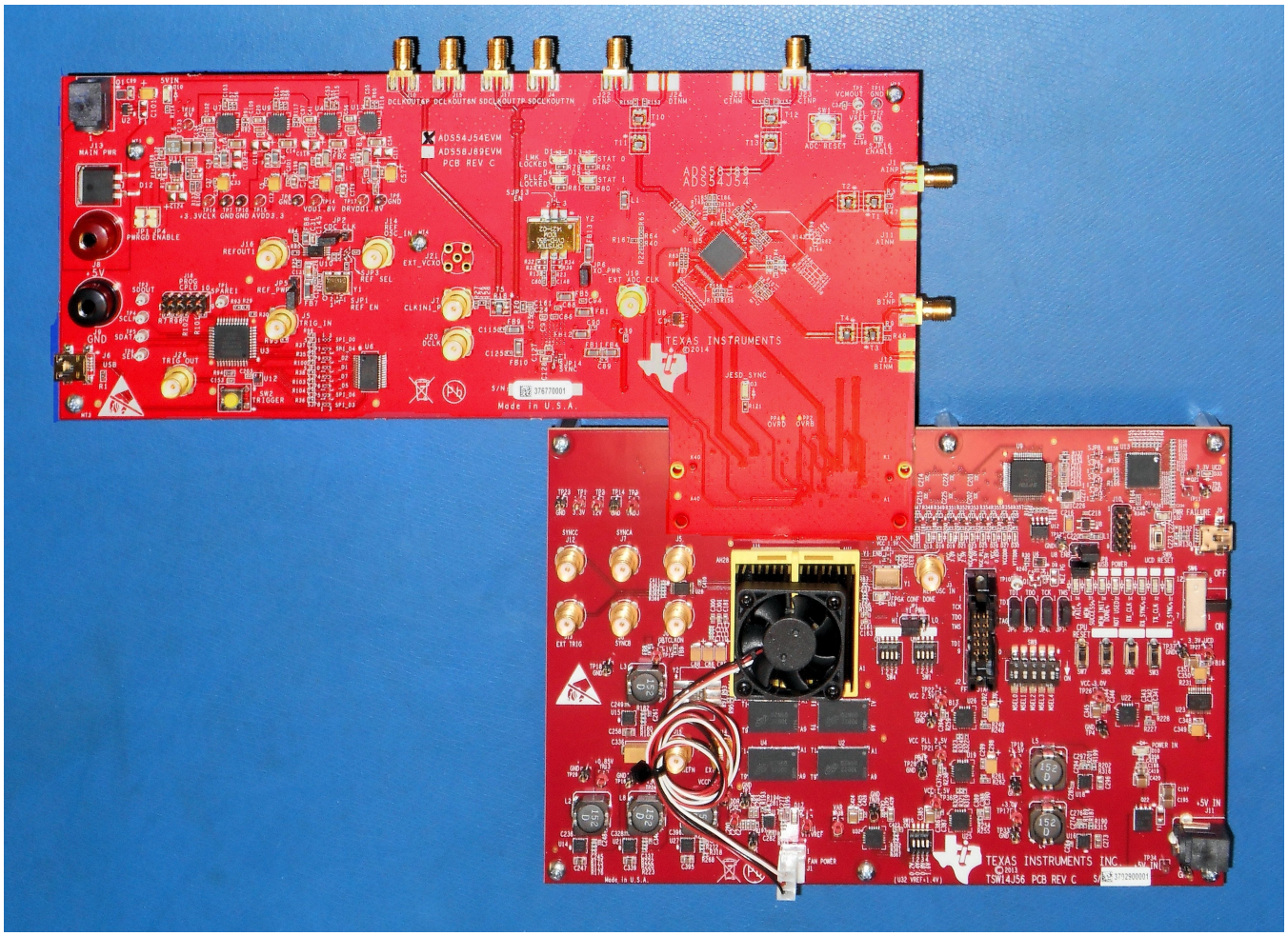

Figure 10. Test Setup

3.2 TSW14J56EVM Setup

See the TSW14J56EVM User's Guide (SLWU086) for a more detailed explanation of the TSW14J56 setup and its features. This document assumes that the HSDC Pro software and the TSW14J56 pattern capture and generation board are both installed and functioning properly. This information can be found at http://www.ti.com/tool/tsw14j56evm.

3.3 ADS54J54EVM Quick-Start Procedure

Connect J3 of a ADS54J54EVM into J4 of a TSW14J56 JESD204B capture card.

3.3.1 TSW14J56 Data Capture Card

1. Connect a 5-V power supply to connector *J11* of the TSW14J56EVM.
2. Flip switch *SW6* to the *ON* position.
3. Insert a USB cable into the USB port on the TSW14J56. Connect the other end to the PC.

3.3.2 ADS54J54EVM

1. Connect a bench 5-V power supply, or equivalent, to the connector J13 using the supplied power supply cable. Alternatively, power may be supplied to the EVM by way of the red banana jack J8 for +5 V and the black banana jack J9 for ground.
2. Connect a USB cable to the USB port on the ADS54J54EVM and connect the other end to the PC.
3. Connect a signal source to an analog input SMA connector such as J1 (*A_INP*). For single-tone testing, a bandpass filter should be used to achieve the best SNR and harmonic performance.

3.3.3 ADS54J54 GUI

Use the following steps for setting up the ADS54J54 GUI:

1. Start the ADS54J54 EVM GUI by selecting **Start Menu → Program Files → Texas Instruments ADCs → ADS54J54 EVM GUI**.
2. In the upper right-hand corner, there is either a red or green LED indicator labeled **USB Status** and a button labeled **RECONNECT FTDI?**. If the LED button is red, then click the button until the LED indicator turns green. This indicates that the ADS54J54EVM is connected to the computer.
3. Under the ADC Controls tab of the ADS54J54 tab, click on the **Reset ADC** button. The ADS54J54 EVM SPI GUI always does a read-back of every register write to verify that the desired value was written. The ADS54J54 powers up in 3-wire SPI mode while the GUI requires 4-wire mode for the readback function to work properly. The **Reset ADC** button will reset the ADC and set the device in 4-wire mode so that the GUI will continue to work properly.
4. Under the PLL1 Controls tab of the LMK04828 tab, click on the **Reset LMK** button. The LMK04828 powers up in 3-wire SPI mode while the GUI requires 4-wire mode for the readback function to work properly. The **Reset LMK** button will reset the LMK04828 and set the device in 4-wire mode so that the GUI will continue to work properly.
5. On the low-level tab, click the **Load Config** button. Choose one of the configuration files available. If choosing ADS54J54_500M_442.cfg, this configuration file will set the ADS54J54 to use four JESD204B lanes and set up the 2x decimation filter to output 250 Msps while the LMK04828 is configured to provide a 500-MHz device clock to the ADS54J54. If choosing ADS54J54_500M_881.cfg, the ADS54J54 will not decimate the sample output to 250 Msps but will output 500 Msps on 8 JESD204B lanes.
6. The two PLL's of the LMK04828 should now be locked. This is indicated on the ADS54J54 circuit board by the illuminated LED's, D4 (PLL2 LOCKED) and D1 labeled (LMK LOCKED).
7. The TSW14J56 capture card should now be receiving a DEVICE clock and a SYSREF clock. This causes the receiver FPGA to assert the JESD204B SYNC high, since synchronization has not been established with the transmitter ADC. This is indicated by LED D3 (JESD_SYNC) illuminating on the ADS54J54EVM. The SYSREF signal can be observed on either SMA J4 or J17 of the ADC EVM.
8. The TSW14J56 capture card should now be receiving valid data.
9. Since a periodic SYSREF signal acts as a sub-harmonic clock of the converter sampling clock and may have spurious effect on the converter performance, it may be turned off during normal operation once synchronization has been achieved. Click on the tab labeled *LMK0428 Clock Outputs* located at the top of the GUI. Check the control for SDCLKout_PD in the block of controls for clocks CLKout 2 and 3. (See Figure 8) This will power down the SYSREF to the ADS54J54. The SYSREF must be running initially in order to establish a JESD204B link between the ADS54J54 and the FPGA on the TSW14J56 but after initialization, the SYSREF is no longer needed and may result in clock spurs coupling into the ADS54J54, reducing performance.

NOTE: If SYSREF is turned off during normal operation, TX and RX devices must have the ability to generate a *Generate SYSREF* request to the LMK04828 clock generator whenever a synchronization request is detected at the SYNC interface.

10. If the JESD204B link does not get established, make sure the SYSREF MUX panel on the ADS54J54 GUI is set to SYSREF CONTINUOUS. If this is set to any other value, the SYSREF outputs will be disabled from the LMK04828, thus preventing synchronization from occurring.

3.3.4 High Speed Data Converter Pro (HSDC Pro)

1. Start the HSDC Pro software tool by selecting **Start Menu → All Programs → Texas Instruments ADCs → High Speed Data Converter Pro**.
2. When prompted for the serial number of the board, select the serial number that represents the TSW14J56 that has been connected to the ADS54J54. This number is on a sticker on the TSW14J56 board.
3. In the *Select ADC* drop-down box, select *ADS54J54_LMF442*. If it asks to download the firmware, select *Yes*. Multiple LEDs light up on the TSW14J56, once the firmware has finished downloading.
4. Select *Single Tone* from the *Test Selection* drop-down menu.
5. At the bottom-left corner, enter *250M* in the *ADC Output Data Rate* box. If not using an external 10-MHz syncing signal from the analog signal source, then the 500-MHz sample clock from the LMK04828 will not be coherent with the analog signal generator. In this case, do not select *Auto Calculation of Coherent Frequencies*. If the clocks are synchronized with an external 10M syncing signal and are to be coherent, then select *Auto Calculation of Coherent Frequencies*.
6. If a windowing function is desired, then *Blackman* should be selected above the plot window. If the clocks are synchronized with an external 10M syncing signal and coherent, select *Rectangular*.
7. All boards and software are now setup. Click the **Capture** button. A sample capture is shown in Figure 11 for the ADS54J54 with a 250-MHz clock and 170-MHz input frequency.

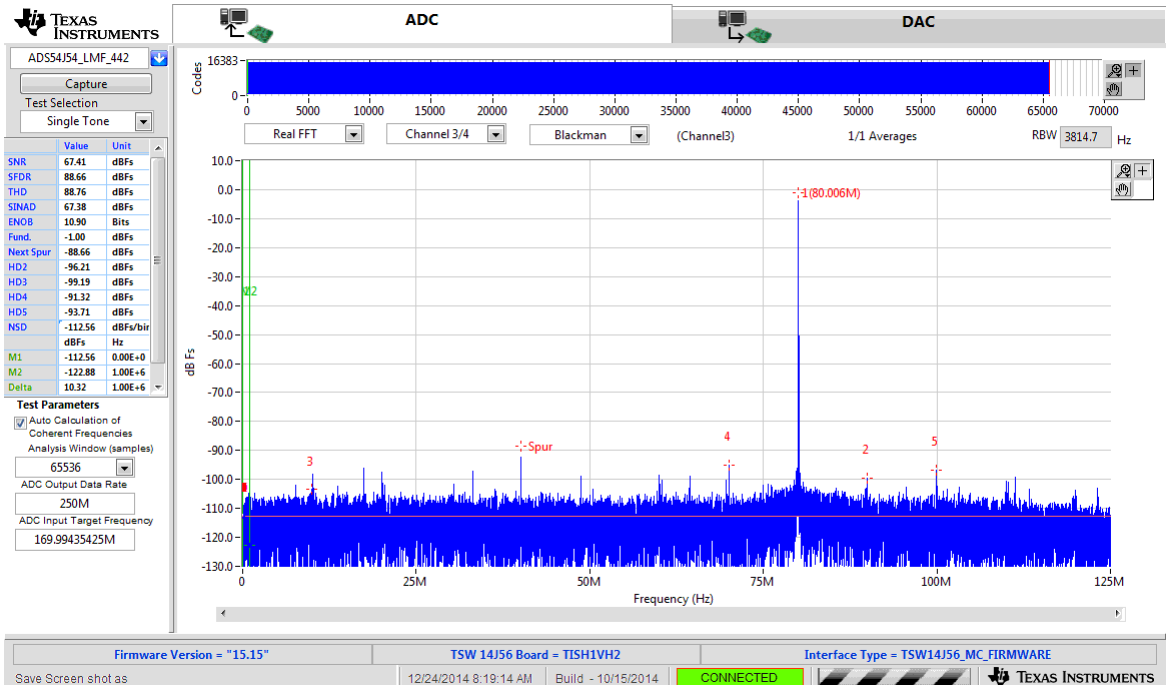

Figure 11. High Speed Data Converter Pro (HSDC Pro) Sample Capture

Revision History

Changes from Original (January 2015) to A Revision **Page**

- Changed first paragraph by removing reference to an included 5-VDC power supply to *a cable for connection to an external 5-VDC power supply*. 1
- Changed *Block Diagram of the ADS54J54EVM* image. 2
- Changed the description in the *Input and Output Connectors and Jumper Descriptions of the ADS54J54EVM* table for *J13 (Main PWR)* from a *provided 5-VDC power supply*, to *+5-V bench supply (cable supplied)*. 3
- Changed list item one in the *ADS54J54EVM* section. 15

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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      3.1.1 *Notice applicable to EVMs not FCC-Approved:*

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      CAUTION

      This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

      Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

      FCC Interference Statement for Class A EVM devices

      NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

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- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

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Concernant les EVMs avec antennes détachables

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