

TI Precision Designs: Verified Design

18-Bit, 1-MSPS Data Acquisition (DAQ) Block Optimized for Lowest Power



TI Precision Designs

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Design Resources

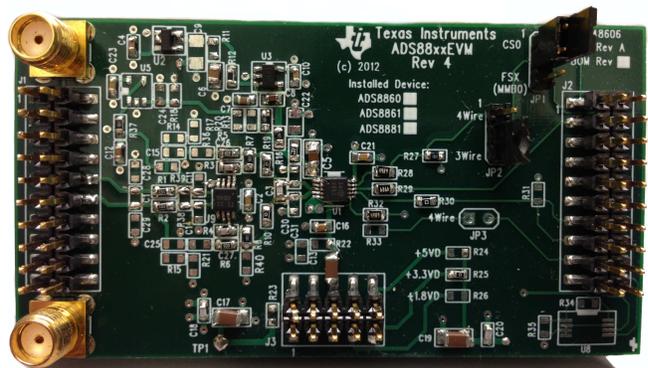
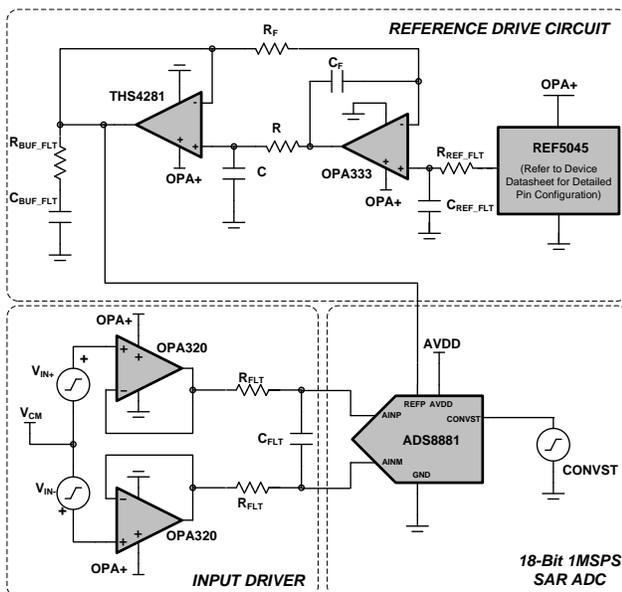
TIPD113	All Design Files
TINA-TI™	SPICE Simulator
ADS8881	Product Folder
OPA2320	Product Folder
REF5045	Product Folder
OPA2333	Product Folder
THS4281	Product Folder
REF6045	Product Folder

Circuit Description

This circuit describes a data acquisition (DAQ) block comprising an 18-bit successive-approximation-register (SAR) analog-to-digital converter (ADC), front-end driver circuit for inputs of the ADC, an external reference, and driver circuit for the ADC reference input. This design has been optimized to achieve good dynamic performance for the lowest power consumption using a full-scale sinusoidal input signal of frequency 10 kHz. The differential input signal is processed through low noise and low power amplifiers configured as unity-gain buffers and a low-pass RC filter before being fed into the ADC.



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1 Design Summary

The primary objective for this TI Design is to design an optimized data acquisition (DAQ) system, which achieves superior AC performance at the lowest power consumption using the 18-bit ADS8881 at 1 MSPS, for a full-scale sinusoidal input signal of frequency 10 kHz. The design requirements for this block are:

- System supply voltage, OPA+: 5-V DC
- ADC supply voltage, AVDD: 3.3-V DC
- ADC sampling rate: 1 MSPS
- ADC reference voltage (V_{REF}): 4.5-V DC
- ADC input signal: Differential sinusoidal signals with amplitude of $V_{PK} = 4.3\text{ V}$ (-0.4 dBFS to avoid clipping) and frequency, $f_{IN} = 10\text{ kHz}$ are applied to the inputs of the ADC

The design goals and performance are summarized in [Table 1](#). The AC performance for this DAQ block is measured using TI's ADCPro™ tool as [Figure 1](#) shows.

Table 1. Comparison of Design Goal, Simulation, and Measured Performance

PARAMETER	GOAL	SIMULATED	MEASURED
Total power (mW)	< 35	NA ⁽¹⁾	28.61
Signa-to-noise ratio – SNR (dB)	≥ 98	NA ⁽²⁾	98.97
Total harmonic distortion – THD (dB)	≤ –105	NA ⁽²⁾	–105.64
Signa-to-noise and distortion ratio – SINAD (dB)	≥ 98	NA ⁽²⁾	98.12
Effective number of bits – ENOB	16	NA ⁽²⁾	16.01

⁽¹⁾ Power consumption for SAR ADC is not accurately modeled in the TINA-TI™ models

⁽²⁾ ADC dynamic performance is not simulated as TINA-TI™ models for SAR ADC do not include the noise and distortion information.

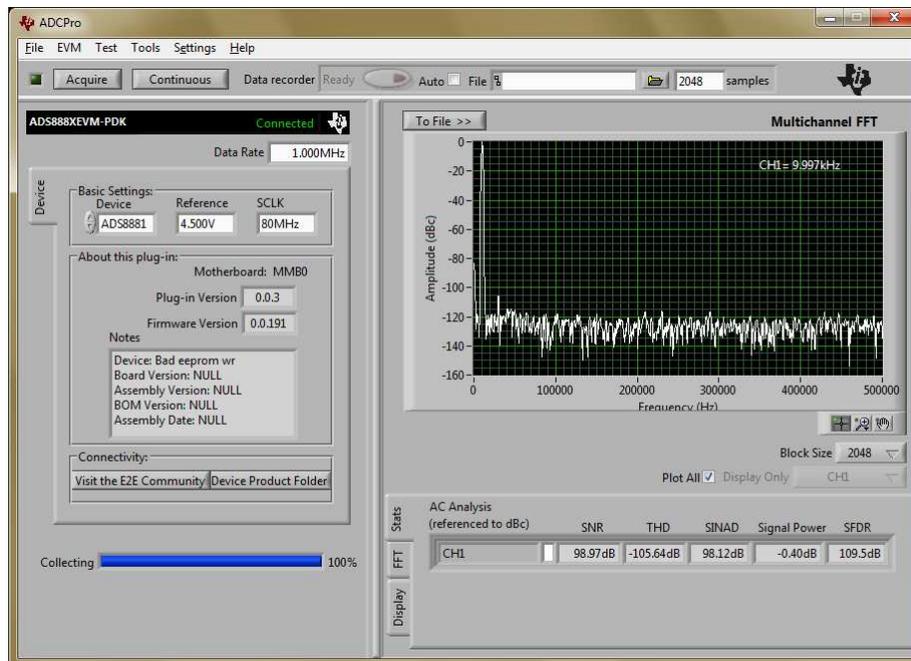


Figure 1. Measurement Data—AC Performance of DAQ Block Using ADCPro™

2 Theory of Operation

The two primary design considerations to maximize the performance of a high-resolution SAR ADC are the input driver and the reference driver. Figure 2 shows a block diagram comprising the critical analog circuit blocks, which must be carefully designed to achieve the design specifications of an 18-bit 1 MSPS DAQ block. The diagram includes the most important specifications for each individual analog block in the order of design priority. These individualized specifications are important because the design criteria for each block is dependent on the desired ADC performance as well as the input signal type.

This design uses an 18-bit SAR ADC at a throughput of 1 MSPS and it has been optimized for a differential full-scale sinusoidal input signal of 10-kHz frequency. Adhere to the following design steps to meet the performance goals of this design:

1. Select an appropriate amplifier with sufficient small-signal bandwidth and low power, which minimally degrades the noise and distortion performance of the ADC.
2. Design a low-pass anti-aliasing RC filter to band-limit the noise contribution from the front-end circuitry while paying attention to the stability of the driving amplifiers.
3. Design a high-precision reference driver circuit, which provides the required value of V_{REF} with low offset, drift, and noise contributions.

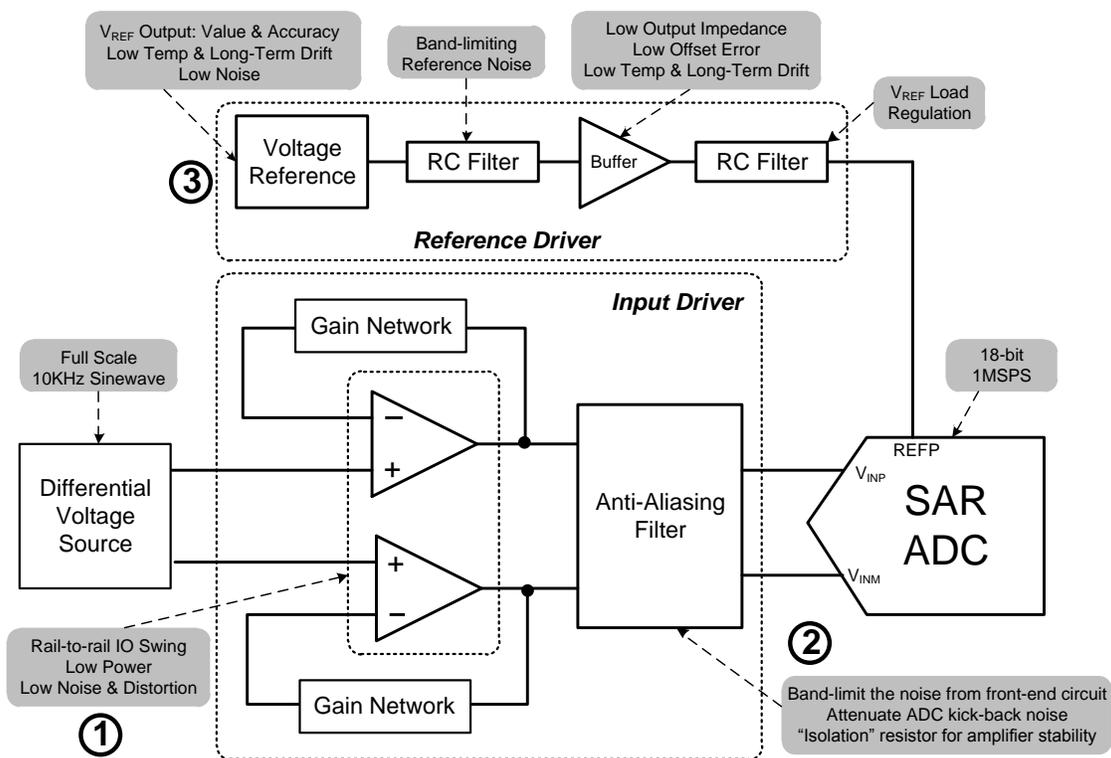


Figure 2. Block Diagram Highlighting Primary Design Criteria for DAQ Block

2.1 Understanding ADC Dynamic Performance

In this TI Precision Design, the primary focus is to achieve excellent dynamic performance out of the DAQ block for a pure sinusoidal input while minimizing the total power consumption of the system. The main AC specifications under consideration for this design are THD, SNR, SINAD, and ENOB. All of these parameters are essentially different ways of quantifying the noise and distortion performance of an ADC based on a fast-Fourier transform (FFT) analysis. shows a typical FFT plot for an ADC.

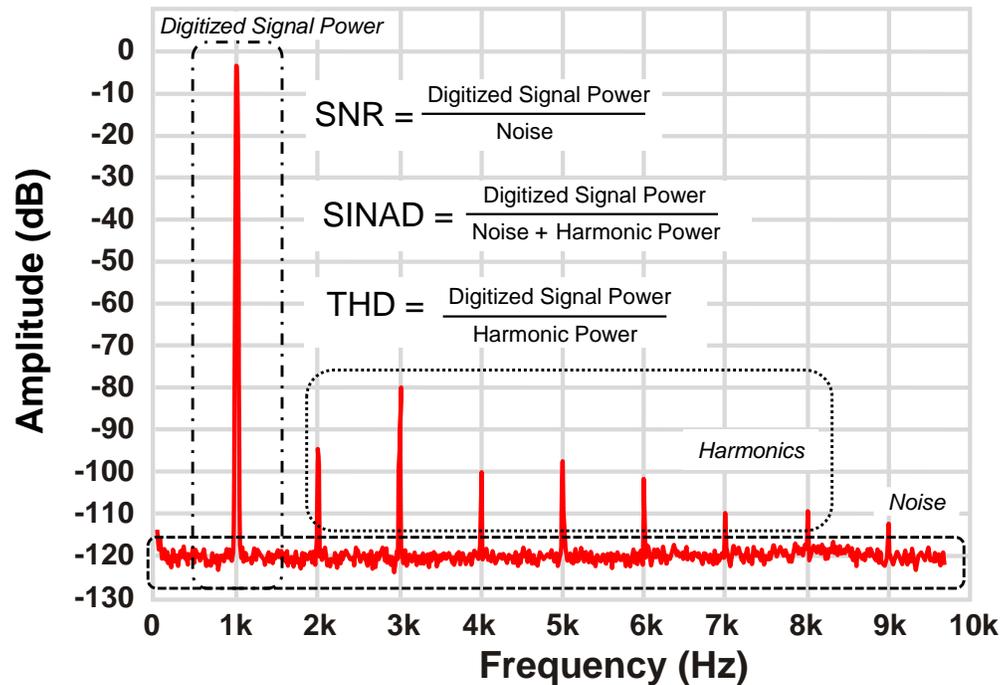


Figure 3. Typical FFT Plot for DAQ System

Total harmonic distortion (THD) is defined as the ratio of the root-sum-square (RSS) of all harmonic components (generally nine harmonics are used) to the power of the fundamental signal frequency. The THD is generally specified with an input signal near full-scale (FS); however, in this design the input is kept 0.4 dB below FS to prevent clipping of the analog front end. If the RMS value of the input signal is denoted as V_{SIG_RMS} and the power in n^{th} harmonic is denoted by $V_{HAR_n_RMS}$, then the total harmonic distortion ($V_{HAR_TOT_RMS}$) and THD can be calculated in Equation 1 as:

$$V_{HAR_TOT_RMS} = \sqrt{V_{HAR_1_RMS}^2 + V_{HAR_2_RMS}^2 + \dots + V_{HAR_9_RMS}^2}$$

$$THD = \frac{V_{SIG_RMS}}{V_{HAR_TOT_RMS}} \quad (1)$$

The signal-to-noise ratio (SNR) provides insight into the total noise of the system. The total noise of the DAQ system is the RSS of the front-end amplifier noise ($V_{n_AMP_RMS}$) and the ADC noise ($V_{n_ADC_RMS}$). The ADC noise includes the quantization noise as well as the noise contributed by the ADC internal circuitry or the *input-referred noise* of the ADC. The total noise contributions from all of these sources, denoted as $V_{n_TOT_RMS}$ are referred to the input of the ADC for calculating the total SNR of the system (SNR_{SYS} in Equation 2).

$$V_{n_TOT_RMS} = \sqrt{V_{n_AMP_RMS}^2 + V_{n_ADC_RMS}^2}$$

$$SNR_{SYS} = \frac{V_{SIG_RMS}}{V_{n_TOT_RMS}} \quad (2)$$

The signal-to-noise and distortion ratio (SINAD) combines the effect of distortion and noise to provide a cumulative measure of the overall dynamic performance of the system (see Equation 3).

$$\text{SINAD}_{\text{SYS}} = \frac{V_{\text{SIG_RMS}}}{\sqrt{V_{n_TOT_RMS}^2 + V_{\text{HAR_TOT_RMS}}^2}} \quad (3)$$

The effective number of bits (ENOB) is an effective measurement of the quality of a digitized signal from an ADC by specifying the number of bits above the noise floor. For an ideal N-bit ADC with only quantization noise, the SNR (in dB) can be calculated in Equation 4 as:

$$\begin{aligned} \text{SNR} &= 6.02 \times N + 1.76 \\ \Rightarrow N &= \frac{\text{SNR} - 1.76}{6.02} \end{aligned} \quad (4)$$

Equation 4 can be used to define the ENOB for a system, as Equation 5 shows. The expression for ENOB is a better indication of the overall dynamic performance of the DAQ block if the SNR is substituted with $\text{SINAD}_{\text{SYS}}$.

$$\text{ENOB} = \frac{\text{SINAD}_{\text{SYS}} - 1.76}{6.02} \quad (5)$$

While ENOB provides a good summary of the ADC dynamic performance, it does not describe the entire performance of the converter over the operating frequency ranges and input signals. Additionally, ENOB does not include the ADC DC specifications such as offset and gain error. Hence, paying attention to other converter specifications as well is important depending on the application in which the ADC is being used.

2.2 Input Driver Design

2.2.1 Input Amplifier Design

The analysis explained in Section 2.1 makes it clear that it is important to keep the noise and distortion contribution from the front-end circuit at an extremely low-level to maximize the performance of a high-precision ADC. However, as the primary objective for this TI Design is to minimize power consumption of the system, it is extremely important to first select an appropriate low-power amplifier with sufficiently low noise and distortion for the input driver circuit. The effect of front-end circuit noise on the overall system performance is explained in the following analysis in Section 2.2.1.1.

2.2.1.1 System Noise Analysis

This subsection analyzes the effect of noise from the front-end circuitry on the overall dynamic performance of a high-precision ADC. For simplification purposes, this analysis has been done for a single-ended input stage (refer to Figure 4). The same concept has been extended to differential input ADCs later in the design.

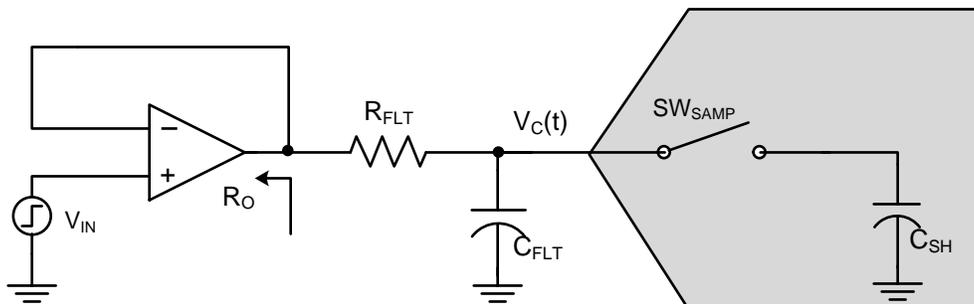


Figure 4. Simplified Schematic of Single-Ended ADC Input Stage

In the schematic in [Figure 4](#), the 3-dB bandwidth of the RC filter, denoted as BW_{RC} , is critical to band-limit the broadband noise contribution from the amplifier. Because the input drivers are configured as unity-gain buffers, only the noise from the amplifier contributes to the front-end noise. The amplifier noise is broadly categorized as low-frequency flicker or $1/f$ noise (0.1 Hz to 10 Hz) and higher frequency broadband noise, generally specified as a noise spectral density (e_{n_RMS}) over a wide frequency range.

Let the noise gain of the amplifier be denoted as N_G . Then the contribution of the amplifier broadband noise (V_{n_RMS}) referred to the ADC input is limited by the bandwidth of the RC filter, as [Equation 6](#) shows:

$$V_{n_RMS} = N_G \times e_{n_RMS} \times \sqrt{\frac{\pi}{2} \times BW_{RC}} \quad (6)$$

The flicker noise of the amplifier is specified as peak-to-peak noise (V_{1/f_AMP_PP}), which must first be converted to RMS noise followed by multiplication with the noise gain, N_G to calculate the flicker noise contribution (see [Equation 7](#)).

$$V_{1/f_AMP_RMS} = N_G \times \frac{V_{1/f_AMP_PP}}{6.6} \quad (7)$$

So, the total noise contribution from the front-end circuit for a single-ended system can be calculated by doing an RSS of the broadband and flicker noise contributions from the amplifier, as [Equation 8](#) shows.

$$V_{n_AMP_RMS} = N_G \times \sqrt{\left(\frac{V_{1/f_AMP_PP}}{6.6}\right)^2 + e_{n_RMS}^2 \times \frac{\pi}{2} \times BW_{RC}} \quad (8)$$

The same concept can be extended to differential input ADCs as well; the only difference is that for differential ADCs, both amplifiers driving the two inputs add noise to the system. So a factor of $\sqrt{2}$ is multiplied with the noise calculated in [Equation 8](#).

$$V_{n_AMP_RMS} = N_G \times \sqrt{2} \times \sqrt{\left(\frac{V_{1/f_AMP_PP}}{6.6}\right)^2 + e_{n_RMS}^2 \times \frac{\pi}{2} \times BW_{RC}} \quad (9)$$

However, the user should note that if the ADC front end provides some gain or attenuation to the input signal, then the thermal noise contribution of the resistors ($\sqrt{4kTR \times BW_{RC}}$) must also be accounted for in the overall noise calculation. In this expression, k is the Boltzmann's constant, T is the temperature in Kelvin, and R is the value of the resistor used in the front-end gain network.

For an ADC with an input full-scale range of V_{FSR} , the input-referred noise can be calculated from the specified value of SNR in the datasheet by using [Equation 10](#):

$$V_{n_ADC_RMS} = \frac{V_{FSR}}{2\sqrt{2}} \times 10^{-\frac{SNR(dB)}{20}} \quad (10)$$

So, to have a minimal impact on the SNR of the system, the total noise contribution from the amplifier must be kept at least five times less than the input-referred noise of the ADC (see [Equation 11](#)). This design criteria puts a maximum limitation on the bandwidth of the RC filter (BW_{RC}) for a particular amplifier with good noise specifications.

$$V_{n_AMP_RMS} \leq \frac{1}{5} \times V_{n_ADC_RMS} \quad (11)$$

For a differential input ADC, the values for the amplifier noise and RC filter bandwidth must satisfy the following criteria in [Equation 12](#):

$$N_G \times \sqrt{2} \times \sqrt{\left(\frac{V_{1/f_AMP_PP}}{6.6}\right)^2 + e_{n_RMS}^2 \times \frac{\pi}{2} \times BW_{RC}} \leq \frac{1}{5} \times \frac{V_{FSR}}{2\sqrt{2}} \times 10^{-\frac{SNR(dB)}{20}} \quad (12)$$

According to the expression in [Equation 12](#), the broadband noise density (e_{n_RMS}) of the amplifier must be kept as low as possible for maximum system performance. Also note that in most cases the flicker noise contribution is negligible compared to the broadband noise integrated over the bandwidth of the RC filter. A similar argument applies to the distortion contribution from the amplifier, which must also be kept extremely low; however, both noise and distortion come at a cost of burning more power in the amplifier. Hence, selecting the appropriate low power and low noise amplifier is the first step recommended for this system design. The other important amplifier specifications to be considered for making this selection are:

- **Rail-to-rail input and output swing** to support the full-scale sinusoidal signal at the ADC inputs.
- **Small signal bandwidth of the amplifier** must be as high as possible so that the feedback loop of the amplifier can correct for distortions at higher frequencies.

2.2.2 RC Filter Design

After selecting an appropriate amplifier for the design, the next step is to design an appropriate antialiasing RC filter at the inputs of the ADC. The bandwidth of the filter (BW_{RC}) should be kept low to band-limit the noise contribution from the front-end circuit, but it should be high enough to prevent any distortion in the input signal.

The capacitor C_{FLT} helps reduce the sampling charge injection at the ADC input and provides a charge bucket to quickly charge the input capacitor C_{SH} during the sampling process. The value of the capacitor C_{FLT} should be chosen such that when switch SW_{SAMP} closes, the voltage droop (ΔV_{FLT}) on C_{FLT} is less than 5% of the input voltage.

The charge required for the ADC sampling capacitor is given by [Equation 13](#):

$$Q_{IN} = C_{SH} \times V_{REF} \quad (13)$$

The charge supplied by the filter capacitor is given by [Equation 14](#):

$$Q_{FLT} = C_{FLT} \times \Delta V_{FLT} \leq C_{FLT} \times (0.05 \times V_{REF}) \quad (14)$$

By the principle of charge conservation, the charge required by the sampling capacitor should be equal to the charge provided by the filter capacitor. Hence, the following [Equation 15](#) can be derived:

$$\begin{aligned} Q_{IN} &= Q_{FLT} \\ \Rightarrow C_{FLT} \times (0.05 \times V_{REF}) &\geq C_{SH} \times V_{REF} \\ \Rightarrow C_{FLT} &\geq 20 \times C_{SH} \end{aligned} \quad (15)$$

At this point, understanding the trade-offs involved in selecting the values of C_{FLT} and R_{FLT} is important. If the value of C_{FLT} is high, it provides better attenuation against the charge-injection noise when the sampling switch closes. However, C_{FLT} cannot be made arbitrarily high because it degrades the phase margin of the driving amplifier, making it unstable. The series resistor R_{FLT} functions as an isolation resistor, which helps stabilize the driving amplifier, as explained in [\[1\]](#) and [\[2\]](#). A higher value of R_{FLT} is helpful from the amplifier stability perspective, but higher values of R_{FLT} add distortion due to interactions with the non-linear input impedance of the ADC. The distortion increases with source impedance, input signal frequency, and input signal amplitude; therefore, the selection of R_{FLT} requires a balancing of the stability and distortion of the design.

The minimum value for R_{FLT} is dependent on the output impedance of the amplifier and its stability requirements. If the output impedance of the driving amplifier is equal to R_O , a minimum value for R_{FLT} can be calculated to keep the amplifiers stable by evaluating the effect of R_O , R_{FLT} , and C_{FLT} on the amplifiers open-loop gain (A_{OL}) response as shown in [Figure 5](#). In this figure, the closed-loop response of the amplifier for a gain of 1 is denoted as A_{CL} and the unity-gain bandwidth is denoted as f_{CL} .

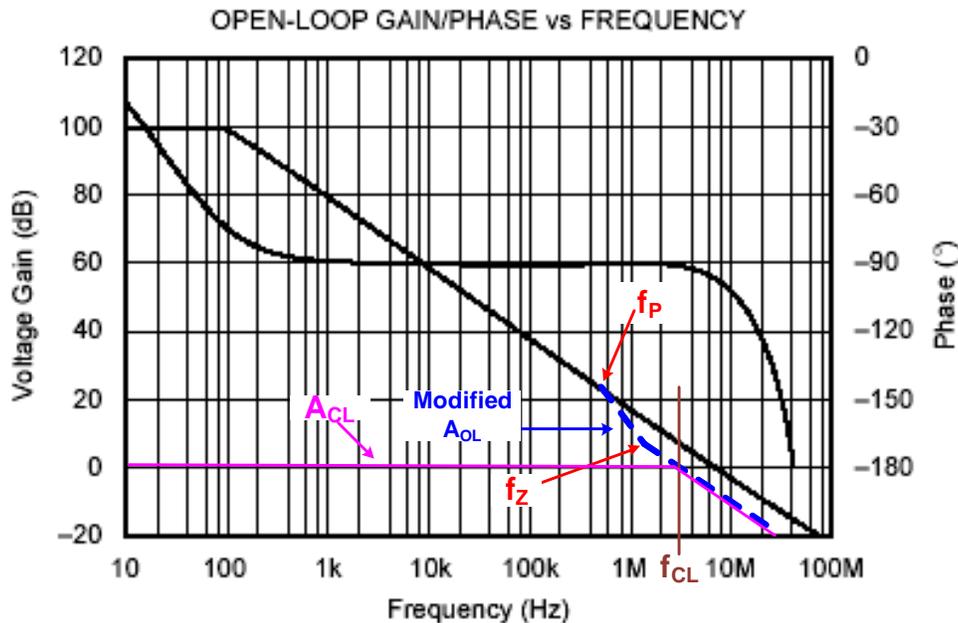


Figure 5. Analyzing Effect of RC Filter on Op Amp Stability Using A_{OL} Response

The combination of R_O , R_{FLT} , and C_{FLT} introduces one pole, f_p (Equation 16) and one zero, f_z (Equation 17) in the open-loop response of the amplifier, for which the corner frequencies are given in the following Equation 16 and Equation 17:

$$f_p = \frac{1}{2\pi(R_O + R_{FLT})C_{FLT}} \quad (16)$$

$$f_z = \frac{1}{2\pi R_{FLT} C_{FLT}} \quad (17)$$

To ensure that the phase change from the zero negates the phase change that the pole initiates, it is important that the frequency distance between the pole and zero must be less than or equal to one decade (see Equation 18).

$$\log\left(\frac{f_z}{f_p}\right) \leq 1 \quad (18)$$

Substituting Equation 16 and Equation 17 into Equation 18, the minimum value for R_{FLT} can be derived as:

$$R_{FLT} \geq \frac{R_O}{9} \quad (19)$$

In the interest of stability, the effects of f_z must occur at a frequency lower than the closed-loop gain bandwidth of the amplifier (f_{CL}). The reason for this specification is for stability of the amplifier circuit, for which the closure rate between the open- and closed-loop gain curves should not be greater than 20 dB per decade. To account for the fabrication process variations associated with the performance of the amplifier, a good practice is to choose f_z such that the closed-loop gain bandwidth of the amplifier, f_{CL} is at least twice the frequency of the zero (see Equation 20).

$$\frac{f_{CL}}{f_z} \geq 2 \quad (20)$$

Much of this discussion and subsequent results described in Section 3.1.2 and Section 4.1 related to op-amp stability are covered in detail in [1].

2.3 Reference Driver Design

External voltage reference circuits are used in a DAQ system if there is no internal reference in the ADC or if the accuracy of the internal reference is not sufficient to meet the performance goals of the system. These circuits provide low drift and very accurate voltages for ADC reference input. However, the output broadband noise of most references can be in the order of a few $100 \mu\text{V}_{\text{RMS}}$, which degrades the noise and linearity performance of precision ADCs for which the typical noise is in the order of tens of μV_{RMS} . So, to optimize the ADC performance, the output of the voltage reference must be appropriately filtered and buffered. Advances have also been made in this area, leading to the first available integrated reference and buffer and all-in-one chip with reference and buffer, which is further addressed in .

Figure 6 shows the basic circuit diagram for the reference driver circuit for precision ADCs.

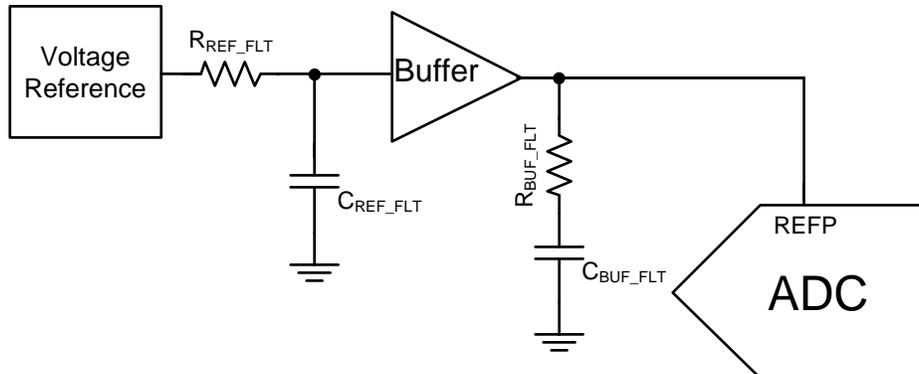


Figure 6. Simplified Schematic of Reference Driver Circuit

The reference noise can be divided into two major categories:

- Low frequency, peak-to-peak flicker or $1/f$ noise (V_{1/f_REF_pp}) from 0.1 Hz to 10 Hz
- Higher frequency broadband noise, generally specified as a noise spectral density ($e_{n_REF_RMS}$) over a wide range of frequency

The broadband output noise from the reference circuit is band-limited by the 3-dB cutoff frequency (f_{REF_3dB}) of an RC filter at the output. So, the primary objective for the filter design is to keep the bandwidth low enough such that the intrinsic noise from the reference does not degrade the performance of the ADC. For a high-precision ADC with an input dynamic range of V_{FSR} , the RMS value of input-referred noise can be calculated from the specified value of SNR in the datasheet by using Equation 21:

$$V_{n_ADC_RMS} = \frac{V_{FSR}}{2\sqrt{2}} \times 10^{-\frac{SNR(dB)}{20}} \quad (21)$$

Hence, the total integrated noise from the reference ($V_{n_REF_RMS}$) must be kept at least one-third of the ADC noise to prevent any degradation in the system performance, as Equation 22 shows:

$$V_{n_REF_RMS} \leq \frac{V_{n_ADC_RMS}}{3} \quad (22)$$

For an RC filter, the effective noise bandwidth is equal to the product of $\pi / 2$ and the 3-dB cutoff frequency. The value of total noise contribution from the reference circuit $V_{n_REF_RMS}$ is calculated by the RSS of the flicker noise and broadband noise, as Equation 23 shows:

$$V_{n_REF_RMS} = \sqrt{\left(\frac{V_{1/f_REF_pp}}{6.6}\right)^2 + e_{n_REF_RMS}^2 \times \frac{\pi}{2} \times f_{REF_3dB}} \quad (23)$$

Substituting Equation 21 and Equation 23 in Equation 22 results in Equation 24:

$$\sqrt{\left(\frac{V_{1/f_REF_pp}}{6.6}\right)^2 + e_{n_REF_RMS}^2 \times \frac{\pi}{2} \times f_{REF_3dB}} \leq \frac{1}{3} \times \frac{V_{FSR}}{2\sqrt{2}} \times 10^{-\frac{SNR(dB)}{20}} \quad (24)$$

The variation in the broadband noise density of the voltage reference ranges from 100 nV/ $\sqrt{\text{Hz}}$ to 10000 nV/ $\sqrt{\text{Hz}}$ depending on the reference type and power consumption. In general, the reference noise is inversely proportional to its quiescent current (I_{Q_REF}). Because broadband noise density is not always included in the voltage reference datasheet, an approximation of the noise density for band-gap reference circuits is provided in Equation 25.

$$e_{n_REF_RMS} \approx \frac{10000\text{nV}}{\sqrt{\text{Hz}}} \times \frac{1}{\sqrt{2 \times I_{Q_REF} (\text{in } \mu\text{A})}} \quad (25)$$

Equation 25 is derived on the basis of the measured characteristic between the output noise density and quiescent current of several TI reference circuits, as Figure 7 shows.

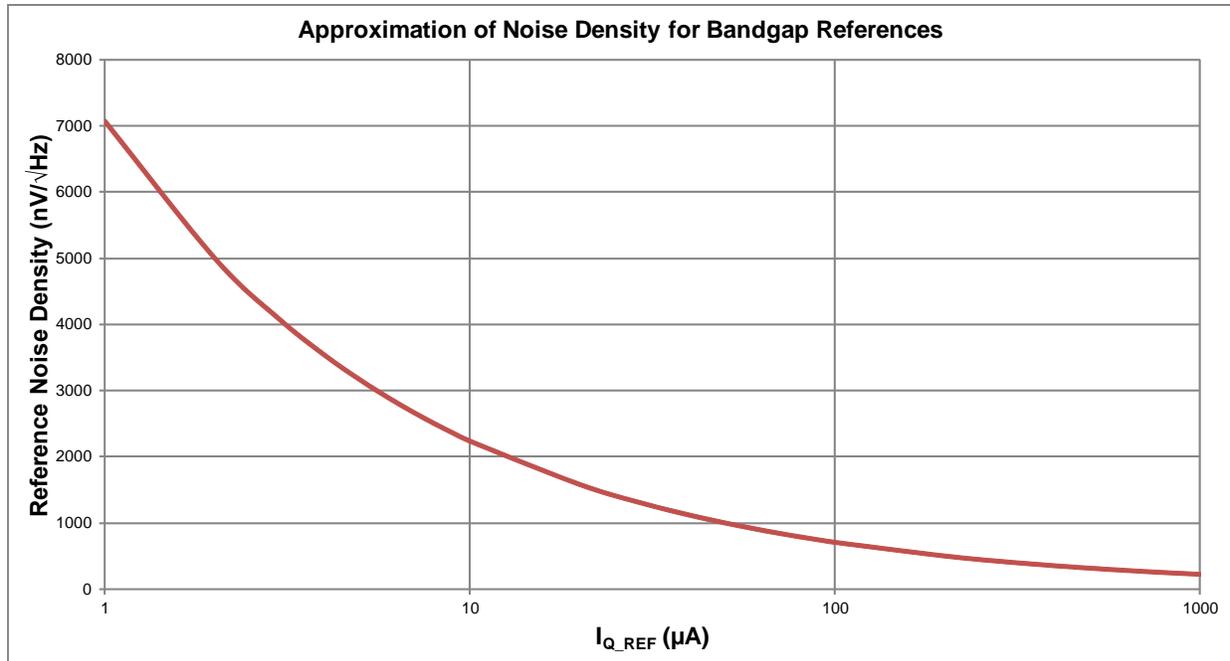


Figure 7. Characteristic Curve: Reference Noise vs Current

Using Equation 24 and Equation 25, the maximum limit for f_{REF_3dB} can be derived as Equation 26 shows:

$$f_{REF_3dB} \leq \frac{2 \times I_{Q_REF} (\mu\text{A})}{(10000 \text{ nV} / \sqrt{\text{Hz}})^2} \times \frac{2}{\pi} \times \left[\frac{1}{9} \times \frac{V_{FSR}^2}{8} \times 10^{\frac{-\text{SNR}(\text{dB})}{10}} - \left(\frac{V_{1/f_REF_pp}}{6.6} \right)^2 \right] \quad (26)$$

The value of the capacitor for the RC filter must be kept higher than 100 nF to keep its thermal noise lower than 0.2 μV_{RMS} . Using the selected value for C_{REF_FLT} and f_{REF_3dB} , the value of R_{REF_FLT} can be calculated using Equation 26 (see Equation 27):

$$R_{REF_FLT} = \frac{1}{2\pi f_{REF_3dB} \times C_{REF_FLT}} \quad (27)$$

After the noise of the reference block is band-limited, the next important step is to ensure that the reference can drive the dynamic load posed by the ADC reference input. The reference buffer must regulate the voltage such that ΔV_{REF} stays within a 1-LSB error at the start of each conversion. This requirement necessitates the use of a capacitor (C_{BUF_FLT}) at the output of the buffer amplifier to drive the ADC reference pin. The calculations to determine the size of C_{BUF_FLT} are given below:

For an ADC with resolution N , the difference in V_{REF} between two conversions is given by [Equation 28](#):

$$\Delta V_{REF} \leq \frac{V_{REF}}{2^N} \quad (28)$$

Let the total charge consumed during each conversion be Q_{REF} . Due to the configuration of the reference buffer, a big portion of this charge is contributed by the C_{BUF_FLT} capacitor during the fast-conversion process and the remaining charge is provided by the buffer amplifier. In general, it is safe to assume that the capacitor provides more than two-thirds of this charge during the fast conversion process. Hence, the minimum value of C_{BUF_FLT} required to regulate the reference voltage is given by [Equation 29](#):

$$C_{BUF_FLT} = \frac{2}{3} \times \frac{Q_{REF}}{\Delta V_{REF}} \geq \frac{2}{3} \times \frac{Q_{REF} \times 2^N}{V_{REF}} \quad (29)$$

The average value of Q_{REF} can be calculated from the maximum ADC conversion time (T_{CONV_MAX}) and the average value of reference input current (I_{REF}) specified in the ADC datasheet as shown in [Equation 30](#):

$$Q_{REF} = I_{REF} \times T_{CONV_MAX} \quad (30)$$

The combination of [Equation 28](#), [Equation 29](#), and [Equation 30](#) yields the expression for the minimum value of C_{BUF_FLT} as derived in [Equation 31](#):

$$C_{BUF_FLT} \geq \frac{2}{3} \times \frac{I_{REF} \times T_{CONV_MAX} \times 2^N}{V_{REF}} \quad (31)$$

The capacitor values derived from [Equation 31](#) are high enough to make the driving amplifier unstable, so TI recommends to use a series resistor, R_{BUF_FLT} , to isolate the amplifier output and make it stable. The value of R_{BUF_FLT} is dependent on the output impedance of the driving amplifier as well as on the signal frequency. Typical values of R_{BUF_FLT} range between 0.1 Ω to 2 Ω and the exact value can be found by using SPICE simulations. Note that higher values of R_{BUF_FLT} cause high voltage spikes at the reference pin which affects the conversion accuracy.

The capacitor C_{BUF_FLT} affects the stability of the driving amplifier; therefore, TI recommends to use a series resistor, R_{BUF_FLT} , to isolate the amplifier output and make it more stable. The value of R_{BUF_FLT} is dependent on the output impedance of the driving amplifier as well as on the signal frequency. Typical values of R_{BUF_FLT} range between 0.1 Ω to 2 Ω and the exact value can be found by using SPICE simulations. TI recommends to use the smallest possible values for R_{BUF_FLT} to avoid any voltage spikes at the reference pin, which can potentially affect the conversion accuracy.

After designing the appropriate passive filter for band-limiting the noise of the reference circuit, the next step is to select an appropriate amplifier for use as a reference buffer. The key specifications to be considered when selecting an appropriate amplifier for the reference buffer are:

- **Open-loop output impedance** for a reference buffer must be kept as low as possible because the ADC draws current from the reference pin during conversion and the resultant drop in reference voltage is directly proportional to the output impedance of the driving buffer. Impedance also helps to keep the amplifier stable while driving a large capacitive load (C_{BUF_FLT}).
- **Input offset:** The initial input offset must be minimized to ensure that the reference voltage driving the ADC is very accurate.
- **Offset drift:** The offset temperature drift of the reference buffer must be as low as possible to ensure that the reference voltage for the ADC does not change significantly over the operating temperature range.

3 Component Selection

This design is focused on optimizing the performance of a DAQ system for minimum power consumption using TI's low-power, high-resolution, 18-bit SAR ADC ADS8881 at its maximum sampling rate of 1 MSPS. This design uses a full-scale sine-wave signal of 10-kHz frequency at the differential inputs of the ADC. This section explains the procedure for selecting the various circuit components specific to this design.

3.1 Component Selection for Input Driver Circuit

3.1.1 Amplifier Selection

To meet the goals for this design, the first step is to select an appropriate amplifier for driving the ADC inputs. Because this design is specified for a full-scale sinusoidal input signal, the op amp must support *rail-to-rail input and output (RRIO) swing*. The other key specifications to consider for meeting the performance goals for this application are *low power, low noise, and high small-signal bandwidth* to reduce the signal distortion at high frequencies.

The OPA320 CMOS amplifier is a high-precision, low-power, and low-noise amplifier optimized for low-voltage, single-supply operation with rail-to-rail input and output. In this application, the input is a 10-kHz sine-wave signal with amplitude equal to the full-scale input range of the ADC, which utilizes the rail-to-rail input swing of this amplifier, operating from a single 5-V supply. This amplifier offers a low noise (7 nV/√Hz) and high bandwidth at an extremely-low quiescent current of 1.85 mA (max.). This feature makes the amplifier an ideal choice to drive the inputs of a high performance ADC like the ADS8881 and achieve maximum dynamic performance out of the system at the lowest power consumption.

3.1.2 RC-Filter Passive Components Selection

The critical passive components for this design are the resistor (R_{FLT}) and capacitor (C_{FLT}) for the RC filter at the input of the ADC. The tolerance of the selected resistor can be chosen as 1% because the use of a differential capacitor at the input balances the effects due to any resistor mismatch. However, give special attention when selecting an appropriate capacitor type for this application, as it helps to minimize signal distortion at the ADC inputs. The COG (NPO) capacitors are appropriate for this application due to their high Q, low temperature coefficient, and stable electrical characteristics under varying voltages, frequency, and time.

The specified value of the input capacitance for ADS8881 is 59 pF, so according to [Equation 15](#):

$$C_{FLT} \geq 20 \times C_{SH}$$

$$\Rightarrow C_{FLT} \geq 1.18nF \tag{32}$$

The selected value of capacitance for each input of the ADC is set slightly higher than the calculated value to 4.4 nF if the filter is designed in a common-mode configuration as shown in [Figure 8](#). However, this design uses a differential configuration for the RC filter, so a 2.2-nF capacitor is connected across the differential inputs of the ADC.

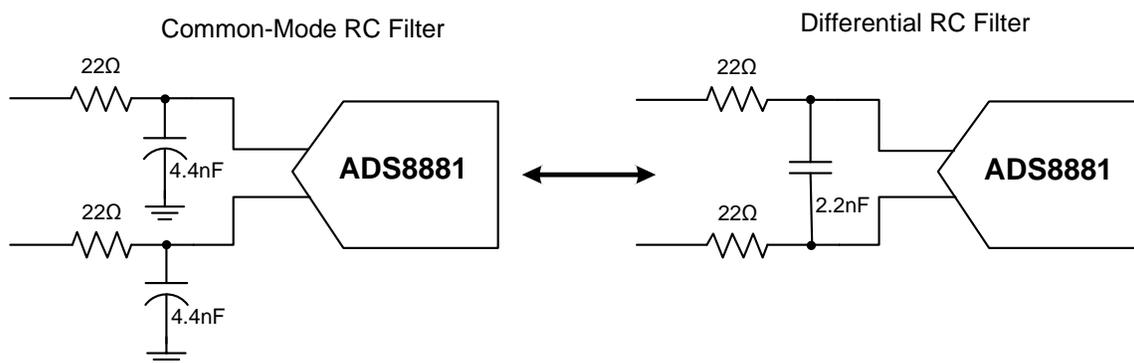


Figure 8. Design Configurations for Antialiasing RC Filter at ADC Input

The value for the resistor R_{FLT} is selected to maintain the stability of the driving amplifier and is dependent on the output impedance of the driving amplifier, as Equation 19 explains. The output impedance of OPA320 has been simulated using the TINA-TI™ SPICE tool, as Figure 9 shows. The simulation results shown in Figure 10 indicate that the value of R_o is equal to 92.08 Ω at the frequencies of interest.

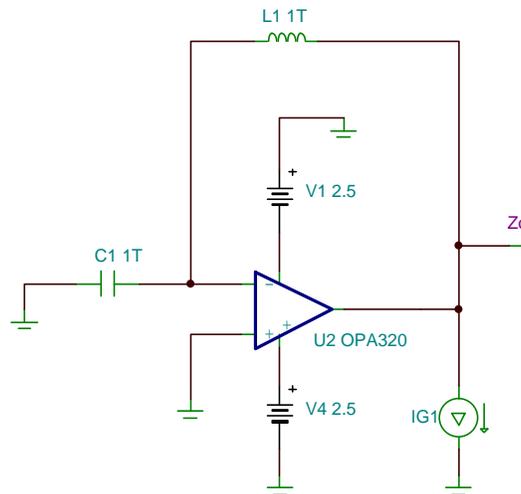


Figure 9. TINA-TI™ Schematic: Measuring Output Impedance of OPA320

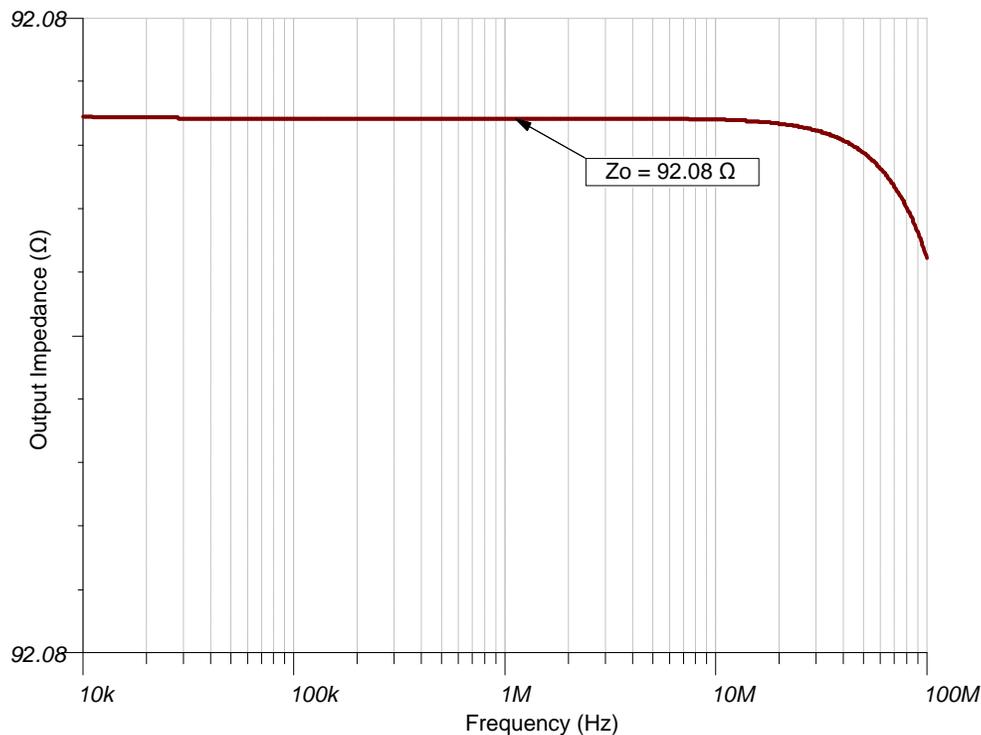


Figure 10. TINA-TI™ Simulation Result: Output Impedance of OPA320

Using Equation 19, the minimum value for resistance R_{FLT} is calculated using the R_o of OPA320 as:

$$R_{FLT} \geq \frac{92}{9} \approx 10\Omega \tag{33}$$

The selected value of R_{FLT} for each differential input of the ADC is 22 Ω for the optimum system performance.

3.2 Component Selection for Reference Driver Circuit

3.2.1 Passive Components Selection

The external reference used to drive the ADS8881 in this design is the REF5045 reference from TI. This reference has been selected because it provides the highest possible reference voltage of 4.5 V in a system with only a 5-V supply. As mentioned in the datasheet of REF5045, the device requires a capacitance of 10 μF at the V_{OUT} pin for stability purposes. A series resistor of 0.2 Ω is used with the 10- μF capacitor for smooth power-up of the reference.

According to the discussion in [Section 2.3](#), the noise from the reference should be bandwidth-limited by designing a low-pass RC filter at the reference output. According to [Equation 26](#), the maximum value of the 3-dB bandwidth for this filter can be calculated in [Equation 34](#) as:

$$f_{\text{REF_3dB}} \leq \frac{2 \times I_{\text{Q_REF}} (\mu\text{A})}{\left(10000 \text{ nV} / \sqrt{\text{Hz}}\right)^2} \times \frac{2}{\pi} \times \left[\frac{1}{9} \times \frac{V_{\text{FSR}}^2}{8} \times 10^{-\frac{\text{SNR}(\text{dB})}{10}} - \left(\frac{V_{1/2_REF_pp}}{6.6} \right)^2 \right]$$

$$\Rightarrow f_{\text{REF_3dB}} \leq 1.75 \text{ kHz} \quad (34)$$

The value of capacitor $C_{\text{REF_FLT}}$ has been selected as 1 μF to keep the thermal noise of the capacitor at a low value. The next higher value for a standard capacitor is 10 μF . These capacitors are very bulky and expensive which is why they are generally avoided in a design unless absolutely necessary. The minimum value of $R_{\text{REF_FLT}}$ can be calculated using [Equation 34](#) as:

$$R_{\text{REF_FLT}} \geq \frac{1}{2\pi \times 1.75 \times 10^3 \times 10^{-6}} = 91 \Omega \quad (35)$$

The value of $R_{\text{REF_FLT}}$ has been selected as 1 $k\Omega$ for this design. The selected value for the resistor is much higher than the calculated minimum value to further reduce the bandwidth of the filter so that the broadband noise contribution from the reference is negligible.

The next important passive element in the reference design is the capacitor $C_{\text{BUF_FLT}}$, which helps to regulate the voltage at the ADC reference pin under dynamic load conditions. According to the ADS8881 datasheet, the average current drawn into the reference pin (I_{REF}) is 350 μA and for a maximum throughput of 1 MSPS, $T_{\text{CONV_MAX}}$ is equal to 710 ns. Hence, according to [Equation 31](#), the value of $C_{\text{BUF_FLT}}$ can be calculated in [Equation 36](#) as:

$$C_{\text{BUF_FLT}} \geq \frac{2 \times 350 \times 10^{-6} \times 710 \times 10^{-9} \times 2^{18}}{3 \times 4.5} = 9.65 \mu\text{F} \quad (36)$$

The value of $C_{\text{BUF_FLT}}$ has been selected as 10 μF for this design.

3.2.2 Amplifier Selection

As explained in [Section 2.3](#), the key amplifier specifications to be considered to design a reference buffer for a high-precision ADC are *low offset*, *low drift*, *wide bandwidth*, and *low output impedance*. While selecting an amplifier that meets all these requirements is possible, it may come at a cost of excessive power consumption. For example, the OPA350 is a 38-MHz amplifier with an offset of 0.5 mV and low offset drift of 4 $\mu\text{V}/^\circ\text{C}$, but it consumes a quiescent current of 5.2 mA, which is extremely high for this design. This high consumption occurs because offset and drift are DC specifications while bandwidth, output impedance, and high-capacitive drive capability are AC specifications. Thus, achieving all the performance in one amplifier requires power. A more efficient way to minimize power is to use a composite reference buffer, as it utilizes an amplifier with superior high-frequency specifications in the feedback loop of a DC precision amplifier to obtain the best results for both specifications at a much lower power.

In this design, the reference buffer has been designed using two amplifiers—THS4281 and OPA333 in a composite double-feedback architecture as shown in [Figure 11](#).

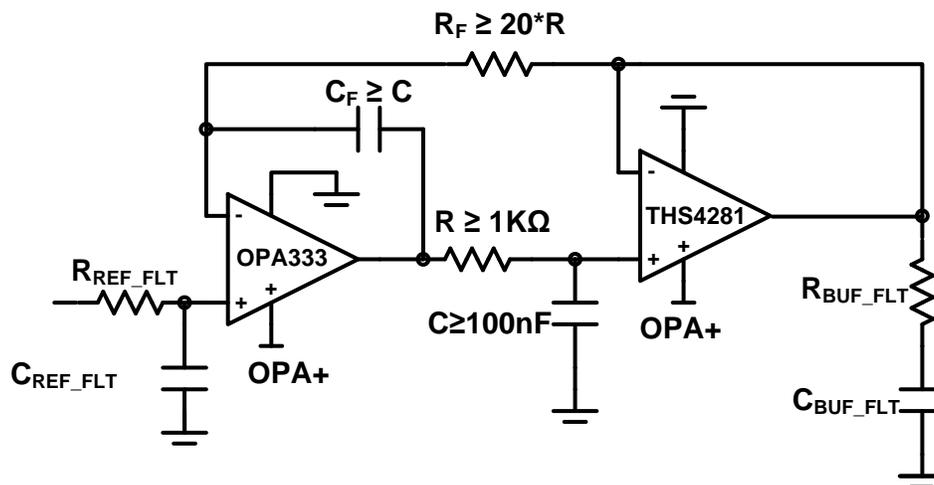


Figure 11. Schematic of Reference Buffer Circuit

The THS4281 has a wide 3-dB bandwidth of 90 MHz at a gain of 1 and output impedance of 1 Ω for 1-MHz operation, with a maximum quiescent current of only 1 mA. These specifications make the THS4281 device ideal for driving the high capacitor C_{BUF_FLT} and regulating the voltage at the ADC reference input. However, the THS4281 suffers from poor offset (2.5 mV max.) and drift (7 $\mu\text{V}/^\circ\text{C}$ max.) specifications. The OPA333 is used as a DC-correcting amplifier to improve the DC specifications of the reference buffer. The OPA333 is a zero-drift (0.05 $\mu\text{V}/^\circ\text{C}$ max.) and low offset (10 μV max.) amplifier with a maximum quiescent current of only 25 μA . Thus, for a much better performance related to reference accuracy and load regulation, this two-amplifier approach consumes only 20% of power compared to a single amplifier buffer.

In this reference buffer design, the noise specifications of the DC amplifier (OPA333) are not very important because the amplifier is heavily filtered by the low-frequency RC filter at its output. The value of C is chosen to be greater than 100 nF to keep the capacitor thermal noise to less than 0.2 μV_{RMS} and the value of R is selected greater than 1 k Ω to avoid any stability issues due to high-capacitive loading.

This amplifier uses a dual feedback in the design, out of which one feedback is active during DC operation and the other feedback is active during higher-frequency AC operation. The active feedback during DC operation, as shown in [Figure 12](#), displays the DC model of the circuit, where R_F appears as a short because there is no current flowing in that branch and C_F appears as an open circuit. This feedback connects the output of the THS4281 device directly to the inputs of the OPA333 device, which then corrects for its offset and drift. The value of R_F should be at least 20 times greater than R to avoid any stability issues.

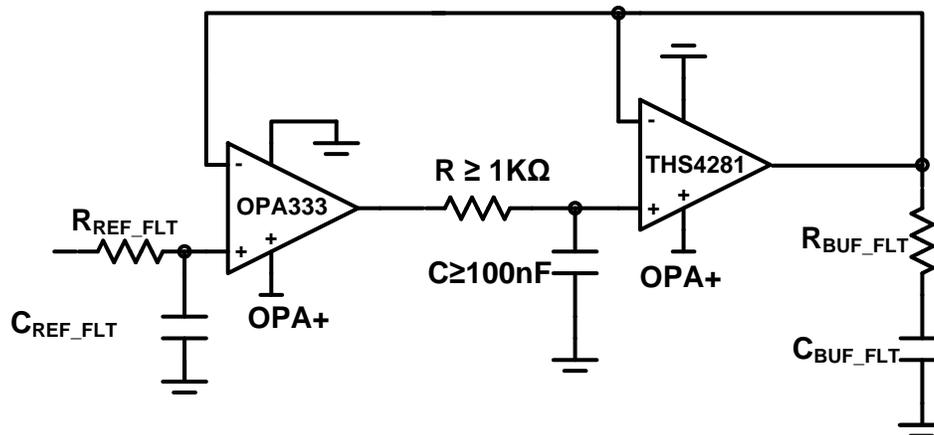


Figure 12. DC-Equivalent Schematic of Reference Buffer

The active feedback connection during higher-frequency operation is shown in Figure 13. At such frequencies of operation, R_F acts as an open connection, C_F acts as a short, and the two amplifiers are connected as isolated unity-gain buffers. The value of C_F must be equal to or greater than C to avoid any stability issues.

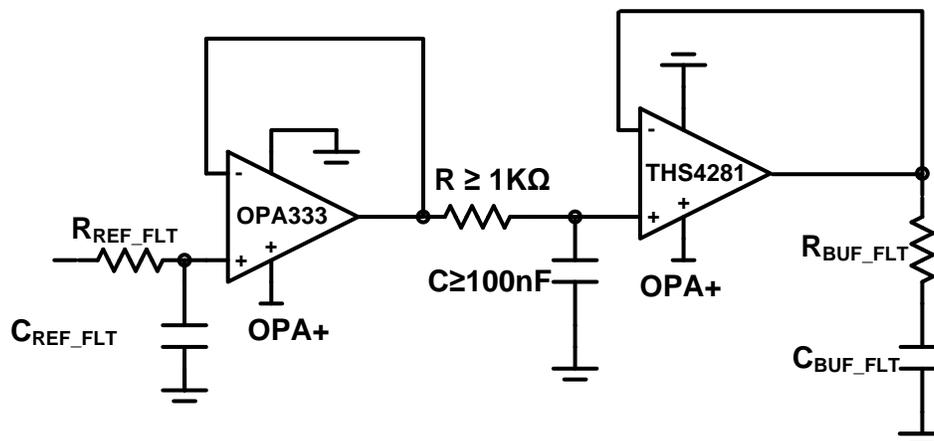


Figure 13. High-Frequency Equivalent Schematic of Reference Buffer Circuit

3.2.3 Integrated Reference and Buffer

With new and increased integration among available components, another option to drive the reference on the ADC is an integrated reference and buffer. This option replaces the reference driver circuit with one main component, which avoids the long design process of choosing the correct amplifier for the best performance. Even when an amplifier does meet the necessary specifications for a design, such as wide bandwidth, low output impedance, low offset, and low drift, the power consumption must still be considered as well as design time. The REF60xx family is a high-performance line of reference drivers that TI offers, which is the industry's first integrated low-output impedance buffer. Each reference driver is trimmed during production to achieve a max drift of only 5 ppm/°C for both the reference and integrated buffer combined. The device also consumes a low 820- μ A quiescent current while still being able to replenish a charge of 70 pC on a 47- μ F capacitor in 1 μ s. This integrated device decreases design time by eliminating the requirement of implementing the entire reference driver circuit.

The REF6045 is specifically the ideal choice for this design, with an output of 4.5 V, and simplifies the reference circuitry as shown in [Figure 14](#)

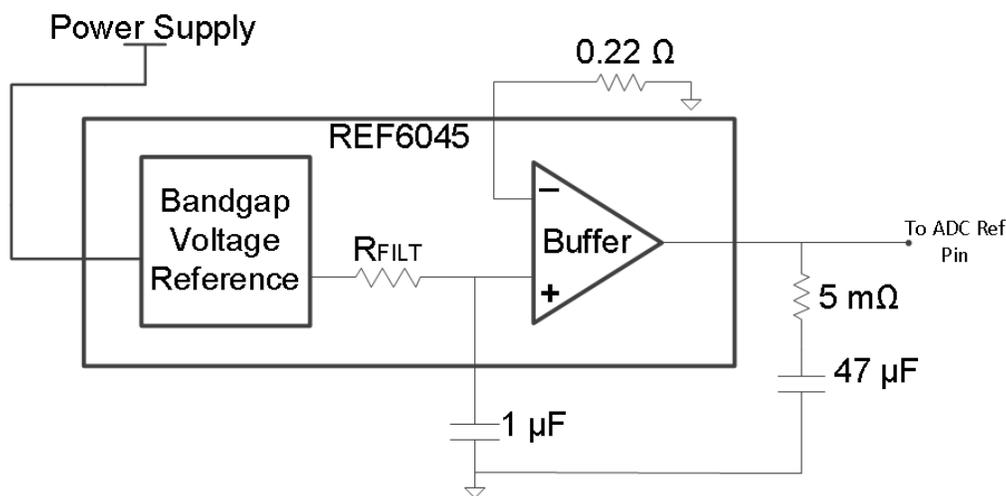


Figure 14. REF6045 Voltage Reference With Integrated Buffer

4 Simulation

The TINA-TI™ schematic shown in Figure 15 includes the final design and circuit component values obtained in the design process.

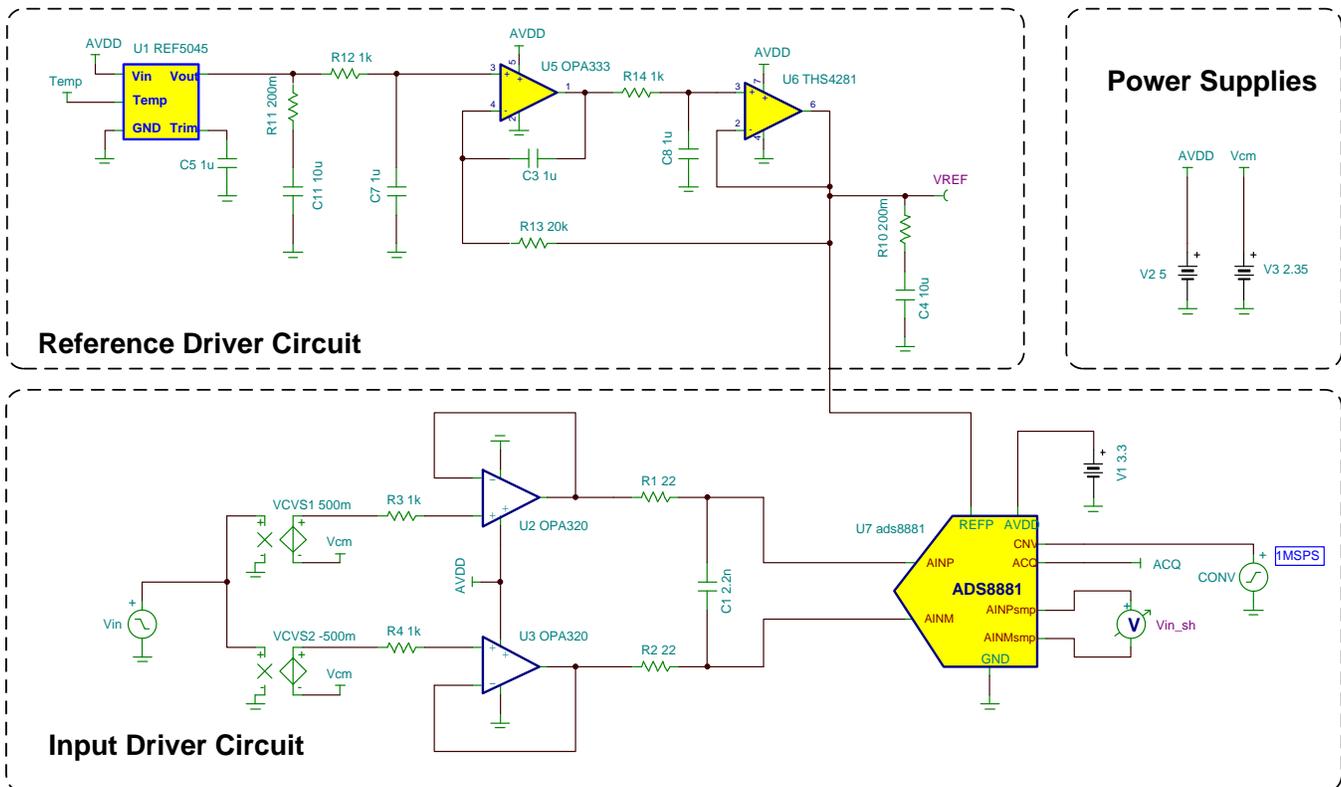


Figure 15. TINA-TI™ Schematic—Complete DAQ Block

The TINA-TI SPICE Model for ADS8881 is used to evaluate the performance of the entire signal chain. The SPICE model for the ADC accurately models the input sample-and-hold circuit of the ADC, which is important in designing for an appropriate front-end input driver circuit. The model also includes the dynamic loading of the REFP input pin, which is helpful for optimizing the design of the external reference driver circuit. The ADC model outputs two signals known as "AINPsm" and "AINMsm", which represent the output of the internal sample-and-hold stage of the ADC. During sampling, these two signals track the corresponding input signals and during conversion these signals are held at a value of the input signal, which is being converted by the ADC.

The circuit in the preceding Figure 15 is simulated for transient analysis using a 10-kHz sine-wave signal to check that the ADC input is settling to a sufficient accuracy before the start of every conversion. The same circuit is also used to simulate an accurate settling of reference input voltage at the beginning of each conversion. The simulation details and results are provided in the subsequent subsections.

4.1 Stability of Input Driver Amplifiers

The TINA-TI schematic that Figure 16 shows is used to check the stability of the amplifiers driving the ADC inputs. Despite paying careful attention to the input amplifier stability during the selection of design components, it is an important first step to check the amplifier stability in simulations. If the input amplifiers are unstable or marginally stable, then the selection of components should be revisited to make the design more robust from a stability perspective.

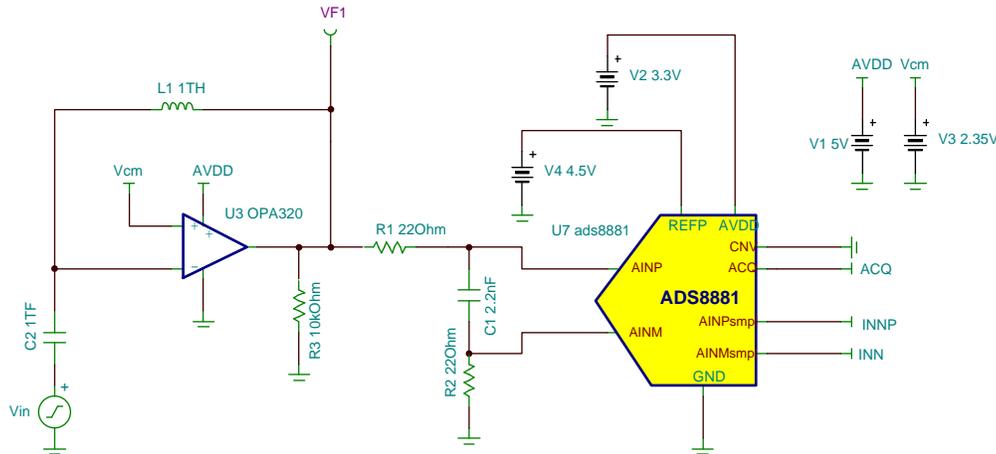


Figure 16. TINA-TI™ Schematic—Checking Input Amplifier Stability

This circuit simulates the loop gain of the input driver to determine the phase margin and hence the stability of the amplifier. A large inductor of value 1TH is connected in the feedback loop of the amplifier, so it behaves like an open-loop configuration at frequencies higher than the DC. The circuit has been simplified by only considering the half-circuit of the differential input structure. To appropriately load the amplifier output, the ADC is connected with the “CNV” pin tie to GND so that it is always sampling the input.

Figure 17 shows the AC magnitude and phase response for the loop-gain of this circuit. The resulting phase margin of 62.84° at the 0-dB crossover frequency of 7.74 MHz validates the stability of the input drivers for this design.

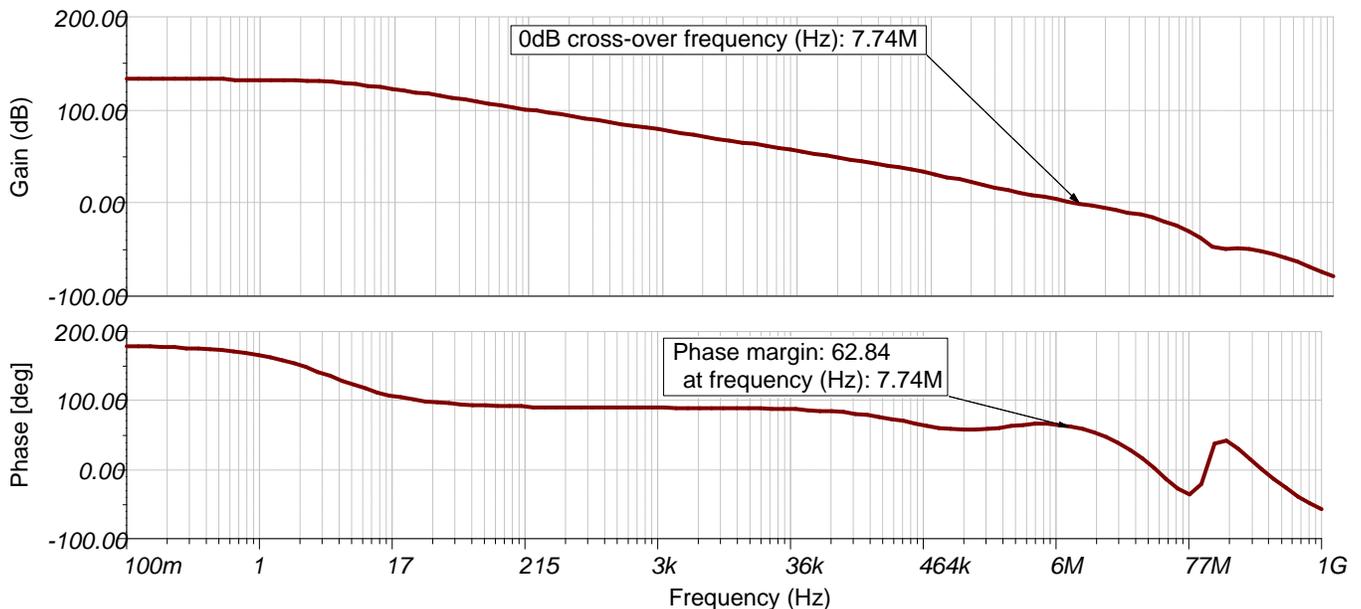


Figure 17. TINA-TI™ Simulation Result—Loop Gain Magnitude and Phase Plot for Input Driver Stability

4.2 Transient Simulation of ADC Input Circuit

The TINA-TI™ schematic that the preceding Figure 15 shows is used to check the accurate settling of the sine-wave signal at the inputs of the ADC during the sampling phase. Figure 18 shows the simulated time-domain response for the circuit. The transient plot on the top of the figure shows one cycle of a 10-kHz sine-wave with an amplitude of ± 4.63 V applied at the differential inputs of the ADS8881. The signal "Vin" represents the actual input signal at the differential inputs of the ADC and the signal "Vin_sh" shows the output of the ADCs input sample-and-hold circuit, as explained in Section 4. The lower plot shows the same waveform zoomed-in on the time scale for more details. The curves are collated together to show that the sampled signal accurately tracks the input signal during sampling and stays on hold when the ADC is converting.

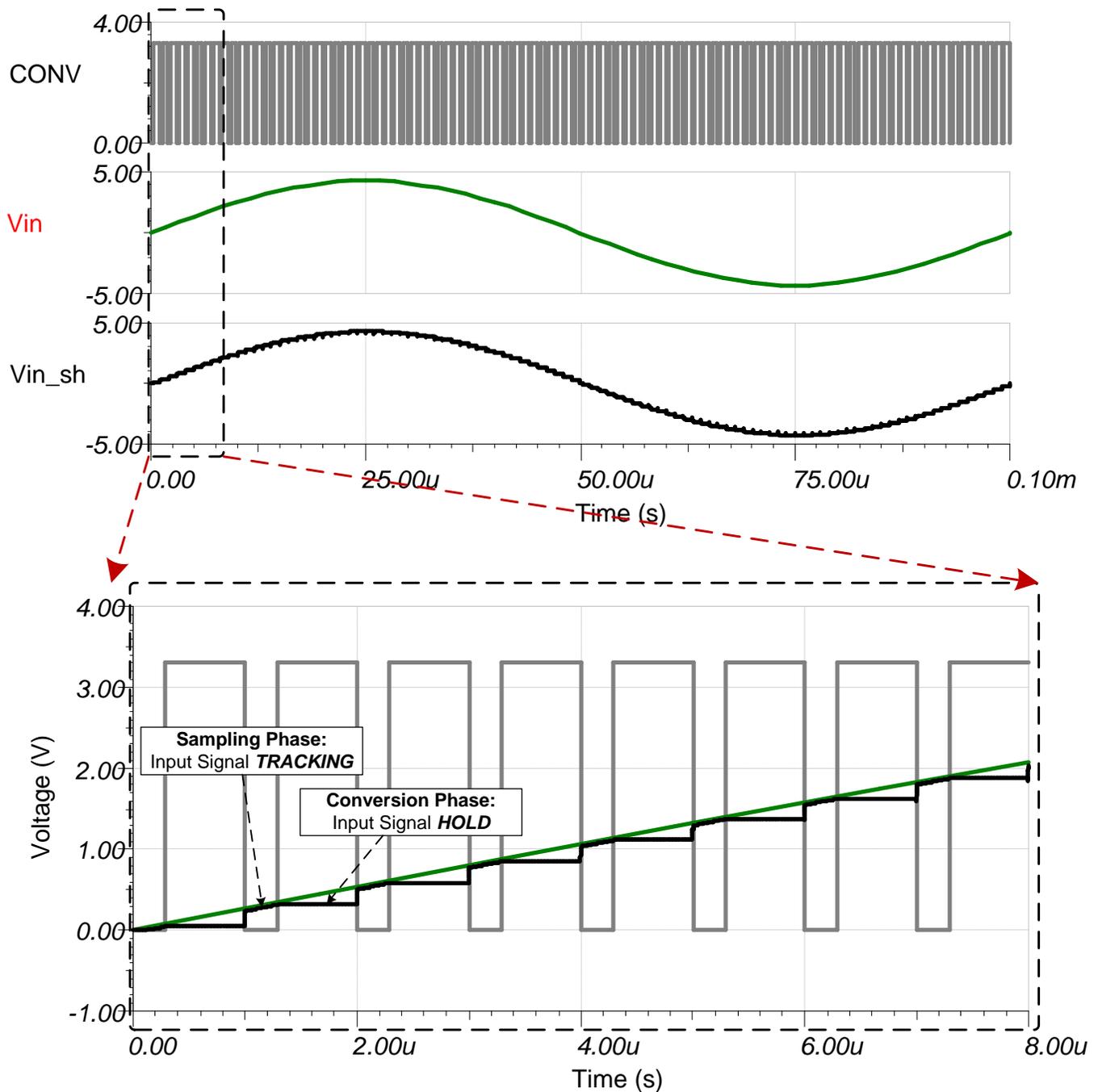


Figure 18. TINA-TI™ Simulation Result—Digitization of Input Sine-Wave Showing ADC Sample-and-Hold

A further zoomed-in version of the input signal and sampled signal (see Figure 19) shows a phase delay between the two signals, which is caused purely by the propagation delay through the front-end driving circuitry and the input stage of the ADC.

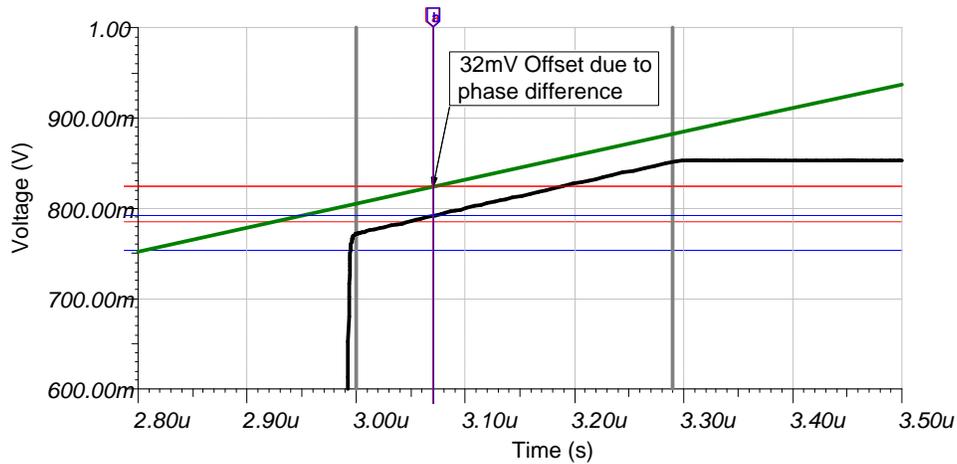


Figure 19. TINA-TI™ Simulation Result—Phase Shift between Input and Sampled Signals

4.3 Settling Response of ADC Reference Input

The TINA-TI™ schematic shown in Figure 15 is used to check the settling of the reference buffer output driving the REFP pin of the ADS8881. As explained in Section 2.3, the voltage at the reference pin should settle to less than the LSB of the ADC for maintaining the overall system performance. The size of the LSB for the ADS8881 using $V_{REF} = 4.5\text{ V}$ is equal to $34.3\text{ }\mu\text{V}$. According to the transient simulation plot that Figure 20 shows, the voltage error at the REFP pin between two successive conversions is equal to $\Delta V_{REF} = 0.3\text{ }\mu\text{V}$, which is significantly less than the size of the LSB. This result validates that the reference voltage has settled to a sufficient accuracy that is required to maintain the performance of this design.

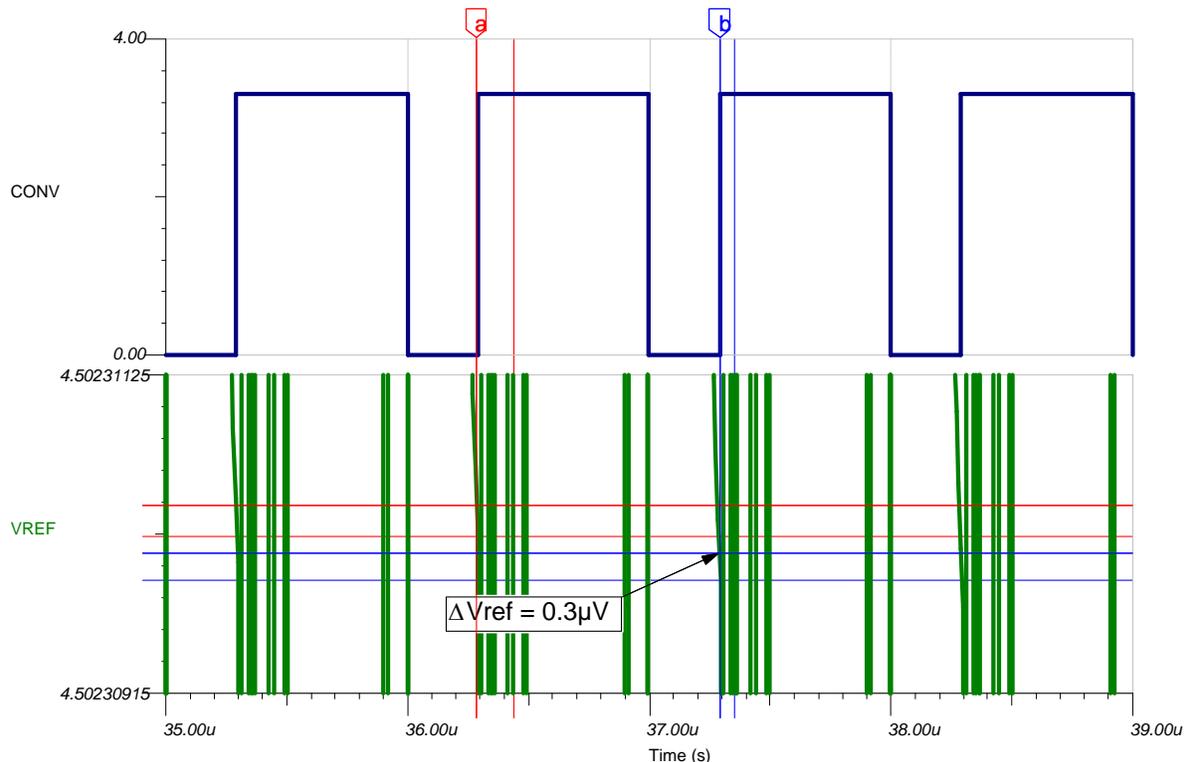


Figure 20. TINA-TI™ Simulation Result—ADC Reference Settling

5 Verification and Measured Performance

The measurement results for verification of this TI Precision Design are listed in this section.

5.1 DC Noise Measurement

All ADC circuits suffer from some amount of inherent broadband noise contributed by the internal resistors, capacitors, and other circuitry, which is referred to the inputs of the ADC. The front-end driver circuit also contributes some noise to the system, which can also be referred to the ADC inputs. The cumulative noise of the ADC, often called the *input-referred noise*, has a significant impact on the overall system performance. The most common way to characterize this noise is by using a constant DC voltage as the input signal and collecting a large number of ADC output codes. A histogram can then be plotted to show the distribution of output codes, which can be used to show the impact of noise on the overall system performance. In this design, the DC noise for the system is measured by shorting the inputs of both input-driving amplifiers to a common-mode voltage, $V_{CM} = \frac{1}{2} \times V_{REF} = 2.25 \text{ V}$, such that the differential voltage at the inputs of the ADC is equal to $V_{DIFF} = 0 \text{ V}$. Figure 21 shows the resulting histogram of the output codes.

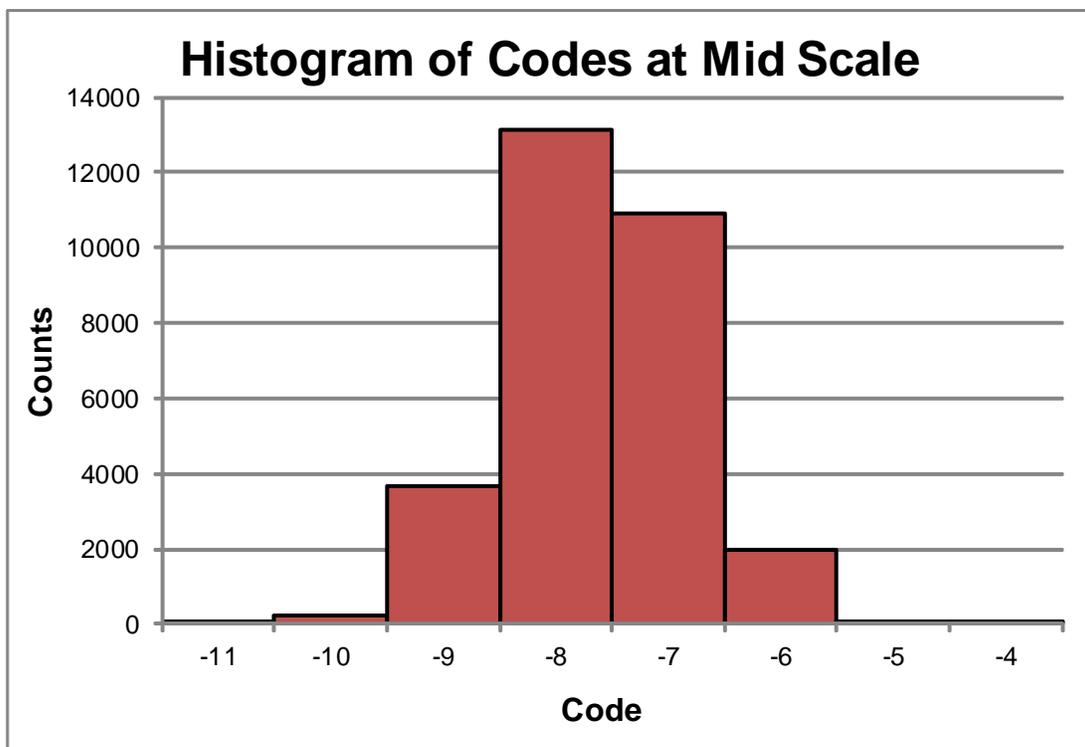


Figure 21. Measurement Data—Histogram Showing DC Noise (Mid-Scale)

The distribution of output codes looks like a Gaussian distribution, which indicates a properly-designed system. However, if the output code distribution has large peaks and valleys, which make it distinctly non-Gaussian, then the distribution indicates significant DNL errors in the ADC or issues with the system design such as insufficient power-supply decoupling, improper ground connections, or other poor printed-circuit board (PCB) layout effects. For a theoretically-perfect ADC system, the histogram of output codes would be a single vertical bar because the ADC output is always the same for a DC input voltage. However, the noise contributions from the ADC and the front-end circuit leads to a distribution of output codes, which provides a measure of the overall DC noise of the system. Table 2 lists the measured values of peak-to-peak difference between the codes (N_{pp}) and the standard deviation of codes (N_{σ}).

The noise-free resolution of an ADC is defined as the number of steady output bits from the converter beyond which it is impossible to differentiate between individual code transitions. This parameter is an extremely conservative measurement of the ADC performance because the formula for noise-free resolution is derived from the peak-to-peak code noise, which is dependent on the total number of samples.

A more reliable approach is to use the standard deviation of output codes (N_σ) in calculating the effective resolution of the ADC. Note that the results shown in [Table 2](#) do not assume a Gaussian-based formula in calculating the standard deviation from the peak-to-peak value because the overall DC noise is comparable to the size of the LSB. For an 18-bit ADC used in this design, the measured value of effective resolution is also equal to 18 bits, which indicates that there is no degradation in the performance of the converter due to the effects of DC noise.

Note that the *effective resolution* and *effective number of bits (ENOB)* shown in [Section 5.2](#) are not to be confused with each other as they are two completely different entities. The ENOB for an ADC is measured with an AC sinusoidal input signal and includes the effects due to quantization noise and distortion terms, which have no impact on a DC measurement.

Table 2. Measurement Results for DC Noise

PARAMETER	FORMULA	MEASURED VALUE
Mean output code	—	-7.64
Peak-to-peak code noise (N_{PP})	Maximum output code – minimum output code + 1	8
Standard deviation of codes (N_σ)	—	0.82
Noise-free resolution	$\log_2 \left(\frac{2^{18}}{N_{PP}} \right)$	15
Effective resolution	$\log_2 \left(\frac{2^{18}}{N_\sigma} \right)$	18

5.2 ADC Dynamic Performance Measurement

The TI Precision Design explained in this document has been optimized to achieve maximum performance out of the ADS8881 at a throughput of 1 MSPS for the lowest power consumption. However, this system also achieves excellent AC noise and distortion performance, as listed in Table 3. The measurements have been performed using a 10-kHz sinusoidal input signal. Figure 22 shows a screenshot of TI's ADCPro™ tool displaying the measured AC performance of the system. The datasheet specifications are based on $V_{REF} = 5\text{ V}$, but these measurement results indicate the ADC performance for $V_{REF} = 4.5\text{ V}$, which implies that the measured values are approximately 0.9 dB less than the actual ADC performance for SNR, THD, and SINAD. Despite this adjustment, the measured THD from this system is worse than the specified THD of the ADS8881 because this design uses OPA320 as the input-driving amplifier, which adds significant distortion to the system. The choice of the input driver was mainly influenced by the low power consumption of OPA320 at the cost of a limited unity-gain bandwidth, due to which the amplifier is not able to correct for higher frequency distortions in the system.

Table 3. Measurement Results for ADC AC Performance

PARAMETER	ADS8881 DATASHEET SPECIFICATIONS	MEASURED VALUE
Signa-to-noise ratio – SNR (dB)	99 at $V_{REF} = 5\text{ V}$	98.97
Total harmonic distortion – THD (dB)	-112 at $V_{REF} = 5\text{ V}$	-105.64
Signa-to-noise and distortion ratio – SINAD (dB)	98.8 at $V_{REF} = 5\text{ V}$	98.12
Effective number of bits – ENOB	—	16.01

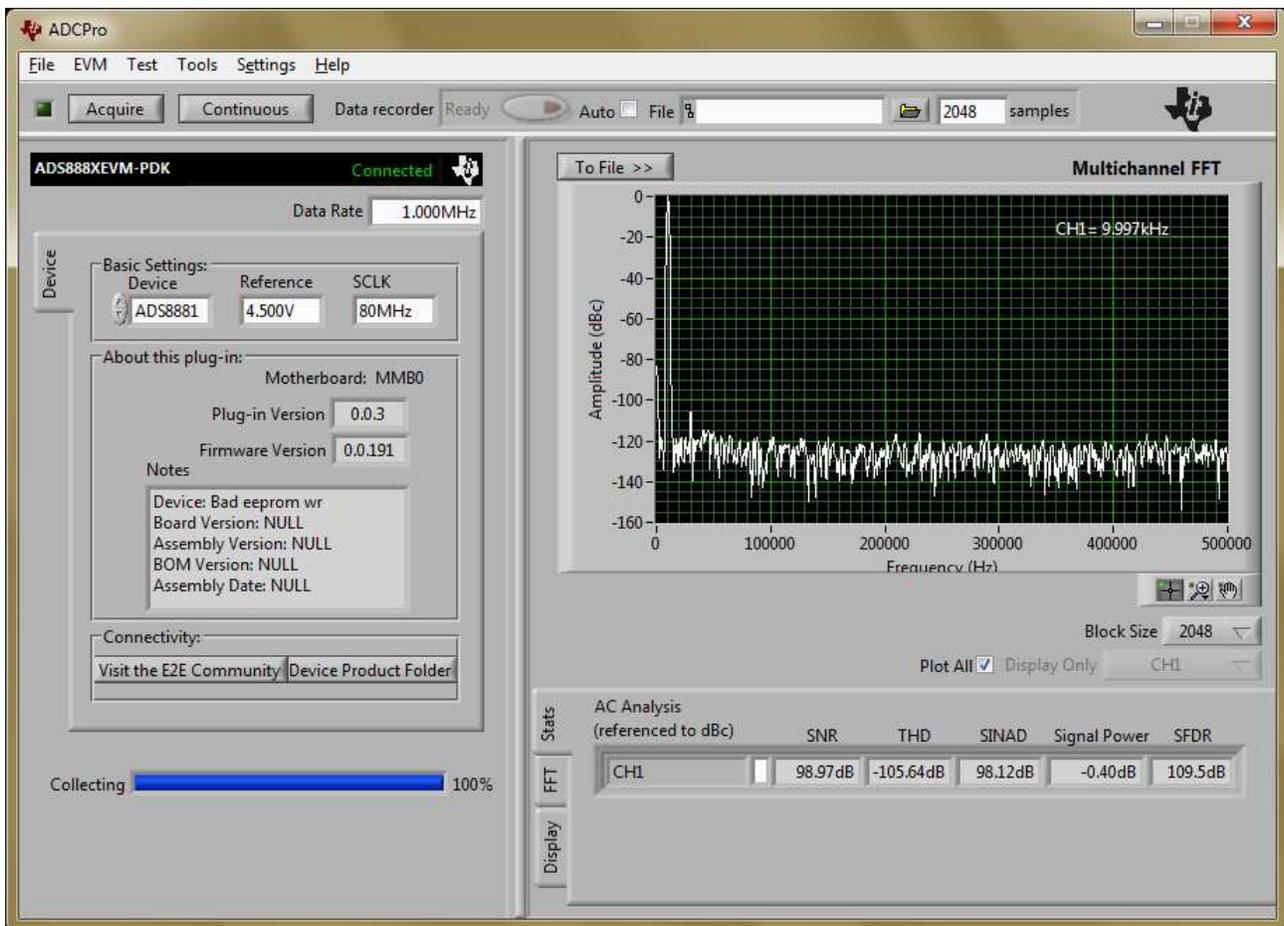


Figure 22. Measurement Data—AC Performance of DAQ Block Using ADCPro™

5.3 ADC Linearity Measurement

The linearity of the system was measured by sweeping the differential input voltage from -4.45 V to 4.45 V in 26 voltage steps and the integral non-linearity (INL) error is plotted after cancelling the offset and gain errors from the response. Figure 23 shows this 26-point INL plot. This DAQ block does not provide the best linearity performance because it has been optimized for lowest power consumption and low noise. The amplifier used in the front-end driver (OPA320) has a relatively-higher output impedance due to its low power, which results in a higher value for the isolation resistor (R_{FLT}) to keep the amplifier stable. The higher value of the isolation resistor increases the overall distortion for a full-scale input signal, which directly affects the linearity performance of the system.

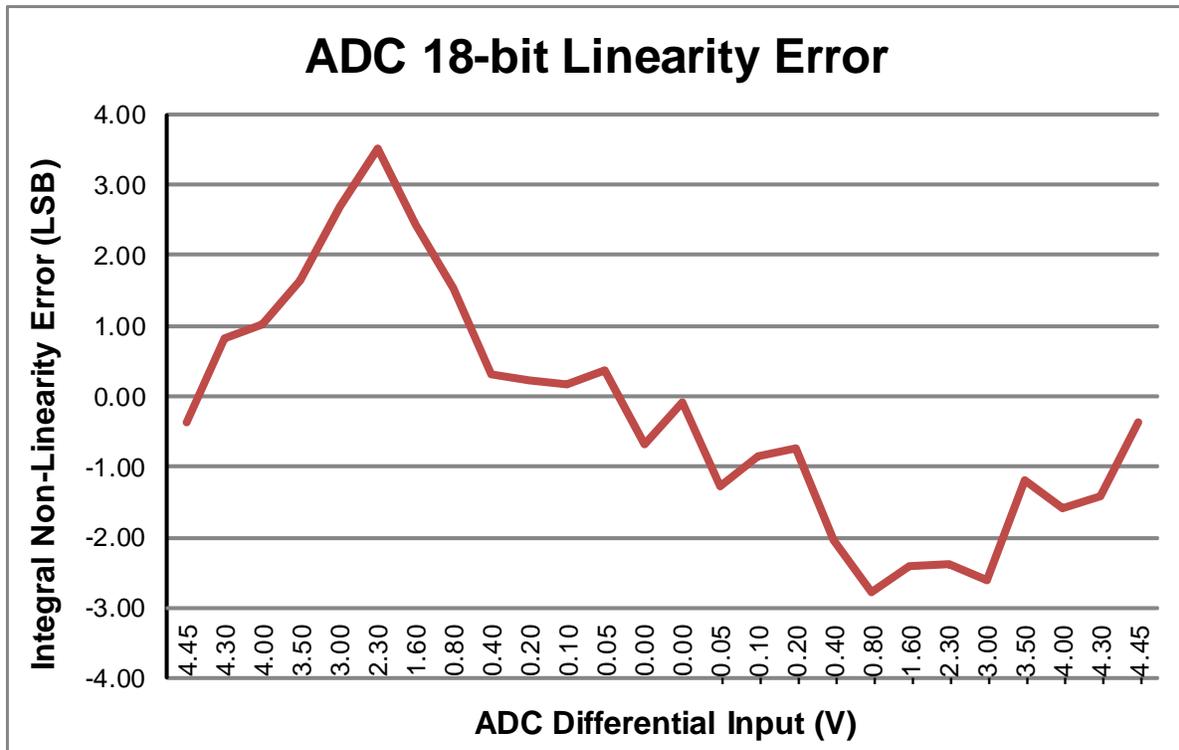


Figure 23. Measurement Data—ADC INL Plot (26 Points)

Table 4. Measurement Results for Linearity Test

PARAMETER	ADS8881 DATASHEET SPECIFICATION	MEASURED VALUE
Offset error (mV)	$\pm 4\text{ mV (max)}$	-0.277
Gain error (% FSR)	$\pm 0.03\% \text{ (max)}$	0.0014
INL _{MIN} (LSB)	-3	-2.78
INL _{MAX} (LSB)	3	3.5

6 Modifications

The components selected for this design are optimized to meet the design goals mentioned in [Section 1](#) at the beginning of the design. Selecting a low-power, low-noise amplifier with RRIO swing like the OPA320 helps to achieve the design goal of consuming less than 35 mW of power at a 5-V DC analog supply, while still achieving a good dynamic performance for a full-scale, 10-kHz sinusoidal input signal. The comparison in [Table 5](#) shows a few more low-power, low-noise RRIO amplifiers from TI's portfolio, which have been considered for this design. The results clearly show that the OPA350 has a better bandwidth, which can further reduce the higher frequency distortion in the circuit; however, this device was not selected due to its high power consumption. The lower-power RRIO amplifiers that were considered for this design include the OPA376 and OPA364. These amplifiers have lower bandwidth and higher broadband noise density, which make them an inappropriate selection for this design.

Table 5. Op Amp Specification Comparison for Driving Inputs of ADS8881

OP AMP	MAX I _Q (mA)	1/f NOISE: 0.1 Hz to 10 Hz (μ V _{PP})	NOISE DENSITY AT 10 kHz (nV/ \sqrt Hz)	UNITY GAIN BANDWIDTH (MHz)
OPA320	1.85	2.8	7	20
OPA350	7.5	Not specified	7	38
OPA376	1	0.8	7.5	5.5
OPA364	1.4	10	17	7

However, there are many applications which do not have a full-scale sinusoidal signal as inputs to the system. Such designs do not require to use an RRIO amplifier for driving the ADC inputs. [Table 6](#) lists a brief comparison between a few more amplifiers from TI's portfolio, which can be used as input drivers for such applications.

Table 6. Brief Comparison of ADC Input Drivers for Modified System Requirements

OP AMP	MAX I _Q (mA)	1/f NOISE: 0.1 Hz to 10 Hz (μ V _{PP})	NOISE DENSITY AT 10 kHz (nV/ \sqrt Hz)	UNITY GAIN BANDWIDTH (MHz)
OPA836	1.5	Not specified	4.6	205
OPA835	0.365	Not specified	9.3	56
OPA300	12	40	3	150

7 Design Files

7.1 Schematics

To download the schematics, see the design files at [TIPD113](#).

7.2 Bill of Materials

To download the schematics, see the design files at [TIPD113](#).

7.3 PCB Layout Recommendations

The most important considerations in designing the PCB layout for this DAQ block are as follows:

- The length of traces from the reference buffer circuit (REF5045, THS4281, and OPA333) to the REFP input pin of the ADC must be kept as small as possible to minimize the trace inductance that can lead to instability and potential issues with the accurate settling of the reference voltage.
- The input driver circuit, comprising OPA320 buffers should be located as close as possible to the inputs of the ADC to minimize loop area, thus making the layout more robust for electromagnetic interference (EMI) and radio-frequency interference (RFI) rejection. Similarly, the resistors and capacitor of the antialiasing filter at the inputs of the ADC should be kept close together and close to the inputs of the ADC to minimize the loop area.
- The traces feeding the differential input voltage from the source up to the differential inputs of the ADC should be kept symmetrical without any sharp turns.

Figure 24 shows the complete PCB layout for this design.

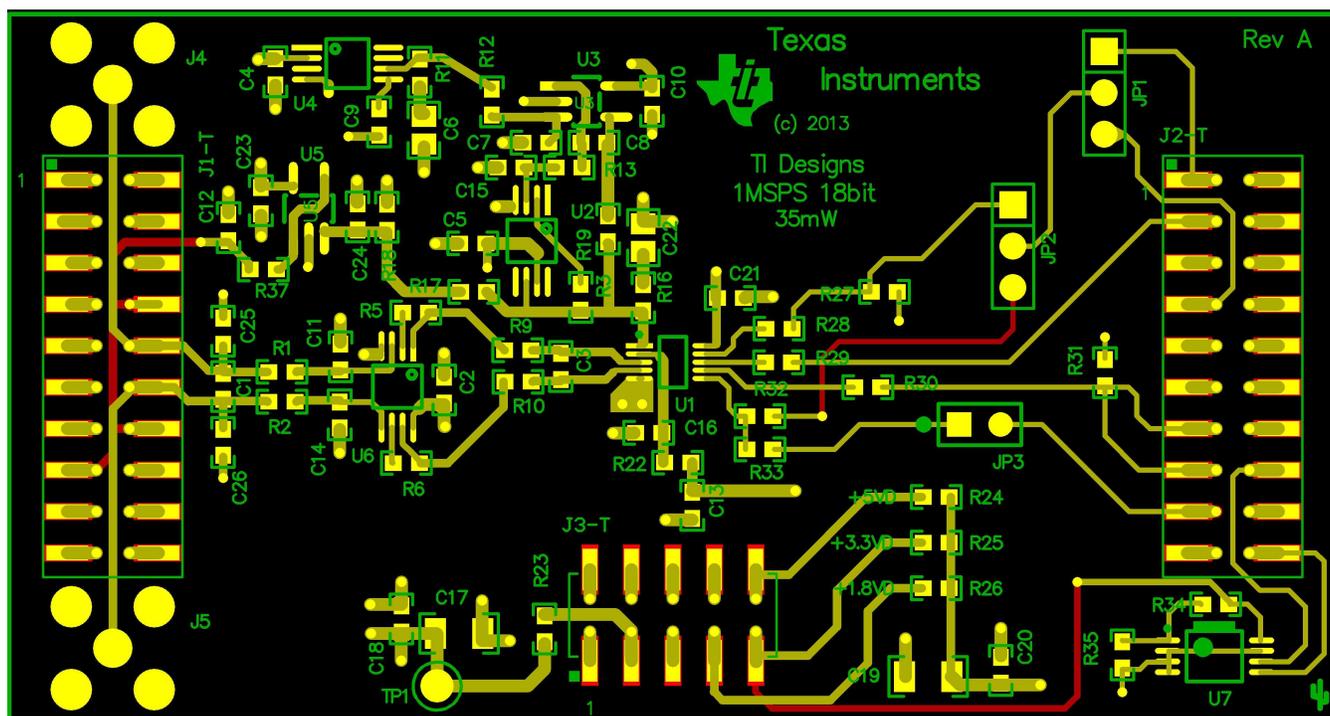


Figure 24. PCB Layout

8 Related Documentation

1. Green, Tim; *Operational Amplifier Stability - Parts 1-11*, November 2008 (http://www.engenius.net/site/zones/acquisitionZONE/technical_notes/acqt_050712)
2. Baker, Bonnie C; Oljaca, Miro; <http://www.electro-tech-online.com/custompdfs/2013/05/6602451.pdf>
3. Green, Tim; *Selecting the right amplifier for precision CDAC SAR A/D*, Internal Presentation, February

2008

8.1 Trademarks

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9 Acknowledgments

Credit for this work goes to Rafael Ordonez for designing the PCB board schematic and layout and taking all the measurement data.

10 About the Author

VINAY AGARWAL is a product definer in the Precision Analog, SAR ADC team at Texas Instruments based in Tucson, Arizona. Prior to this role, he has worked on designing precision data converters and amplifiers at TI. Vinay earned his master of science degree from Tufts University, Medford and bachelors in technology (Honors) from Indian Institute of Technology, Kharagpur in India.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

REVISION	PAGE	DESCRIPTION
SLAU513		Initial release
SLAU513A	11	Updated theory of operation for Reference Driver Design
	14	Updated reference current for ADS8881
SLAU513B	1, 15, 16	Updated front page block diagram and Figure 11 , Figure 12 , and Figure 13 ; changed system supply to OPA+ and ADC supply to AVDD
	2	Updated Design Summary ; modified OPA+ and AVDD supply specifications
SLAU513C	1	Replaced "Design Archive" with "TIPD113" to indicate the name of the design in Design Resources
	28	Deleted images for schematic and bill of materials and replaced with links to download these updated files from tool folder on TI.com
	17	Updated reference design options, including integrated reference and buffer, REF6045

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