Application Report
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# Driver Circuit Design Considerations for ADS855x

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High Performance Analog/Field Application

## ABSTRACT

ADS8556, ADS8555 is a 6 channel,16bit,simultaneous sampling, successive approximation register(SAR) analog-to-digital converter with true bipolar input, supports up to 630 Ksps sampling rate per channel.ADS855x's structure is suitable for power line measurement and protection systems of industrial application. This application report presents the solution with system performance improvement test to resolve the challenges of designing the driver circuit for ADS855x.

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## 1 Introduction

In power line measurement and protection systems, it is common to sample large numbers of voltage and current channels of multiphase power line networks, but it is critical to have the simultaneous sampling capability to maintain the phase information between the voltage and current channels in high voltage and high accurate systems.ADS8556/8555 is 6-channel, 16bit simultaneous sampling SAR ADC with true bipolar input up to ±12V,these features make it ideal for this kind of system application.

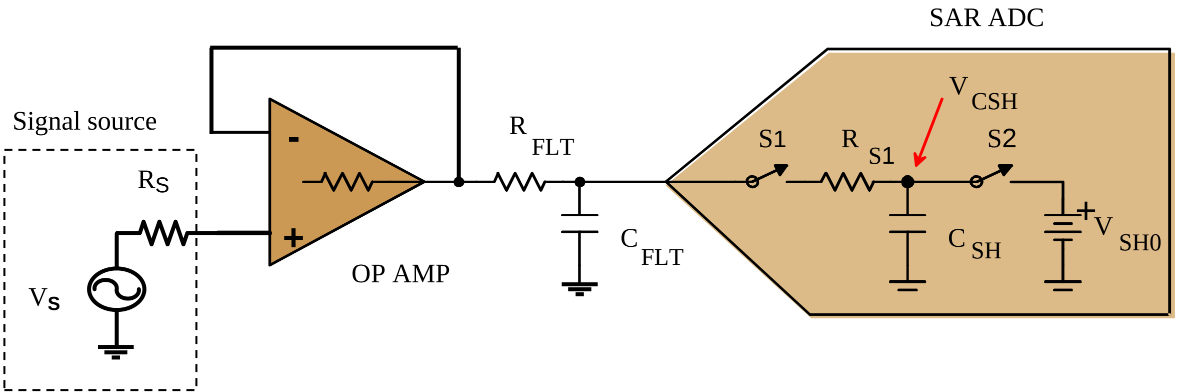


**Figure 1. Typical Driver Circuit for SAR ADC**

SAR ADC's driving circuit generally includes a front-end amplifier in combination with a low-pass RC filter (Figure 1), this driver circuit's major functions include: (a) signal conditioning for input signal from the source; (b) as a filter, including an RC lowpass filter and active filter with amplifier; (c) isolation between signal source and ADC, typical SAR ADC with switched-capacitor network is a dynamic load; (d) provide enough charges to ADC's internal sampling capacitor during ADC's acquisition time. Right selections of components of the drive circuit can make it possible to get optimal system performance, including the value selections of $R_{FLT}$ and $C_{FLT}$.

## 2 Design Challenge for driver circuit without amplifier

To simplify circuit design and save cost, it is popular to design the driver circuit of SAR ADC without any amplifier by engineers in power line measurement and protection systems, only use a passive RC filter. But, if the correct values of $R_{FLT}$ and $C_{FLT}$ are not selected, the system performance suffers in the area of DC and AC performance, THD (total harmonic distortion), and so on.

## 2.1 Driver circuit without amplifier

The circuit in Figure 2 is a typical circuit without amplifier used widely in power line protection systems. The second order RC filters or much bigger value $R_{FLT}$ and $C_{FLT}$ are often used in this kind of application, thus providing bad system performance. The input signal resource ( $V_S$ ) is usually ±10V or ±5V bipolar, 50Hz sine wave signal. To filter the noise and get optimal filter result, a larger value resistor ($R_{FLT}$) and capacitor ($C_{FLT}$) are used. This also provides a lower cutoff frequency of filter. The reason for using this big resistor is the demand of isolation between the SAR ADC and signal resource because there is no front-end amplifier. In general, 48 sample point per cycle is often used, so the sampling rate of the ADC is 2.4ksps for 50Hz sine wave.

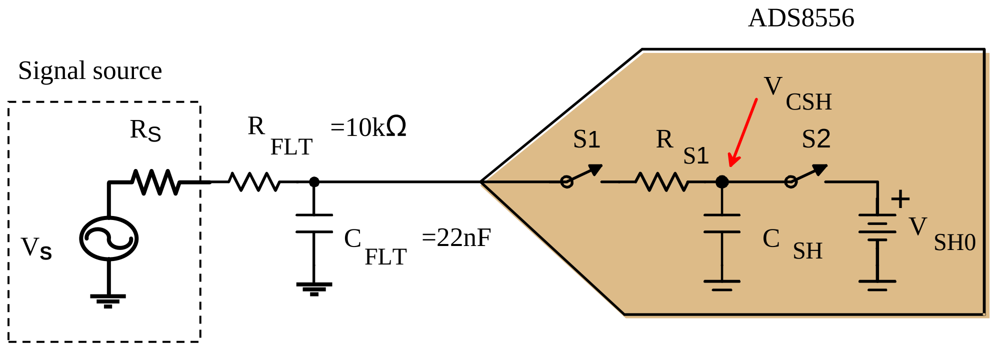


**Figure 2. ADS8556's Driver Circuit Without Front-end Amplifier**

After tests, the system performances are bad for this circuit configuration, especially THD, SINAD (Signal-to-noise and distortion ratio) and SFDR (Spurious Free Dynamic Range) performances (Table 1). If the sampling rate is increased, the performances for the same circuit decrease.

## 2.2 Design Challenges

SAR ADC's sampling rate and acquisition time are important parameters in the design challenges.

### *2.2.1 Sampling rate and Acquisition time*

SAR ADC's sampling rate is usually correlative to ADC's Acquisition time ($t_{ACQ}$) and Conversion time ($t_{CONV}$).

$$T = \frac{1}{f_S} = t_{ACQ} + t_{CONV}$$

$f_S$ is the sampling rate.

For ADS8556,

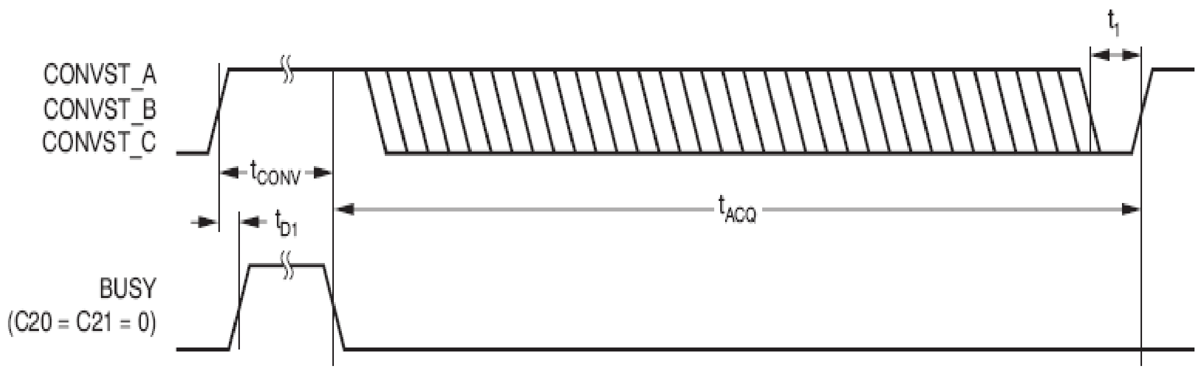


**Figure 3. ADS8556's Acquisition time and Conversion time**

The conversion time (1.26µs) in ADS8556's data sheet is the maximum time ADS8556 needs for one conversion. The acquisition time (280ns) in ADS8556's data sheet is minimum time to specify the excellent performance at the highest sampling rate. The real acquisition time to ADC depends on the real sampling rate because the conversion time is approximately fixed and ADC will enter into the acquisition status automatically after the conversion is finished.

### 2.2.2 Challenges

For the application in Figure 2, the sampling rate ($f_S$) is 2.4ksps, the conversion time ($t_{CONV}$) of ADS8556 is 1.26µs:

$$t_{ACQ} = \frac{1}{f_S} - t_{CONV} = 415.4us$$

Because $$t_{ACQ} \geq k \times \tau$$

Where $t_{ACQ}$ is ADC's acquisition time (Reference 3)

k is time-constant multiplier,11.78 for 16 bit ADC

$\tau$ is time-constant

Calculate the required time constant of ADC:

$$\tau \leq \frac{t_{ACQ}}{k} = \frac{415.4us}{11.78} = 35.26us$$

If $R_S = 0\Omega$, the front-end RC filter's time constant:

$$\tau_{FLT} = (R_S + R_{FLT}) \times C_{FLT} = 10k\Omega \times 22nF = 220us$$

This cannot meet the requirement charging the ADC's internal sampling capacitor to the proper value and maintaining stability during ADC's acquisition time.

Considering the ADC acquisition time first, the cutoff frequency of the RC filter is ($R_S$ = 0Ω):

$$f_{-3dB} = \frac{1}{2\pi R_{FLT} C_{FLT}} = \frac{1}{2\pi\tau_{FLT}} = \frac{1}{2\pi\frac{t_{ACQ}}{k}} = \frac{1}{2\pi \times 35.26us} = 4.514kHz$$

Because no amplifier is used as an active filter in Figure 2, the RC filter acts as all filter functions. The input signal from power lines is only 50Hz frequency signal, so to get a better filter effect, the low cutoff frequency RC filter is often selected by engineers. That is why the larger resistor and capacitor values are used. The cutoff frequency of designed RC filter in Figure 2 is:

$$f_{-3dB} = \frac{1}{2\pi(R_S + R_{FLT})C_{FLT}} = \frac{1}{2\pi \times 10k \times 22nF} = 723.4Hz$$

So for the circuit design of the SAR ADC's driver without an amplifier, it is critical to consider the tradeoff between the RC filter time constant and the cutoff frequency.

## 3 Choose the right RC filter Components

The proper value for $C_{FLT}$ of front-end RC filter can be determined by following equation**:**

$$20 \times C_{SH} \leq C_{FLT} \leq 60 \times C_{SH}$$

Where $C_{SH}$ is SAR ADC's internal sampling capacitor (Reference 3)

It is ideal for $C_{FLT}$ to use a Silver mica or a C0G type capacitor.

The proper value for $R_{FLT}$ of front-end RC filter can be determined by following equation**:**

$$R_{FLT} \approx \frac{t_{ACQ}}{k \times C_{FLT}}$$

Where $t_{ACQ}$ is the ADC acquisition time and k is time-constant multiplier (Reference 3)

# 4 Performance Test

## 4.1 Test System

Figure 3 is the typical test system for AC performance in this report. The software for this report was developed with *Code Composer Studio*™ V3.3 based on TI's TMS320F28335 Digital Signal Precessor (DSP™) in ADS855x test board.The FFT wave forms are created in ADCPro software, which is available for download from the Texas Instruments website www.ti.com.

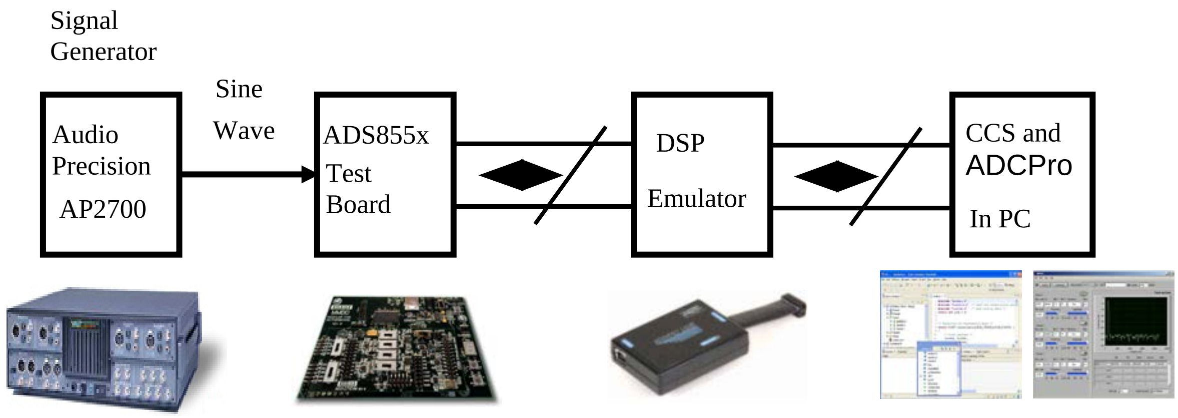


**Figure 4. Performance test system for ADS8556 circuit**

## 4.2 Performance Comparison Test

Table 1 is the system AC performance results based on original design in Figure 2 ($R_{FLT}$ = 10kΩ, $C_{FLT}$ = 22nF) and different input signal amplitudes of $V_S$, which is bipolar and 50Hz signal from AP2700 generator. The ADS8556 sampling rate is 2.4ksps for these tests. From the test data, the system THD, SINAD, SFDR performances are poor.

**Table 1. Test Result for $R_{FLT}$ = 10kΩ, $C_{FLT}$ = 22nF (unit: dBc)**

| $V_S$ （$V_{P-P}$/dBFS） | SNR | THD | SINAD | Tone | Signal power | SFDR |
|---|---|---|---|---|---|---|
| 50mV/−46 | 45.94 | −46.06 | 42.99 | 50.00Hz | −45.85 | 48.4 |
| 100mV/−40 | 51.71 | −52.35 | 49.01 | 50.00Hz | −39.94 | 55.4 |
| 316mV/−30 | 61.83 | −61.11 | 58.44 | 50.00Hz | −30.01 | 64.9 |
| 500mV/−26 | 65.96 | −65.66 | 62.80 | 50.00Hz | −26.03 | 69.7 |
| 1V/−20 | 72.00 | −68.03 | 66.57 | 50.00Hz | −20.02 | 70.0 |
| 3.16V/−10 | 82.22 | −63.10 | 63.04 | 50.00Hz | −10.03 | 63.5 |
| 5V/−6 | 85.65 | −62.10 | 62.08 | 50.00Hz | −6.05 | 62.5 |
| 8.91V/−1 | **89.71** | **−58.57** | **58.57** | **50.00Hz** | **−1.04** | **58.8** |
| 9.44V/−0.5 | 90.25 | −58.18 | 58.18 | 50.00Hz | −0.54 | 58.4 |

If according to the guidelines in item No. 3, reduce the value for $C_{FLT}$ to 1nF (the ADS8556 input capacitor is 20pF for ±5 input range), Table 2 provides new test results:

**Table 2. Test Result for $R_{FLT}$ = 10kΩ, $C_{FLT}$ = 1nF (unit: dBc)**

| $V_S$ ( $V_{P-P}$ /dBFS) | SNR | THD | SINAD | Tone | Signal power | SFDR |
|---|---|---|---|---|---|---|
| 50mV/-46 | 45.69 | -59.64 | 45.52 | 50.00Hz | -45.91 | 68.7 |
| 100mV/-40 | 51.69 | -64.46 | 51.46 | 50.00Hz | -39.93 | 73.4 |
| 316mV/-30 | 61.73 | -72.60 | 61.39 | 50.00Hz | -29.99 | 78.0 |
| 500mV/-26 | 65.42 | -76.71 | 65.11 | 50.00Hz | -26.01 | 83.9 |
| 1V/-20 | 71.59 | -83.71 | 71.33 | 50.00Hz | -20.00 | 90.5 |
| 3.16V/-10 | 82.21 | -92.62 | 80.91 | 50.00Hz | -10.00 | 96.1 |
| 5V/-6 | 84.92 | -95.03 | 84.52 | 50.00Hz | -6.02 | 97.3 |
| 8.91V/-1 | **89.30** | **-94.25** | **88.09** | **50.00Hz** | **-1.00** | **98.9** |
| 9.44V/-0.5 | 90.01 | -93.42 | 88.38 | 50.00Hz | -0.50 | 94.4 |

Table 2 shows that the system performance is significantly improved. The THD improvement with -1dBFS input is about 35dB, SFDR improvement is about 40dB.

Continue reducing the value for $C_{FLT}$ to 680pF according to the guidelines (the ADS8556 input capacitor is 20pF for ±5 input range):

**Table 3. Test Result for $R_{FLT}$ = 10kΩ, $C_{FLT}$ = 680pF (unit: dBc)**

| $V_S$ ( $V_{P-P}$ /dBFS) | SNR | THD | SINAD | Tone | Signal power | SFDR |
|---|---|---|---|---|---|---|
| 50mV/-46 | 45.20 | -62.45 | 45.12 | 50.00Hz | -45.91 | 72.0 |
| 100mV/-40 | 51.35 | -68.71 | 51.27 | 50.00Hz | -39.94 | 76.5 |
| 316mV/-30 | 61.33 | -74.35 | 61.12 | 50.00Hz | -29.99 | 80.1 |
| 500mV/-26 | 65.18 | -76.82 | 64.89 | 50.00Hz | -26.01 | 84.1 |
| 1V/-20 | 71.17 | -83.88 | 70.94 | 50.00Hz | -20.00 | 92.7 |
| 3.16V/-10 | 81.08 | -93.43 | 80.83 | 50.00Hz | -9.99 | 100.8 |
| 5V/-6 | 84.87 | -96.85 | 84.60 | 50.00Hz | -6.02 | 103.5 |
| 8.91V/-1 | **89.24** | **-101.16** | **88. 97** | **50.00Hz** | **-1.00** | **107.8** |
| 9.44V/-0.5 | 89.27 | -100.81 | 88.97 | 50.00Hz | -0.50 | 107.7 |

The THD and SFDR performances are much better than before.THD improvement with -1dBFS input is about 42dB, SFDR is about 49dB, so 680pF $C_{FLT}$ is a perfect choice for better system performance.

## 5 Conclusion

This application report presents a popular driver circuit without amplifier to SAR ADC in industrial application, discusses the challenges which may meet between the performance demand and RC filter design. Based on the input signal, the ADC sampling rate and the input capacitor, the system performance demand and the filter demand, it is important to balance the values of $R_{FLT}$ and $C_{FLT}$.This application report is also suitable for ADS8557 and ADS8558 TI's SAR ADCs.

## 6 References

1. ADS8556 data sheet (SBAS404B)
2. ADS8555 data sheet (SBAS531B)
3. Oljaca, M. and B. Baker. (2008). Start with the right op amp when driving SAR ADCs. EDN. October 16, 2008. Pp. 43-58.
   Download at: www.edn.com/article/CA6602451

# Appendix A. FFT for test data

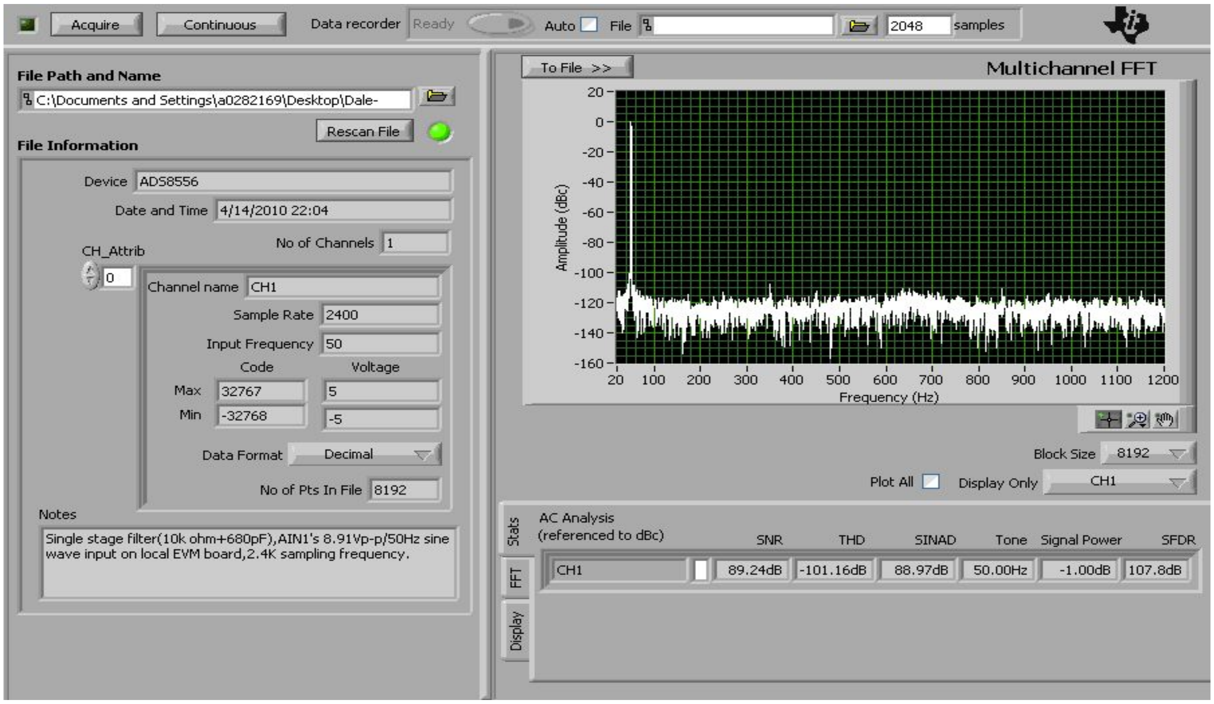


**Figure A-1. FFT for $R_{FLT}$ = 10kΩ, $C_{FLT}$ = 680pF ($V_S$ = -1dBFS)**

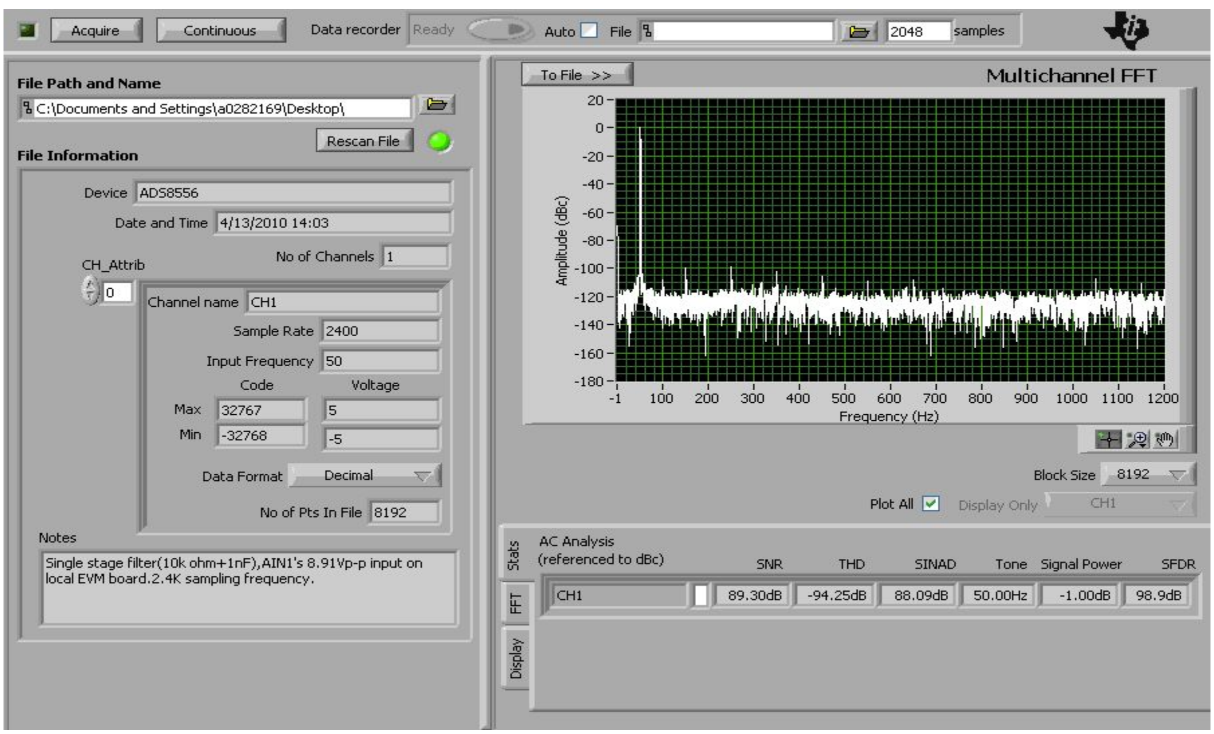


**Figure A-2. FFT for $R_{FLT}$ = 10kΩ, $C_{FLT}$ = 1nF ($V_S$ = -1dBFS)**

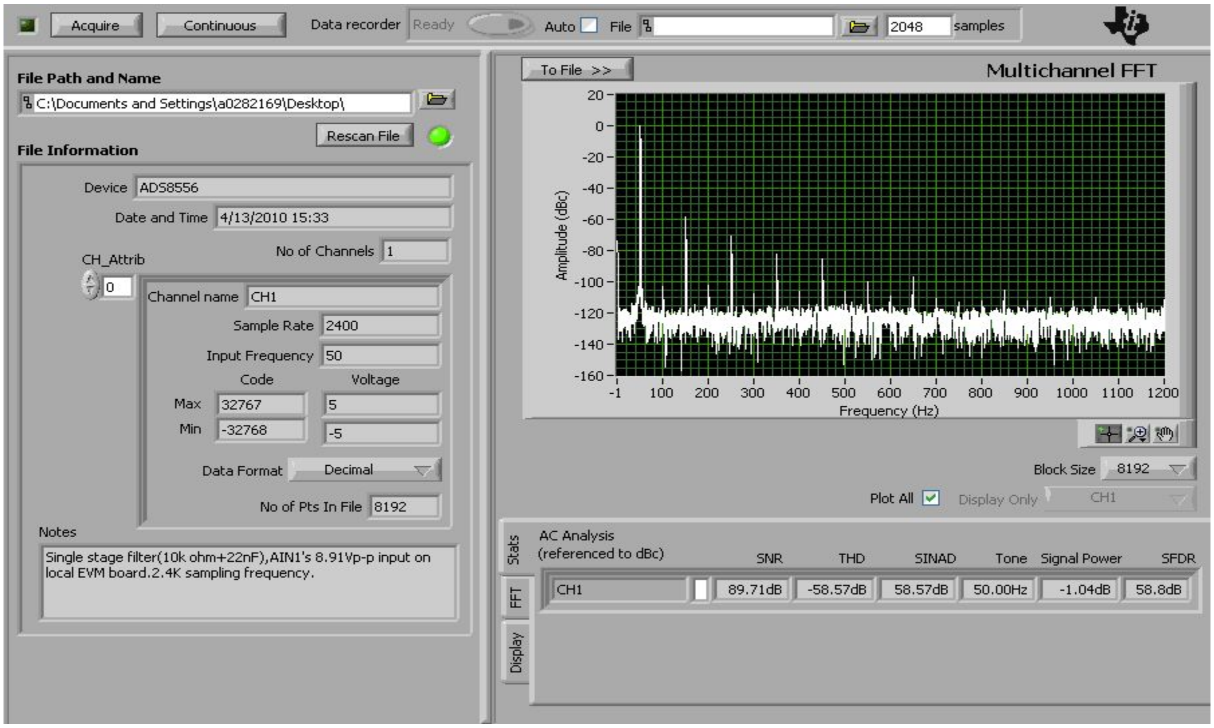


**Figure A-3. FFT for $R_{FLT}$ = 10kΩ, $C_{FLT}$ = 22nF ($V_S$ = -1dBFS)**

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