Configuring I²S to Generate BCLK from TLV320AIC32/33/31/3101/3104/3105/3106/3204/3254/DAC32 Devices and WCLK from McBSP Port

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ABSTRACT

This application note describes a method for interfacing the multichannel buffered serial port (McBSP) to the I²S™ interface of the TLV320AIC32/33/31, the TLV320AIC3101/3104/3105/3106/3204/3254 and DAC32 devices such that the bit clock (BCLK) is generated by the audio data converter device and the word clock (WCLK) is generated by the McBSP.

This type of interface is useful in applications where the host processor (with a McBSP interface) can synchronize the audio (with video, for example) by controlling the WCLK, whereas the data converter device can generate the BCLK depending on the I²S configuration. The McBSP interface is supported in a variety of processors from Texas Instruments, such as the TMS320C5000/C6000™ digital signal processors (DSPs), the DaVinci™ digital media processors, and OMAP applications processors.

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1 Introduction

The TLV320AIC32/33/31/3101/3104/3105/3106/3204/3254 codecs and TLV320DAC32 digital-to-analog converter (DAC) from TI provide a glueless interface to applications with McBSPs. The digital audio interface in these devices is programmable to work with popular audio standard protocols (I^2S, DSP, Left-/Right-Justified, and TDM) and 16-, 20-, 24- and 32- bit data widths. Furthermore, Word-Clock (WCLK) and Bit-Clock (BCLK) can be independently configured in either Master or Slave Mode for flexible connectivity to a wide variety of processors. An on-chip PLL enables generation of audio clocks from a variety of system clocks from 512 kHz to 50 MHz.

The flexibility of the digital audio interface and the on-chip PLL facilitates a host processor with a McBSP interface to provide a single master clock (MCLK) to the audio data converter device in order to generate both the internal audio clock as well as the clock for the digital interface (BCLK). This flexibility eliminates the need to generate BCLK using clock multipliers/dividers within or outside of the host processor.

In addition, because BCLK and WCLK can be configured in either Master or Slave mode independent of each other, the host processor can generate WCLK from BCLK. This feature enables the host processor to control audio streaming by synchronizing audio with other signals, such as video in a multimedia application.

This application report presents the hardware connections and software configurations necessary to enable the digital audio interface as discussed. The host processor under consideration is a TMS320C55x, and the audio data converter device is the TLV320AIC3254. The TLV320AIC3254 is a high-performance audio codec with 16-bit stereo playback and record functionality. The device integrates several analog features such as a microphone interface, input analog mux, low-noise gain stage, headphone drivers, line level drivers, and volume controls.

2 Application Setup

The McBSP on the TMS320C55x is connected to the TLV320AIC3254 through digital audio interface signals, as shown in Figure 1.

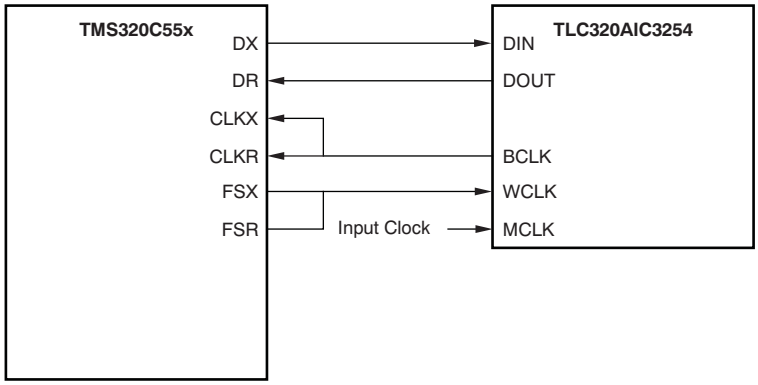

Figure 1. McBSP Connection to TLV320AIC3254 Codec

In the application shown, MCLK is provided by a timer output from the TMS320C55x. The TMS320C55x runs from a 200-MHz clock; the timer divides this clock by 16 to provide an MCLK of 12.5 MHz.

2.1 AIC Configuration

The TLV320AIC3254 uses its internal PLL to run the codec at 44.1 kHz. The codec also generates the BCLK. The TLV320AIC3254 clock configuration is summarized in Table 1.

Table 1. AIC Clock Configuration

Name	Value	Location	Description
PLL_CLKIN	0 (Default)	Pg 0, Reg 4, D3-D2	PLL_CLKIN = MCLK
CODEC_CLKIN	3	Pg 0, Reg 4, D1-D0	CODEC_CLKIN = PLL_CLK
PLL Power Up	1	Pg 0, Reg 5, D7	PLL is powered up
PLL P-Val	1	Pg 0, Reg 5, D6-D4	PLL Divider P
PLL R-Val	1	Pg 0, Reg 5, D3-D0	PLL Multiplier R
PLL J-Val	7	Pg 0, Reg 6, D5-D0	PLL Multiplier J
PLL D-Val MSB	8	Pg 0, Reg 7, D5-D0	PLL Fractional Multiplier D(13:8)
PLL D-Val LSB	206	Pg 0, Reg 8, D7-D0	PLL Fractional Multiplier (D7–D0) D = 8 × 256 + 206 = 2254 PLL_CLK = PLL_CLKIN x (R x J.D) / P = 12.5 x 1 x 7.2254 / 1 = 90.3175 MHz
NDAC Power Up	1	Pg 0, Reg 11, D7	NDAC Divider is powered up
NDAC-Val	8	Pg 0, Reg 11, D6-D0	NDAC-Val = 8 DAC_CLK = PLL_CLK/NDAC = 11.2896 MHz
MDAC Power Up	1	Pg 0, Reg 12, D7	MDAC Divider is powered up
MDAC-Val	2	Pg 0, Reg 12, D6-D0	MDAC-Val = 2 DAC_MOD_CLK = DAC_CLK/MDAC = 5.6448 MHz DAC_Fs = DAC_MOD_CLK/DOSR (= 128, default value) = 44.1 kHz

The corresponding clock-tree diagram that highlights the configured path is shown in Figure 2.

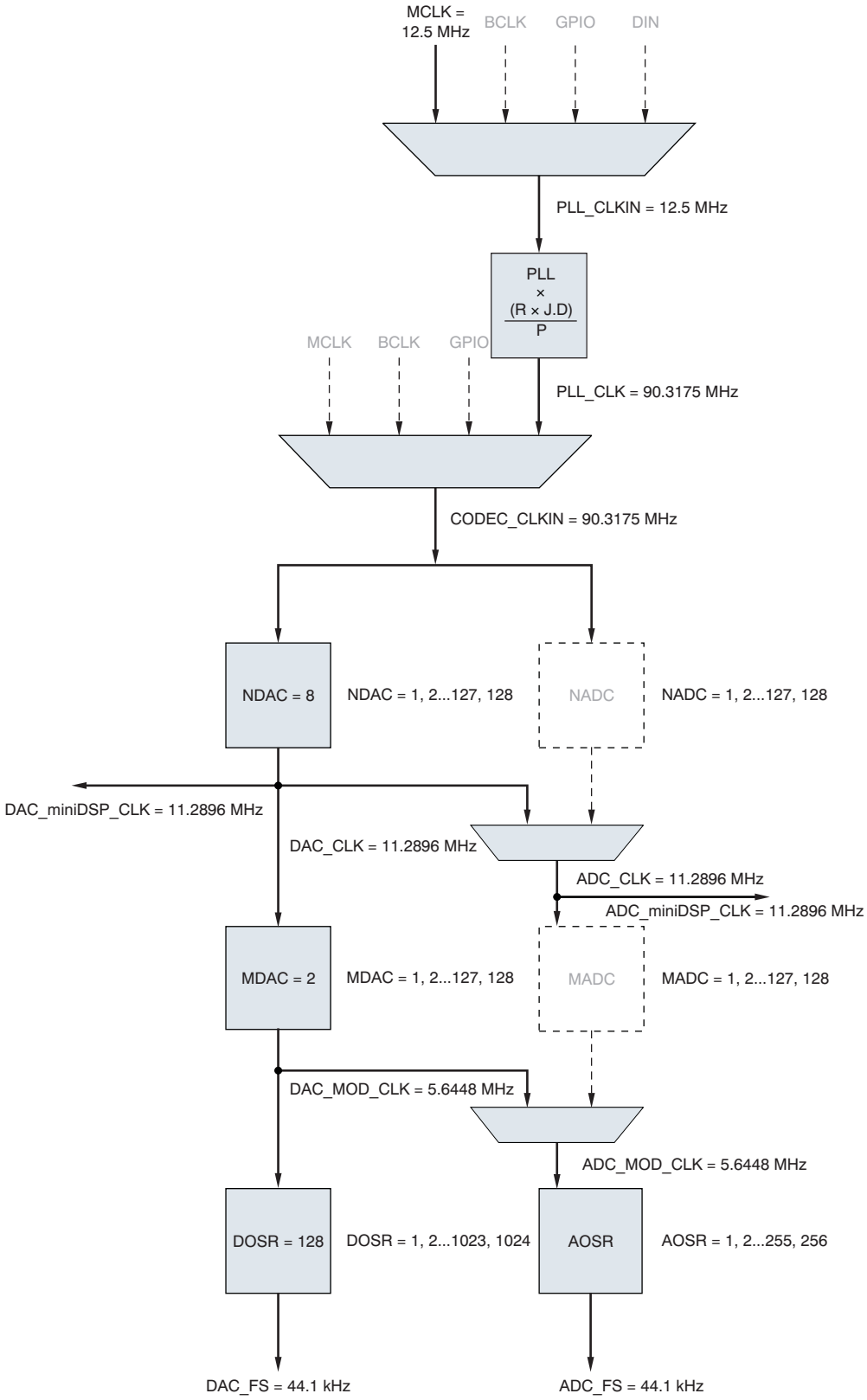

Figure 2. TLV320AIC3254 Clock Tree

The TLV320AIC3254 digital audio interface configuration is given in Table 2.

Table 2. AIC Digital Audio Interface Configuration

Name	Value	Location	Description
Codec Interface	0 (Default)	Pg 0, Reg 27, D7-D6	Codec Interface = I^2S
Codec Interface Word Length	0 (Default)	Pg 0, Reg 27, D5-D4	Codec Interface Word Length = 16 bits
BCLK Direction	1	Pg 0, Reg 27, D3	BCLK is output
WCLK Direction	0	Pg 0, Reg 27, D2	WCLK is input
BDIV_CLKIN	1	Pg 0, Reg 29, D1-D0	BDIV_CLKIN = DAC_MOD_CLK
BCLK Power Up	1	Pg 0, Reg 30, D7	BCLK Divider is powered up
BCLK-N-Val	4	Pg 0, Reg 30, D6-D0	BCLK-N-Val = 4 BCLK = DAC_MOD_CLK / BCLK-N = 1.4112 MHz (32 clocks in a 44.1-kHz. frame, 16 clocks for Left Channel, 16 clocks for Right Channel)

The BCLK generation diagram is shown in Figure 3.

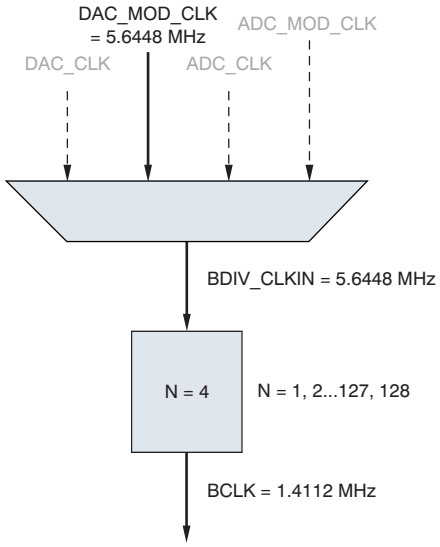

Figure 3. TLV320AIC3254 BCLK Generation

Note: The configurations presented in this section are not the only configurations required for normal operation of the TLV321AIC3254 codec. Other blocks such as analog routing, digital processor, and so forth must also be configured and powered up for the codec to function properly.

2.2 McBSP Configuration

The McBSP must be configured for I^2S mode to accept the BCLK as an input for CLKX/CLKR and to generate the WCLK through FSX/FSR. The detailed configurations of the McBSP registers are listed in Table 3 to Table 11.

Table 3. McBSP Serial Port Control Register 1 (SPCR1x)

Name	Value	Bit	Description
DLB	0	15	Digital Loop Back mode disabled
RJUST	01b	14-13	Right-justify the data and sign-extend the data into the MSBs
CLKSTP	00b	12-11	Normal clocking for non-SPI mode
Reserved	xxx	10-8	Reserved
DXENA	0	7	DX Enabler is off
Reserved	x	6	Reserved (write 0)
RINTM	10b	5-4	McBSP sends RINT request to CPU when receive frame-sync pulse is detected
RSYNCERR	0	3	No synchronization error
RFULL	x	2	Read-only
RRDY	x	1	Read-only
RRST	0	0	Serial port receiver is disabled

Table 4. McBSP Serial Port Control Register 2 (SPCR2x)

Name	Value	Bit	Description
Reserved	xxxxxx	15-10	Reserved
FREE	1	9	Free running
SOFT	x	8	Don't care when FREE is 1
FRST	0	7	Frame Sync Logic is Reset
GRST	0	6	Sample Rate Generator is Reset
XINTM	10b	5-4	McBSP sends XINT request to CPU when transmit frame-sync pulse is detected
XSYNCERR	0	3	No synchronization error
XEMPTY	x	2	Read-only
XRDY	x	1	Read-only
XRST	0	0	Serial port transmitter is disabled

Table 5. McBSP Receive Control Register 1 (RCR1x)

Name	Value	Bit	Description
Reserved	x	15	Reserved
RFRLEN1	0000001b	14-8	Two words per frame(1)
RWDLEN1	010b	7-5	16 bits per word(1)
Reserved	xxxxx	4-0	Reserved

(1) Configurations specific to I^2S.

Table 6. McBSP Receive Control Register 2 (RCR2x)

Name	Value	Bit	Description
RPHASE	0	15	Single phase frame
RFRLEN2	xxxxxx	14-8	Don't care for single phase frame
RWDLEN2	xxx	7-5	Don't care for single phase frame
RCOMPAND	00b	4-3	No companding, MSB received first
RFIG	0	2	Frame sync detect
RDATDLY	01b	1-0	1-bit data delay

Table 7. McBSP Transmit Control Register 1 (XCR1x)

Name	Value	Bit	Description
Reserved	x	15	Reserved
XFRLEN1	0000001b	14-8	Two words per frame(1)
XWDLEN1	010b	7-5	16 bits per word(1)
Reserved	xxxxx	4-0	Reserved

(1) Configurations specific to I^2S.

Table 8. McBSP Transmit Control Register 2 (XCR2x)

Name	Value	Bit	Description
XPHASE	0	15	Single phase frame
XFRLEN2	xxxxxx	14-8	Don't care for single phase frame
XWDLEN2	xxx	7-5	Don't care for single phase frame
XCOMPAND	00b	4-3	No companding, MSB transmitted first
XFIG	0	2	Frame sync detect
XDATDLY	01b	1-0	1-bit data delay

Table 9. McBSP Sample Rate Generator Register 1 (SRGR1x)

Name	Value	Bit	Description
FWID	00001111b	15-8	Frame Sync Pulse Width = 16 CLKG cycles(1)
CLKGDV	00000000b	7-0	CLKG frequency = Input clock frequency(2)

(1) Configurations specific to I^2S.
(2) Configurations specific to receive BCLK for CLKX/CLKR and generate WCLK through FSX/FSR.

Table 10. McBSP Sample Rate Generator Register 2 (SRGR2x)

Name	Value	Bit	Description
GSYNC	0	15	No clock synchronization
CLKSP	x	14	Don't care because CLKS is not used as input clock
CLKSM	1	13	Input for CLKG on CLKX pin (SCLKME = 1)(1)
FSGM	1	12	Frame sync pulse generated by the sample rate generator(1)
FPER	000000011111b	11-0	Frame Sync Period = 32 CLKG cycles(2)

(1) Configurations specific to receive BCLK for CLKX/CLKR and generate WCLK through FSX/FSR.
(2) Configurations specific to I^2S.

Table 11. McBSP Pin Control Register (PCRx)

Name	Value	Bit	Description
Reserved	x	15	Reserved
IDLEEN	0	14	McBSP active when PERIPH domain is idle
XIOEN	0	13	DX, FSX, CLKX are not GPIO pins
RIOEN	0	12	DR, FSR, CLKR are not GPIO pins
FSXM	1	11	Internal transmit frame sync signal(1)
FSRM	1	10	Internal receive frame sync signal(1)
CLKXM	0	9	External transmit clock signal(1)
CLKRM	0	8	External receive clock signal (1)
SCLKME	1	7	Input for CLKG on CLKX pin (CLKSM = 1)(1)
CLKSSTAT	x	6	Read-only
DXSTAT	x	5	Read-only
DRSTAT	x	4	Read-only
FSXP	1	3	Transmit frame sync is active low(2)
FSRP	1	2	Receive frame sync is active low(2)
CLKXP	1	1	Transmit data driven on falling edge of CLKX(2)
CLKRP	1	0	Receive data sampled on rising edge of CLKR(2)

(1) Configurations specific to receive BCLK for CLKX/CLKR and generate WCLK through FSX/FSR.
(2) Configurations specific to I^2S.

2.3 McBSP Startup Sequence

The McBSP configuration described in Section 2.2 is during initialization of the McBSP interface. Apart from initialization, a timing sequence must be followed for proper startup of the McBSP interface:

- First, initialize the McBSP registers as shown in Section 2.2. This configuration resets the Sample Rate Generator and the Frame Sync Logic, and keeps the Transmitter and the Receiver in a disabled state. It also configures the McBSP interrupt generator to send an interrupt to the CPU when a frame sync pulse is detected
- Then, enable the Sample Rate Generator and Frame Sync Logic (GRST = FRST = 1 in SPCR2x). This register can be enabled when the host is ready to send/receive audio that is synchronized with other events (for example, video in a multimedia application). The Sample Rate generator will receive the BCLK through CLKX and will generate the WCLK through the internal Frame Sync Logic.
- The first frame sync pulse generated internally interrupts the CPU. The interrupt service routine enables the Transmitter and Receiver, and audio transfer is initiated with the TLV320AIC3254 (RRST = 1 in SPCR1x, XRST = 1 in SPCR2x). Also, the CPU interrupt for a frame sync pulse is disabled because synchronization of the McBSP relative to the frame sync pulse has been achieved.
- Typically, the McBSP Transmitter and the Receiver are connected to a pair of direct memory access (DMA) controllers for block transfers to/from memory. The McBSP Transmitter signals the Transmitter DMA to send the next set of stereo data and the McBSP Receiver signals the Receiver DMA to receive the next set of stereo data. The Transmitter DMA copies stereo samples from memory to the McBSP registers, while the Receiver DMA copies stereo samples from the McBSP registers to memory. After a block of audio samples is sent/received through the McBSP interface, the respective DMA controllers interrupt the CPU for further action.
- The McBSP operation can be stopped by disabling the Transmitter and the Receiver (RRST = 0 in SPCR1x, XRST = 0 in SPCR2x).

3 Conclusion

This report discusses a digital audio interface scheme that enables BCLK to be generated by the audio data converter device and WCLK to be generated by the McBSP interface of a host processor. This recommended scheme provides flexibility to the host processor in two ways:

1. It allows the user to provide a single MCLK to the audio converter device in order to generate BCLK (through the internal PLL of the audio data converter device), and thereby avoids multipliers/dividers to generate BCLK from the system clock; and
2. It enables the user to have control of audio transmission and reception through the WCLK, thus having the ability to synchronize audio with other events (such as video in a multimedia application).

4 References

The following documents are available for download at the Texas Instruments web site (www.ti.com).

1. TLV320AIC3254 Data Manual (SLAS549)
2. TMS320VC5501/5502/5503/5507/5509/5510 DSP Multichannel Buffered Serial Port (McBSP) Reference Guide (SPRU592)

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