Functional Safety Information

TCAN1476-Q1 and TCAN1476V-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for the TCAN1476-Q1 and TCAN1476V-Q1 (VSON (14, DMT) package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 and Figure 1-2 show the device functional block diagram for reference.

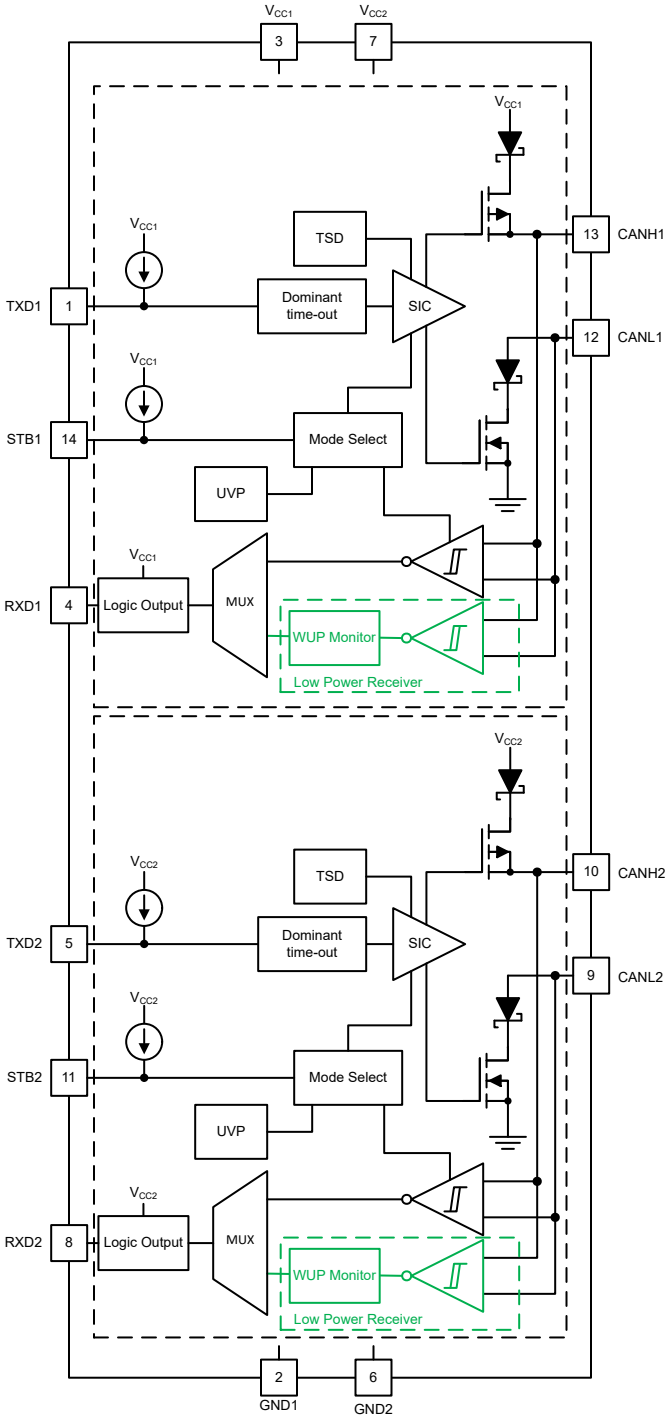

Figure 1-1. TCAN1476-Q1 Functional Block Diagram

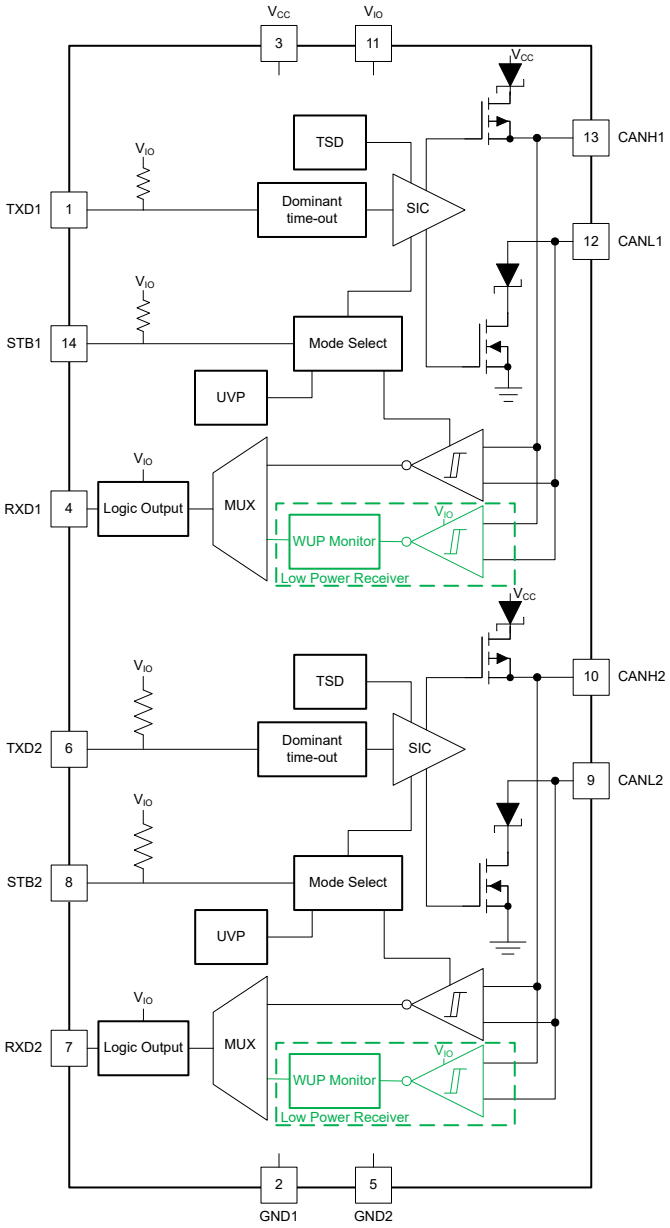

Figure 1-2. TCAN1476V-Q1 Functional Block Diagram

The TCAN1476-Q1 and TCAN1476V-Q1 were developed using a quality-managed development process, but were not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 VSON (14, DMT) Package

This section provides functional safety failure in time (FIT) rates for the VSON (14, DMT) package of the TCAN1476-Q1 and TCAN1476V-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	8
Die FIT rate	3
Package FIT rate	5

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 250mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	BICMOS Bus driver or receiver	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TCAN1476-Q1 and TCAN1476V-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Transmitter fail	52
Receiver fail	13
Power management or state control fail	15
Input and output buffer fail	20

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TCAN1476-Q1 and TCAN1476V-Q1 (VSON (14, DMT) package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2 and Table 4-7)
- Pin open-circuited (see Table 4-3 and Table 4-8)
- Pin short-circuited to an adjacent pin (see Table 4-4 and Table 4-9)
- Pin short-circuited to V_{CC} (see Table 4-5 and Table 4-10)
- Pin short-circuited to V_{IO} (see Table 4-11)
- Pin short-circuited to V_{BAT} (see Table 4-6 and Table 4-12)

Table 4-2 through Table 4-12 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- V_{CC} = 4.5V to 5.5V
- V_{IO} = 1.7V to 5.5V
- V_{BAT} = 6V to 24V

4.1 TCAN1476-Q1 (VSON (14, DMT) Package)

Figure 4-1 shows the TCAN1476-Q1 pin diagram for the VSON (14, DMT) package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TCAN1476-Q1 datasheet.

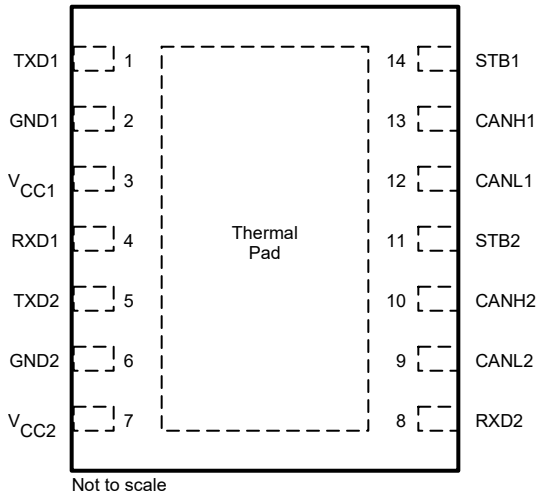

Figure 4-1. Pin Diagram (VSON (14, DMT) Package)

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
TXD1	1	The CAN1 driver enters dominant timeout, disabling the driver. Data cannot be transmitted on the CAN1 bus.	B
GND1	2	None.	D
V_{CC1}	3	The CAN1 transceiver becomes unpowered and a high system-level supply current potentially occurs.	B
RXD1	4	By default, the RXD pin is high-side FET ON. With a pin short-circuit to ground, a direct path forms between supply and ground, causing high current flow.	A
TXD2	5	The CAN2 driver enters dominant timeout, disabling the driver. Data cannot be transmitted on the CAN2 bus.	B
GND2	6	None.	D
V_{CC2}	7	The CAN2 transceiver becomes unpowered and a high system-level supply current potentially occurs.	B
RXD2	8	By default, the RXD pin is high-side FET ON. With a pin short-circuit to ground, a direct path forms between supply and ground, causing high current flow.	A
CANL2	9	The $V_{CANL(R)}$ specification is violated. The EMC performance of the transceiver potentially degrades.	C
CANH2	10	The device cannot drive a dominant signal to the CAN2 bus, so communication on the CAN2 bus is not possible.	B
STB2	11	The STB2 pin is stuck low, so the CAN2 transceiver is unable to enter low-power mode.	B
CANL1	12	The $V_{CANL(R)}$ specification is violated. The EMC performance of the transceiver potentially degrades.	C
CANH1	13	The device cannot drive a dominant signal to the CAN1 bus, so communication on the CAN1 bus is not possible.	B
STB1	14	The STB1 pin is stuck low, so the CAN1 transceiver is unable to enter low-power mode.	B
Thermal Pad	-	None.	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
TXD1	1	The TXD1 pin defaults high; the CAN1 driver is always recessive and unable to transmit data.	B
GND1	2	The CAN1 transceiver is not powered.	B
V_{CC1}	3	The CAN1 transceiver is not powered.	B
RXD1	4	There is no RXD1 pin connection to the MCU. The MCU is unable to read data from the CAN1 bus using the RXD1 pin.	B
TXD2	5	The TXD2 pin defaults high; the CAN2 driver is always recessive and unable to transmit data.	B
GND2	6	The CAN2 transceiver is not powered.	B
V_{CC2}	7	The CAN2 transceiver is not powered.	B
RXD2	8	There is no RXD2 pin connection to the MCU. The MCU is unable to read data from the CAN2 bus using the RXD2 pin.	B
CANL2	9	The device cannot drive a dominant signal on the CAN2 bus, so communication on the CAN2 bus is not possible.	B
CANH2	10	The device cannot drive a dominant signal on the CAN2 bus, so communication on the CAN2 bus is not possible.	B
STB2	11	The STB2 pin defaults high; the CAN2 transceiver is stuck in low-power mode.	B
CANL1	12	The device cannot drive a dominant signal on the CAN1 bus, so communication on the CAN1 bus is not possible.	B
CANH1	13	The device cannot drive a dominant signal on the CAN1 bus, so communication on the CAN1 bus is not possible.	B
STB1	14	The STB1 pin defaults high; the CAN1 transceiver is stuck in low-power mode.	B
Thermal Pad	-	None.	D

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
TXD1	1	GND1	The CAN1 driver enters dominant timeout, disabling the driver. Data cannot be transmitted on the CAN1 bus.	B
GND1	2	V_{CC1}	The CAN1 transceiver becomes unpowered, and high I_{CC} current flow is possible.	B
V_{CC1}	3	RXD1	The output of the RXD1 pin becomes stuck high. The MCU is unable to receive data from the CAN1 bus using the RXD1 pin.	B
RXD1	4	TXD2	The output of the RXD1 pin reflects the input to the TXD2 pin, a separate CAN channel. Information from the CAN1 bus is not received correctly by the MCU, or information from the MCU to the CAN2 bus is potentially disrupted, or both.	B
TXD2	5	GND2	The CAN2 driver enters dominant timeout, disabling the driver. Data cannot be transmitted on the CAN2 bus.	B
GND2	6	V_{CC2}	The CAN2 transceiver becomes unpowered and a high system-level supply current potentially occurs.	B
RXD2	8	CANL2	The messages on the RXD2 pin are corrupted by the CANL2 pin. The reception of data from the CAN2 bus using the RXD2 pin is not possible. I_{OS} current is potentially reached.	B
CANL2	9	CANH2	The CAN2 bus becomes stuck recessive and no communication is possible. I_{OS} current is potentially reached when the CAN2 driver is transmitting.	B
CANH2	10	STB2	The CAN2 transceiver potentially turns off when a dominant signal is driven on the CAN2 bus. The device potentially does not enter or stay in the desired mode for the CAN2 bus.	B
STB2	11	CANL1	The CAN2 transceiver potentially turns off when the CAN1 bus is recessive. The device potentially does not enter or stay in the desired mode for the CAN2 bus.	B
CANL1	12	CANH1	The CAN1 bus becomes stuck recessive and no communication is possible. I_{OS}current is potentially reached when the CAN1 driver is transmitting.	B
CANH1	13	STB1	The CAN1 transceiver potentially turns off when a dominant signal is driven on the CAN1 bus. The device potentially does not enter or stay in the desired mode for the CAN1 bus.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to V_{CC}

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
TXD1	1	The TXD1 pin becomes stuck high. The device is unable to transmit data on the CAN1 bus.	B
GND1	2	The CAN1 transceiver becomes unpowered, and high I_{CC} is possible.	B
V_{CC1}	3	None	D
RXD1	4	The RXD1 pin becomes stuck high. The MCU is unable to read data from the CAN1 bus using the RXD1 pin.	B
TXD2	5	The TXD2 pin becomes stuck high. The device is unable to transmit data on the CAN2 bus.	B
GND2	6	The CAN2 transceiver becomes underpowered, and high I_{CC} is possible.	B
V_{CC2}	7	None	D
RXD2	8	The RXD2 pin becomes stuck high. The MCU is unable to read data from the CAN2 bus using the RXD2 pin.	B
CANL2	9	The device cannot drive a dominant signal to the CAN2 bus, so no communication is possible. The CAN2 bus potentially becomes stuck recessive during the fault.	B
CANH2	10	The $V_{CANL(R)}$ specification is violated. The EMC performance of the transceiver potentially degrades.	C
STB2	11	The STB2 pin is stuck high. The CAN2 transceiver becomes stuck in low-power mode.	B
CANL1	12	The device cannot drive a dominant signal to the CAN1 bus, so no communication is possible. The CAN1 bus potentially becomes stuck recessive during the fault.	B
CANH1	13	The $V_{CANL(R)}$ specification is violated. The EMC performance of the transceiver potentially degrades.	C

Table 4-5. Pin FMA for Device Pins Short-Circuited to V_{CC} (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
STB1	14	The STB1 pin is stuck high. The CAN1 transceiver becomes stuck in low-power mode.	B

Table 4-6. Pin FMA for Device Pins Short-Circuited to V_{BAT}

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
TXD1	1	An absolute maximum violation occurs. The device is potentially damaged. The device potentially cannot transmit data on the CAN1 bus.	A
GND1	2	The device becomes unpowered. High I_{BAT} current is possible.	B
V_{CC1}	3	An absolute maximum violation occurs. The device is potentially damaged. The CAN1 bus potentially cannot communicate.	A
RXD1	4	An absolute maximum violation occurs. The device is potentially damaged. The MCU potentially cannot receive data from the CAN1 bus.	A
TXD2	5	An absolute maximum violation occurs. The device is potentially damaged. The device potentially cannot transmit data on the CAN2 bus.	A
GND2	6	The device becomes unpowered. High I_{BAT} current is possible.	B
V_{CC2}	7	An absolute maximum violation occurs. The device is potentially damaged. The CAN1 bus potentially cannot communicate.	A
RXD2	8	An absolute maximum violation occurs. The device is potentially damaged. The MCU potentially cannot receive data from the CAN2 bus.	A
CANL2	9	The CAN2 bus becomes stuck recessive. No communication is possible. I_{OS} current is potentially reached.	B
CANH2	10	The $V_{CANL(R)}$ specification is violated. The EMC performance of the transceiver potentially degrades.	C
STB2	11	An absolute maximum violation occurs. The device is potentially damaged. The CAN2 transceiver becomes stuck in low-power mode.	A
CANL1	12	The CAN2 bus becomes stuck recessive. No communication is possible. I_{OS} current is potentially reached.	B
CANH1	13	The $V_{CANL(R)}$ specification is violated. The EMC performance of the transceiver potentially degrades.	C
STB1	14	An absolute maximum violation occurs. The device is potentially damaged. The CAN1 transceiver becomes stuck in low-power mode.	A

4.2 TCAN1476V-Q1 (VSON (14, DMT) Package)

Figure 4-2 shows the TCAN1476V-Q1 pin diagram for the VSON (14, DMT) package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TCAN1476V-Q1 datasheet.

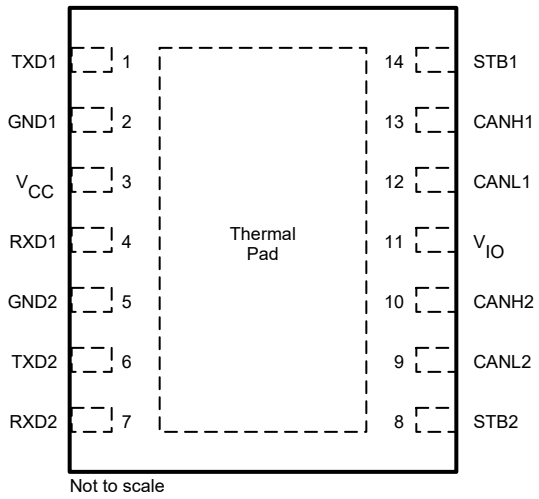

Figure 4-2. Pin Diagram (VSON (14, DMT) Package)

Table 4-7. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
TXD1	1	The CAN1 driver enters dominant timeout, disabling the driver. Data cannot be transmitted on the CAN1 bus.	B
GND1	2	None.	D
V_{CC}	3	The device becomes unpowered and a high system-level supply current potentially occurs.	B
RXD1	4	By default, the RXD pin is high-side FET ON. With a pin short-circuit to ground, a direct path forms between supply and ground, causing high current flow.	A
TXD2	5	The CAN2 driver enters dominant timeout, disabling the driver. Data cannot be transmitted on the CAN2 bus.	B
GND2	6	None.	D
RXD2	7	By default, the RXD pin is high-side FET ON. With a pin short-circuit to ground, a direct path forms between supply and ground, causing high current flow.	A
STB2	8	The STB2 pin is stuck low, so the CAN2 transceiver is unable to enter low-power mode.	B
CANL2	9	The $V_{CANL(R)}$ specification is violated. The EMC performance of the transceiver potentially degrades.	C
CANH2	10	The device cannot drive a dominant signal to the CAN2 bus, so communication on the CAN2 bus is not possible.	B
V_{IO}	11	The device enters protected mode. The transceiver is passive on both the CAN1 and CAN2 buses.	B
CANL1	12	The $V_{CANL(R)}$ specification is violated. The EMC performance of the transceiver potentially degrades.	C
CANH1	13	The device cannot drive a dominant signal to the CAN1 bus, so communication on the CAN1 bus is not possible.	B
STB1	14	The STB1 pin is stuck low, so the CAN1 transceiver is unable to enter low-power mode.	B
Thermal Pad	-	None.	D

Table 4-8. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
TXD1	1	The TXD1 pin defaults high; the CAN1 driver is always recessive and unable to transmit data.	B
GND1	2	The CAN1 transceiver is not powered.	B
V_{CC}	3	The device is not powered.	B
RXD1	4	There is no RXD1 pin connection to the MCU. The MCU is unable to read data from the CAN1 bus using the RXD1 pin.	B
TXD2	5	The TXD2 pin defaults high; the CAN2 driver is always recessive and unable to transmit data.	B
GND2	6	The CAN2 transceiver is not powered.	B
RXD2	7	There is no RXD2 pin connection to the MCU. The MCU is unable to read data from the CAN2 bus using the RXD2 pin.	B
STB2	8	The STB2 pin defaults high; the CAN2 transceiver is stuck in low-power mode.	B
CANL2	9	The device cannot drive a dominant signal on the CAN2 bus, so communication on the CAN2 bus is not possible.	B
CANH2	10	The device cannot drive a dominant signal on the CAN2 bus, so communication on the CAN2 bus is not possible.	B
V_{IO}	11	The device enters protected mode. The transceiver is passive on both the CAN1 and CAN2 buses.	B
CANL1	12	The device cannot drive a dominant signal on the CAN1 bus, so communication on the CAN1 bus is not possible.	B
CANH1	13	The device cannot drive a dominant signal on the CAN1 bus, so communication on the CAN1 bus is not possible.	B
STB1	14	The STB1 pin defaults high; the CAN1 transceiver is stuck in low-power mode.	B
Thermal Pad	-	None.	D

Table 4-9. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
TXD1	1	GND1	The CAN1 driver enters dominant timeout, disabling the driver. Data cannot be transmitted on the CAN1 bus.	B
GND1	2	V_{CC}	The CAN1 transceiver becomes unpowered, and high I_{CC} current flow is possible.	B
V_{CC}	3	RXD1	The output of the RXD1 pin becomes stuck high. The MCU is unable to receive data from the CAN1 bus using the RXD1 pin.	B
RXD1	4	GND2	By default, the RXD pin is high-side FET ON. With a pin short-circuit to ground, a direct path forms between supply and ground, causing high current flow.	A
GND2	5	TXD2	The CAN2 driver enters dominant timeout, disabling the driver. Data cannot be transmitted on the CAN2 bus.	B
TXD2	6	RXD2	The output on the RXD2 pin reflects the input to RXD2, and while this is the same transceiver, due to loop delay, the communication is potentially corrupted. Information from the CAN2 bus is potentially not received correctly.	B
STB2	8	CANL2	The CAN2 transceiver potentially turns off when the CAN2 bus is recessive. The device potentially does not enter or stay in the desired mode for the CAN2 bus.	B
CANL2	9	CANH2	The CAN2 bus becomes stuck recessive and no communication is possible. I_{OS} current is potentially reached when the CAN2 driver is transmitting.	B
CANH2	10	V_{IO}	The $V_{CANH(R)}$ specification is potentially violated depending on the V_{IO} level. The EMC performance of the CAN2 transceiver potentially degrades.	B
V_{IO}	11	CANL1	The $V_{CANH(R)}$ specification is potentially violated depending on the V_{IO} level. The EMC performance of the CAN2 transceiver potentially degrades.	B
CANL1	12	CANH1	The CAN1 bus becomes stuck recessive and no communication is possible. I_{OS}current is potentially reached when the CAN1 driver is transmitting.	B
CANH1	13	STB1	The CAN1 transceiver potentially turns off when a dominant signal is driven on the CAN1 bus. The device potentially does not enter or stay in the desired mode for the CAN1 bus.	B

Table 4-10. Pin FMA for Device Pins Short-Circuited to V_{CC}

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
TXD1	1	The TXD1 pin becomes stuck high. The device is unable to transmit data on the CAN1 bus.	B
GND1	2	The CAN1 transceiver becomes unpowered, and high I_{CC} is possible.	B
V_{CC}	3	None	D
RXD1	4	The RXD1 pin becomes stuck high. The MCU is unable to read data from the CAN1 bus using the RXD1 pin.	B
TXD2	5	The TXD2 pin becomes stuck high. The device is unable to transmit data on the CAN2 bus.	B
GND2	6	The CAN2 transceiver becomes underpowered, and high I_{CC} is possible.	B
RXD2	7	The RXD2 pin becomes stuck high. The MCU is unable to read data from the CAN2 bus using the RXD2 pin.	B
STB2	8	The STB2 pin is stuck high. The CAN2 transceiver becomes stuck in low-power mode.	B
CANL2	9	The device cannot drive a dominant signal to the CAN2 bus, so no communication is possible. The CAN2 bus potentially becomes stuck recessive during the fault.	B
CANH2	10	The $V_{CANL(R)}$ specification is violated. The EMC performance of the transceiver potentially degrades.	C
V_{IO}	11	The I/O pins operate as 5V inputs and outputs. The microcontroller is potentially damaged if $V_{CC} > V_{IO}$.	C
CANL1	12	The device cannot drive a dominant signal to the CAN1 bus, so no communication is possible. The CAN1 bus potentially becomes stuck recessive during the fault.	B
CANH1	13	The $V_{CANL(R)}$ specification is violated. The EMC performance of the transceiver potentially degrades.	C
STB1	14	The STB1 pin is stuck high. The CAN1 transceiver becomes stuck in low-power mode.	B

Table 4-11. Pin FMA for Device Pins Short-Circuited to V_{IO}

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
TXD1	1	The TXD1 pin becomes stuck high. The device is unable to transmit data on the CAN1 bus.	B
GND1	2	The CAN1 bus becomes unpowered, and high I_{CC} is possible.	B
V_{CC}	3	The I/O pins operate as 5V inputs and outputs. The microcontroller is potentially damaged if $V_{CC} > V_{IO}$.	C
RXD1	4	The RXD1 pin becomes stuck high. The MCU is unable to read data from the CAN1 bus using the RXD1 pin.	B
TXD2	5	The TXD2 pin becomes stuck high. The device is unable to transmit data on the CAN2 bus.	B
GND2	6	The CAN2 bus becomes unpowered, and high I_{IO} is possible.	B
RXD2	7	The RXD2 pin becomes stuck high. The MCU is unable to read data from the CAN2 bus using the RXD2 pin.	B
STB2	8	The STB2 pin is stuck high. The CAN2 channel becomes stuck in low-power mode.	B
CANL2	9	The device cannot generate a full dominant signal on the CAN2 bus. No communication is possible. I_{OS} current is potentially reached if $V_{IO} \geq 3.3V$.	B
CANH2	10	The $V_{CANL(R)}$ specification is violated if $V_{IO} \geq 3.3V$. The performance of the EMC potentially degrades.	C
V_{IO}	11	None	D
CANL1	12	The device cannot generate a full dominant signal on the CAN1 bus. No communication is possible. I_{OS} current is potentially reached if $V_{IO} \geq 3.3V$.	B
CANH1	13	The $V_{CANL(R)}$ specification is violated if $V_{IO} \geq 3.3V$. The performance of the EMC potentially degrades.	C
STB1	14	The STB1 pin is stuck high. The CAN1 channel becomes stuck in low-power mode.	B

Table 4-12. Pin FMA for Device Pins Short-Circuited to V_{BAT}

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
TXD1	1	An absolute maximum violation occurs. The device is potentially damaged. The device potentially cannot transmit data on the CAN1 bus.	A
GND1	2	The device becomes unpowered. High I_{BAT} current is possible.	B
V_{CC}	3	An absolute maximum violation occurs. The device is potentially damaged. The CAN bus potentially cannot communicate.	A
RXD1	4	An absolute maximum violation occurs. The device is potentially damaged. The MCU potentially cannot receive data from the CAN1 bus.	A
TXD2	5	An absolute maximum violation occurs. The device is potentially damaged. The device potentially cannot transmit data on the CAN2 bus.	A
GND2	6	The device becomes unpowered. High I_{BAT} current is possible.	B
RXD2	7	An absolute maximum violation occurs. The device is potentially damaged. The MCU potentially cannot receive data from the CAN2 bus.	A
STB2	8	An absolute maximum violation occurs. The device is potentially damaged. The CAN2 transceiver becomes stuck in low-power mode.	A
CANL2	9	The CAN2 bus becomes stuck recessive. No communication is possible. I_{OS} current is potentially reached.	B
CANH2	10	The $V_{CANL(R)}$ specification is violated. The EMC performance of the transceiver potentially degrades.	C
V_{IO}	11	An absolute maximum violation occurs. The device is potentially damaged.	A
CANL1	12	The CAN2 bus becomes stuck recessive. No communication is possible. I_{OS} current is potentially reached.	B
CANH1	13	The $V_{CANL(R)}$ specification is violated. The EMC performance of the transceiver potentially degrades.	C
STB1	14	An absolute maximum violation occurs. The device is potentially damaged. The CAN1 transceiver becomes stuck in low-power mode.	A

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2025	*	Initial Release

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