Functional Safety Information

UCC33011(Q1), UCC33021(Q1) UCC33411(Q1), and UCC33421(Q1) Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for the UCC33011(Q1), UCC33021(Q1), UCC33411(Q1), and UCC33421(Q1) (SSOP-16 package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

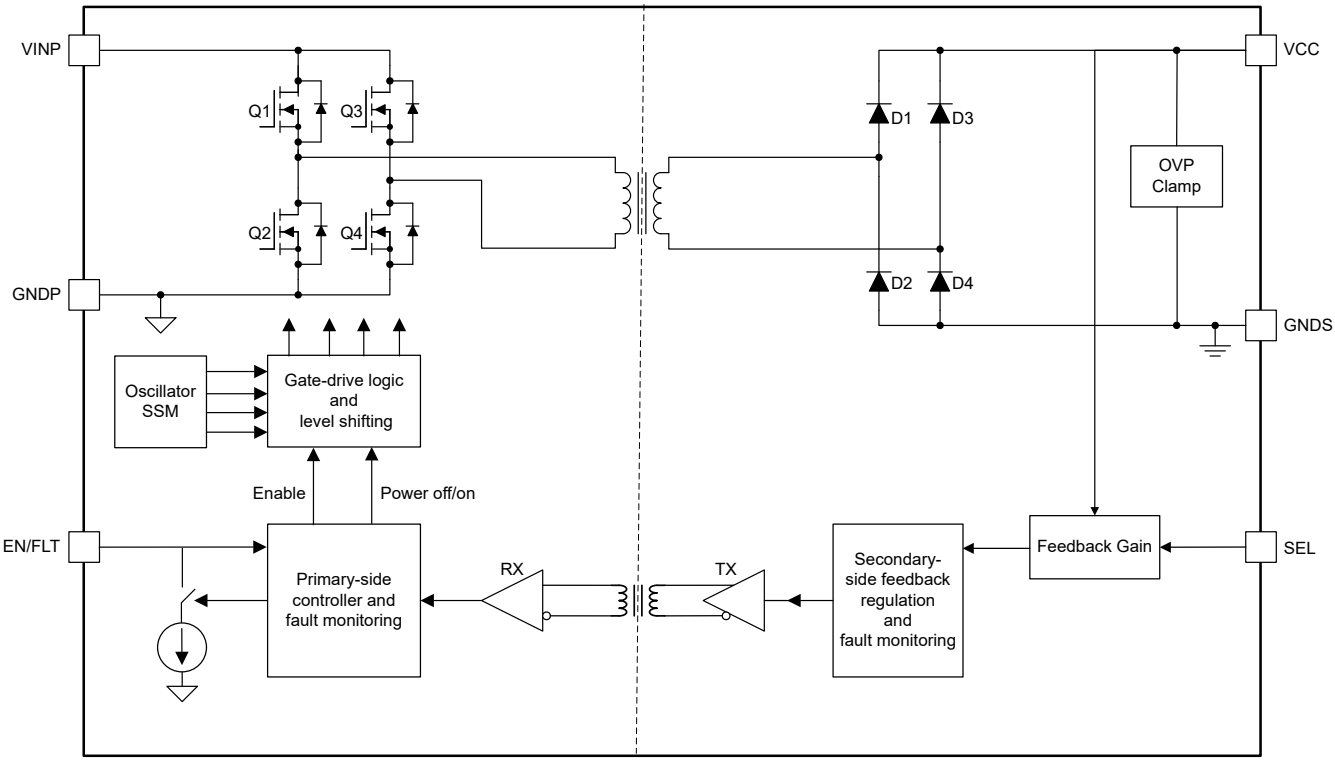

Figure 1-1. Functional Block Diagram

The UCC33011(Q1), UCC33021(Q1), UCC33411(Q1), and UCC33421(Q1) were developed using a quality-managed development process, but were not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 SSOP-16 Package

This section provides functional safety failure in time (FIT) rates for the SSOP-16 package of UCC33011(Q1), UCC33021(Q1), UCC33411(Q1), and UCC33421(Q1) based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	Power Dissipation	FIT (Failures Per 10^9 Hours)
Total component FIT rate	0.5W	21
	1W	27
	1.23W	29
Die FIT rate	0.5W	4
	1W	8
	1.23W	10
Package FIT rate	0.5W	17
	1W	19
	1.23W	19

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 0.5W, 1W, and 1.23W
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	60 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the UCC33011(Q1), UCC33021(Q1), UCC33411(Q1), and UCC33421(Q1) in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
VCC has no power	38
VCC accuracy and ripple do not meet specifications	30
FAULT reporting does not work	14
No effect	18

The FMD in the *Die Failure Modes and Distribution* table excludes short-circuit faults across the isolation barrier. Faults for short circuits across the isolation barrier can be excluded according to IEC 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a safety-separated extra low voltage (SELV) or protective extra low voltage (PELV) power supply is used, pollution degree 2 / OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the UCC33011(Q1), UCC33021(Q1), UCC33411(Q1), and UCC33421(Q1) (SSOP-16 package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The device is configured according to the *Typical Application* in the *Application and Implementation* section of the data sheet.
- The VINP pin is considered the supply pin for primary-side pins.
- The GNDP pin is considered the ground for primary-side pins.
- The VCC pin is considered the supply pin for secondary-side pins.
- The GNDS pin is considered the ground for secondary-side pins.
- The primary-side pins only short to the primary-side pins. The secondary side-pins only short to the secondary-side pins.

4.1 SSOP-16 Package

Figure 4-1 shows the UCC33011(Q1), UCC33021(Q1), UCC33411(Q1), and UCC33421(Q1) pin diagram for the SSOP-16 package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the UCC33011(Q1), UCC33021(Q1), UCC33411(Q1), and UCC33421(Q1) data sheets.

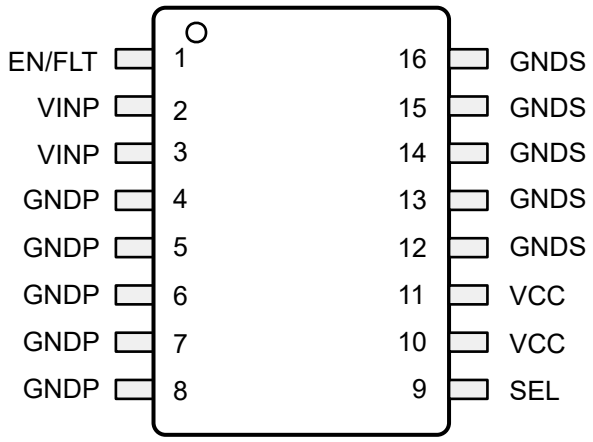

Figure 4-1. Pin Diagram (SSOP-16 Package)

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
EN/FLT	1	The device is disabled. No output.	B
VINP	2	The device has no input. No output.	B
VINP	3	The device has no input. No output.	B
GNDP	4	No effect. Normal operation.	D
GNDP	5	No effect. Normal operation.	D
GNDP	6	No effect. Normal operation.	D
GNDP	7	No effect. Normal operation.	D
GNDP	8	No effect. Normal operation.	D
SEL	9	The output is set to 5.5V.	C
VCC	10	The output is shorted. No output.	B
VCC	11	The output is shorted. No output.	B
GNDS	12	No effect. Normal operation.	D
GNDS	13	No effect. Normal operation.	D
GNDS	14	No effect. Normal operation.	D
GNDS	15	No effect. Normal operation.	D
GNDS	16	No effect. Normal operation.	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
EN/FLT	1	The EN/FLT pin is at an undetermined state. The output can be random.	B
VINP	2	The device operates normally with degradation on thermal performance.	C
VINP	3	The device operates normally with degradation on thermal performance.	C
GNDP	4	The device operates normally with degradation on thermal performance.	C
GNDP	5	The device operates normally with degradation on thermal performance.	C
GNDP	6	The device operates normally with degradation on thermal performance.	C
GNDP	7	The device operates normally with degradation on thermal performance.	C
GNDP	8	The device operates normally with degradation on thermal performance.	C
SEL	9	The SEL pin is at an undetermined state. The output voltage can change between 5V and 5.5V randomly.	C
VCC	10	The device operates normally with degradation on thermal performance.	C
VCC	11	The device operates normally with degradation on thermal performance.	C
GNDS	12	The device operates normally with degradation on thermal performance.	C
GNDS	13	The device operates normally with degradation on thermal performance.	C
GNDS	14	The device operates normally with degradation on thermal performance.	C
GNDS	15	The device operates normally with degradation on thermal performance.	C
GNDS	16	The device operates normally with degradation on thermal performance.	C

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
EN/FLT	1	VINP	The device is always enabled and cannot be turned off.	C
VINP	2	VINP	No effect. Normal operation.	D
VINP	3	GNDP	The device has no input. No output.	B
GNDP	4	GNDP	No effect. Normal operation.	D
GNDP	5	GNDP	No effect. Normal operation.	D

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
GNDP	6	GNDP	No effect. Normal operation	D
GNDP	7	GNDP	No effect. Normal operation.	D
GNDP	8	N/A	Not considered. Corner pin.	D
SEL	9	VCC	The output is set to 5V only.	C
VCC	10	VCC	No effect. Normal operation.	D
VCC	11	GNDS	The output is shorted. No output.	B
GNDS	12	GNDS	No effect. Normal operation.	D
GNDS	13	GNDS	No effect. Normal operation.	D
GNDS	14	GNDS	No effect. Normal operation.	D
GNDS	15	GNDS	No effect. Normal operation.	D
GNDS	16	N/A	Not considered. Corner pin.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
EN/FLT	1	The device is always enabled and cannot be turned off.	C
VINP	2	No effect. Normal operation.	D
VINP	3	No effect. Normal operation.	D
GNDP	4	The device has no input. No output.	B
GNDP	5	The device has no input. No output.	B
GNDP	6	The device has no input. No output.	B
GNDP	7	The device has no input. No output.	B
GNDP	8	The device has no input. No output.	B
SEL	9	The output is set to 5V only.	C
VCC	10	No effect. Normal operation.	D
VCC	11	No effect. Normal operation.	D
GNDS	12	The output is shorted. No output.	B
GNDS	13	The output is shorted. No output.	B
GNDS	14	The output is shorted. No output.	B
GNDS	15	The output is shorted. No output.	B
GNDS	16	The output is shorted. No output.	B

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2025	*	Initial Release

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