Functional Safety Information

UCC25661x-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for the UCC25661x-Q1 (16-pin SOIC package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

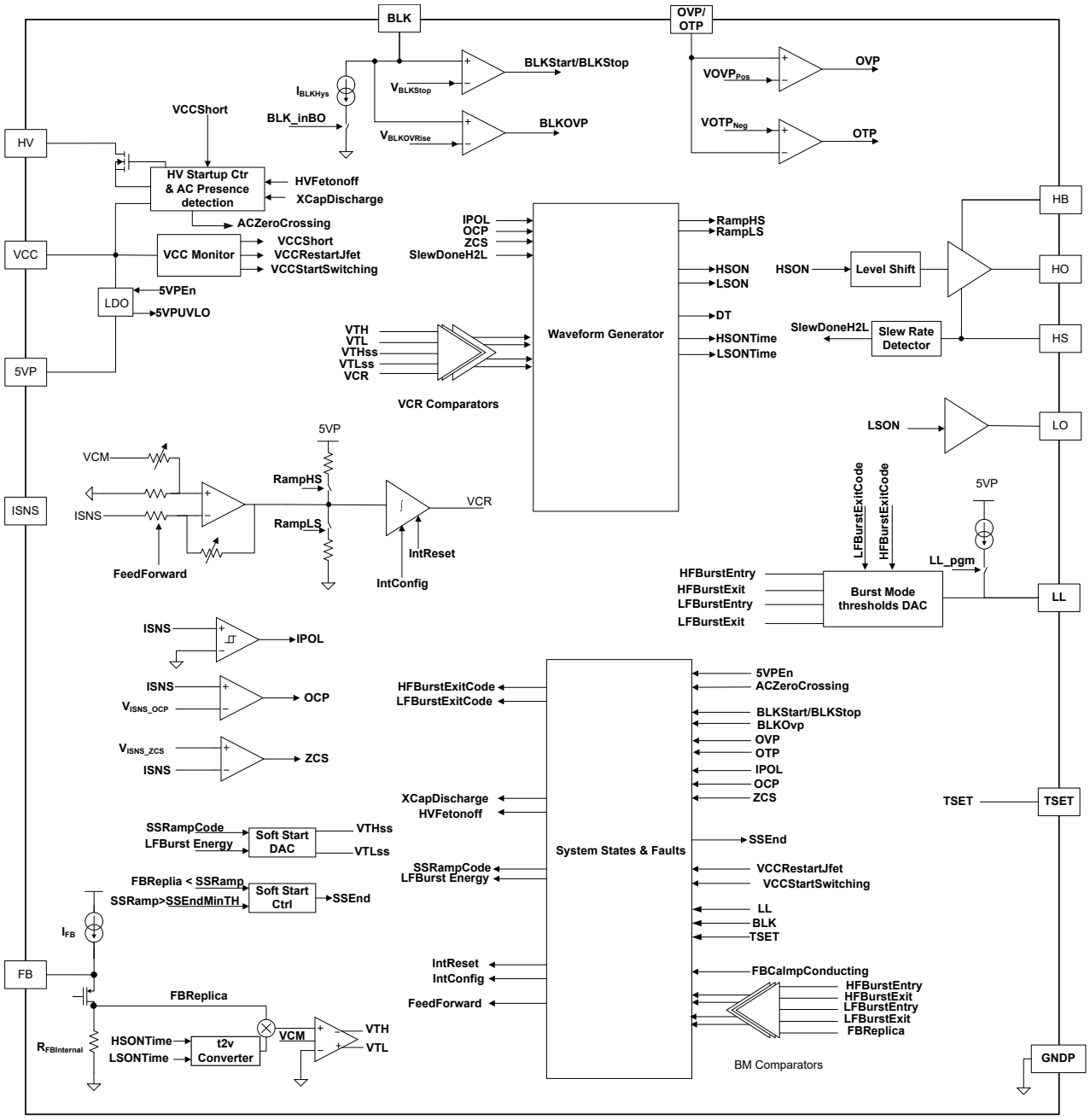

Figure 1-1. Functional Block Diagram

The UCC25661x-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the UCC25661x-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	Power Dissipation (mW)	FIT (Failures Per 10^9 Hours)
Total component FIT rate	100	18
	200	19
	300	21
Die FIT rate	100	3
	200	4
	300	5
Package FIT rate	100	15
	200	15
	300	16

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 100mW, 200m, and 300mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	60 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the UCC25661x-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Vout Regulation Issue	29
Degraded System Efficiency	20
Gate Driver Failure	16
Fault Detection Issue	7
Compromised HV Capability	2
No Effect	26

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the UCC25661x-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to VCC (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the UCC25661x-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the UCC25661x-Q1 data sheet.

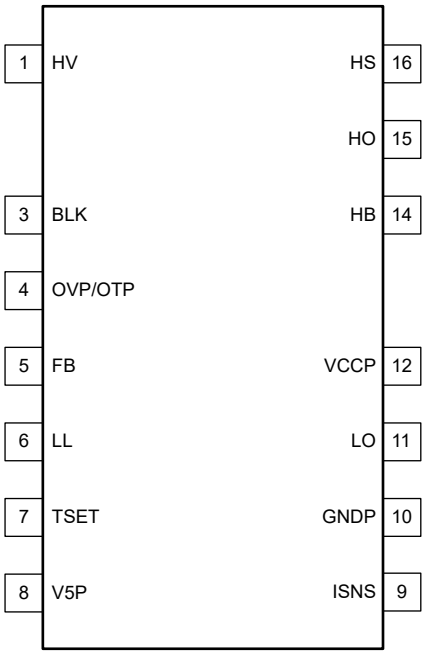

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The analysis is based on the typical application schematic in the UCC25661x-Q1 data sheet.
- VCCP is considered as the supply pin.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
HV	1	The device is not biased. No output.	B
N/A	2	N/A	N/A
BLK	3	No output.	B
OVP/OTP	4	The system tries to restart. No output.	B
FB	5	The system tries to restart. No output.	B
LL	6	The burst-mode function is disabled.	C
TSET	7	The system does not start up.	B
V5P	8	The system does not start up.	B
ISNS	9	Protection triggers. No output.	B
GNDP	10	No effect.	D
LO	11	The system does not start up.	B
VCCP	12	The device is not biased. No output.	B
N/A	13	N/A	N/A
HB	14	The device is not biased. No output.	B
HO	15	Protection triggers. No output.	B
HS	16	Half-bridge shoot through; power stage is damaged. No output.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
HV	1	The device is not biased. No output.	B
N/A	2	N/A	N/A
BLK	3	No output.	B
OVP/OTP	4	OVP/OTP loses protections.	C
FB	5	Protection triggers. No output.	B
LL	6	The burst-mode function is lost.	C
TSET	7	The system does not start up. No output.	B
V5P	8	The output is not regulated.	B
ISNS	9	The system does not start up.	B
GNDP	10	The output is not regulated.	B
LO	11	No output.	B
VCCP	12	No output.	B
N/A	13	N/A	N/A
HB	14	No output.	B
HO	15	The output is not regulated.	B
HS	16	Power stage is damaged. No output.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
HV	1	N/A	N/A	D
N/A	2	BLK	N/A	D
BLK	3	OVP/OTP	The output is not regulated.	B
OVP/OTP	4	FB	The output is not regulated.	B
FB	5	LL	The output is not regulated.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
LL	6	TSET	The output is not regulated.	B
TSET	7	V5P	The system does not start up.	B
V5P	8	ISNS	N/A	D
ISNS	9	GNDP	Protection triggers. No output.	B
GNDP	10	LO	No output.	B
LO	11	VCCP	No output.	B
VCCP	12	N/A	N/A	D
N/A	13	HB	N/A	D
HB	14	HO	The power stage and device are damaged.	A
HO	15	HS	No output.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to VCC

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
HV	1	The system is in normal operation after the HV series resistor is burned.	C
N/A	2	N/A	D
BLK	3	The output is not regulated.	B
OVP/OTP	4	The output is not regulated.	B
FB	5	The output is not regulated.	B
LL	6	The output is not regulated.	B
TSET	7	The output is not regulated.	B
V5P	8	The output is not regulated.	B
ISNS	9	The device is not biased. No output.	B
GNDP	10	The device is not biased. No output.	B
LO	11	No output.	B
VCCP	12	No impact.	D
N/A	13	N/A	D
HB	14	The device and system are damaged.	A
HO	15	The device and system are damaged.	A
HS	16	The output is not regulated.	B

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
July 2025	*	Initial Release

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