Functional Safety Information

TPSI3050M
Functional Safety FIT Rate, FMD, and Pin FMA

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Trademarks

1 Overview

This document contains information for TPSI3050M (SOIC package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

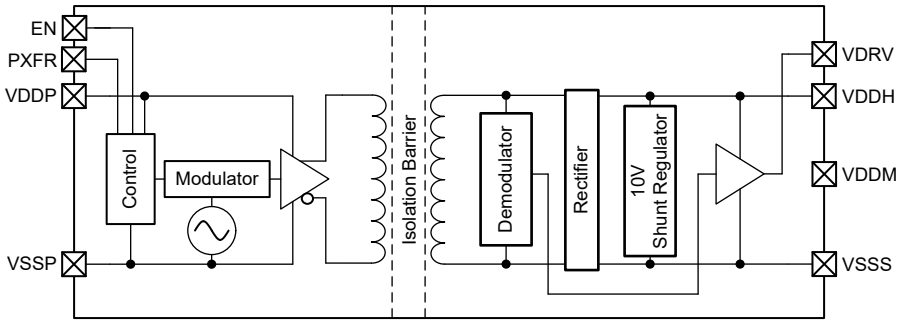

Figure 1-1. Functional Block Diagram

TPSI3050M was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for TPSI3050M based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	19
Die FIT rate	4
Package FIT rate	15

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 250mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS ASICs analog and mixed = <50V supply	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution for TPSI3050M in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
VDDH/VDDM rails fail to power up. VDRV remains low.	15
VDRV does not respond to EN signaling.	20
Output power not meeting specification. Longer VDDH/VDDM start-up and recovery times.	25
VDDH not regulated, potential device damage.	15
VDRV propagation times longer than specified.	5
VDRV only stays high for few microseconds due to improper loading of configuration.	5
Higher EMI	5
Unpredictable power down sequence.	5
VDRV output held high.	5

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPSI3050M. The failure modes covered in this document include the typical pin-by-pin failure scenarios for three-wire mode and two-wire mode:

- Pin short-circuited to VSSP or VSSS (see Table 4-2 and Table 4-6)
- Pin open-circuited (see Table 4-3 and Table 4-7)
- Pin short-circuited to an adjacent pin (see Table 4-4 and Table 4-8)
- Pin short-circuited to VDDP (see Table 4-5 and Table 4-9)

Table 4-2 through Table 4-9 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the TPSI3050M pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TPSI3050M data sheet.

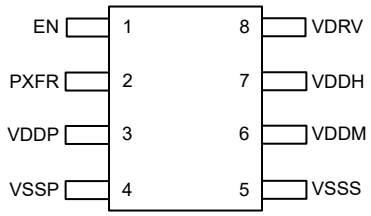

Figure 4-1. Pin Diagram

The TPSI3050M is normally operated in one of two modes of operation for a given application: three-wire mode or two-wire mode. The pin FMA was performed individually for each of these modes of operation in the following sections.

Three-Wire Mode

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Device configured and operating in three-wire mode
- Device in normal operation prior to any open or short condition being applied to the respective pin
- EN set to a static logic low or high (VDRV asserted low or high respectively)
- Opens or shorts occur relative to primary and secondary sides of the device and is a static event

Table 4-2. Three-Wire Mode: Pin FMA for Device Pins Short-Circuited to VSSP or VSSS

Pin Name	Pin No.	Ground	Description of Potential Failure Effects	Failure Effect Class
EN	1	VSSP	VDRV asserts low.	B
PXFR	2	VSSP	Subsequent power cycles result in R_{PXFR} selection to 7.32kΩ, which can result in longer start-up and recovery times if a different R_{PXFR} selection from 7.32kΩ is used in the application.	C
VDDP	3	VSSP	No power transfer. VDDH and VDDM rails collapse. VDRV asserts low with active clamp enabled. If EN static is high, additional leakage current into the EN pin is observed on the order of 25mA.	B
VDRV	8	VSSS	If VDRV is high, VDDH and VDDM rails collapse. VDRV asserts low with an active clamp enabled. If VDRV is low, no effect.	B
VDDH	7	VSSS	VDDH and VDDM rails collapse. VDRV asserts low with an active clamp enabled.	B

Table 4-2. Three-Wire Mode: Pin FMA for Device Pins Short-Circuited to VSSP or VSSS (continued)

Pin Name	Pin No.	Ground	Description of Potential Failure Effects	Failure Effect Class
VDDM	6	VSSS	VDDH and VDDM rails collapse. VDRV asserts low with an active clamp enabled.	B

Table 4-3. Three-Wire Mode: Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
EN	1	VDRV asserts low. The EN pin has an internal resistive pulldown to VSSP.	B
PXFR	2	Subsequent power cycles result in R_{PXFR} selection to 7.32kΩ, which can result in longer start-up and recovery times if a different R_{PXFR} selection from 7.32kΩ is used in the application.	C
VDDP	3	No power transfer. VDDH and VDDM rails collapse. VDRV asserts low with an active clamp enabled.	B
VSSP	4	No power transfer. VDDH and VDDM rails collapse. VDRV asserts low with an active clamp enabled.	B
VDRV	8	No drive to the external switch. The external switch gate control can float dependent upon application circuitry.	B
VDDH	7	VDDH can collapse under loading or switching events.	B
VDDM	6	VDDH and VDDM can collapse under loading or switching events.	B
VSSS	5	Normal power transfer. VDDH and VDDM rails remain charged. VDRV follows the state of EN logic level. Since VSSS is a floating ground, VSSS cannot drive the external switch.	B

Table 4-4. Three-Wire Mode: Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
VDDH	7	VDDM	VDDH and VDDM rails collapse. VDRV asserts low with an active clamp enabled.	B
VDRV	8	VDDH	If VDRV is low, VDDH and VDDM rails collapse. VDRV remains low with an active clamp enabled. If VDRV is high, no effect.	B
EN	1	PXFR	Subsequent power cycles result in R_{PXFR} selection to 7.32kΩ, which can result in longer start-up and recovery times if a different R_{PXFR} selection from 7.32kΩ is used in the application.	C

Table 4-5. Three-Wire Mode: Pin FMA for Device Pins Short-Circuited to VDDP

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
EN	1	VDRV asserts high.	B
PXFR	2	Subsequent power cycles result in R_{PXFR} selection to 7.32kΩ, which can result in longer start-up and recovery times if a different R_{PXFR} selection from 7.32kΩ is used in the application.	C

Two-Wire Mode

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Device configured and operating in two-wire mode
- Device in normal operation prior to any open or short condition being applied to the respective pin
- EN set to a static high (VDRV asserted high)
- Opens or shorts occur relative to primary and secondary sides of the device and is a static event

Table 4-6. Two-Wire Mode: Pin FMA for Device Pins Short-Circuited to VSSP or VSSS

Pin Name	Pin No.	Ground	Description of Potential Failure Effects	Failure Effect Class
EN	1	VSSP	No power transfer. VDDH and VDDM rails collapse. VDRV asserts low with an active clamp enabled.	B
PXFR	2	VSSP	Subsequent power cycles result in R_{PXFR} selection to 7.32kΩ, which can result in longer start-up and recovery times if a different R_{PXFR} selection from 7.32kΩ is used in the application.	C
VDDP	3	VSSP	No power transfer. VDDH and VDDM rails collapse. VDRV asserts low with an active clamp enabled. Additional leakage current into the EN pin is observed on the order of 25mA.	B
VDRV	8	VSSS	VDDH and VDDM rails collapse. VDRV asserts low with an active clamp enabled.	B
VDDH	7	VSSS	VDDH and VDDM rails collapse. VDRV asserts low with an active clamp enabled.	B
VDDM	6	VSSS	VDDH and VDDM rails collapse. VDRV asserts low with an active clamp enabled.	B

Table 4-7. Two-Wire Mode: Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
EN	1	No power transfer. VDDH and VDDM rails collapse. VDRV asserts low with an active clamp enabled. The EN pin has an internal resistive pulldown to VSSP.	B
PXFR	2	Subsequent power cycles result in R_{PXFR} selection to 7.32kΩ, which can result in longer start-up and recovery times if a different R_{PXFR} selection from 7.32kΩ is used in the application.	C
VDDP	3	No power transfer. VDDH and VDDM rails collapse. VDRV asserts low with an active clamp enabled.	B
VSSP	4	No power transfer. VDDH and VDDM rails collapse. VDRV asserts low with an active clamp enabled.	B
VDRV	8	No drive to the external switch. The external switch gate control can float dependent upon application circuitry.	B
VDDH	7	VDDH can collapse under loading or switching events.	B
VDDM	6	VDDH and VDDM can collapse under loading or switching events.	B
VSSS	5	Normal power transfer. VDDH and VDDM rails remain charged. VDRV follows the state of EN logic level. Since VSSS is a floating ground, VSSS cannot drive the external switch.	B

Table 4-8. Two-Wire Mode: Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
VDDH	7	VDDM	VDDH and VDDM rails collapse. VDRV asserts low with an active clamp enabled.	B
VDRV	8	VDDH	VDRV remains high.	B
EN	1	PXFR	Subsequent power cycles result in R_{PXFR} selection to 7.32kΩ, which can result in longer start-up and recovery times if a different R_{PXFR} selection from 7.32kΩ is used in the application.	C

Table 4-9. Two-Wire Mode: Pin FMA for Device Pins Short-Circuited to VDDP

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
EN	1	If EN voltage exceeds the absolute maximum of VDDP, potential damage of device can occur.	A
PXFR	2	Subsequent power cycles result in R_{PXFR} selection to 7.32kΩ, which can result in longer start-up and recovery times if a different R_{PXFR} selection from 7.32kΩ is used in the application.	C

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
March 2025	*	Initial Release

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