Functional Safety Information

LM5125-Q1, LM5125A-Q1, and LM51251A-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for LM5125-Q1, LM5125A-Q1, and LM51251A-Q1 (VQFN package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1, Figure 1-2, and Figure 1-3 show the device functional block diagrams for reference.

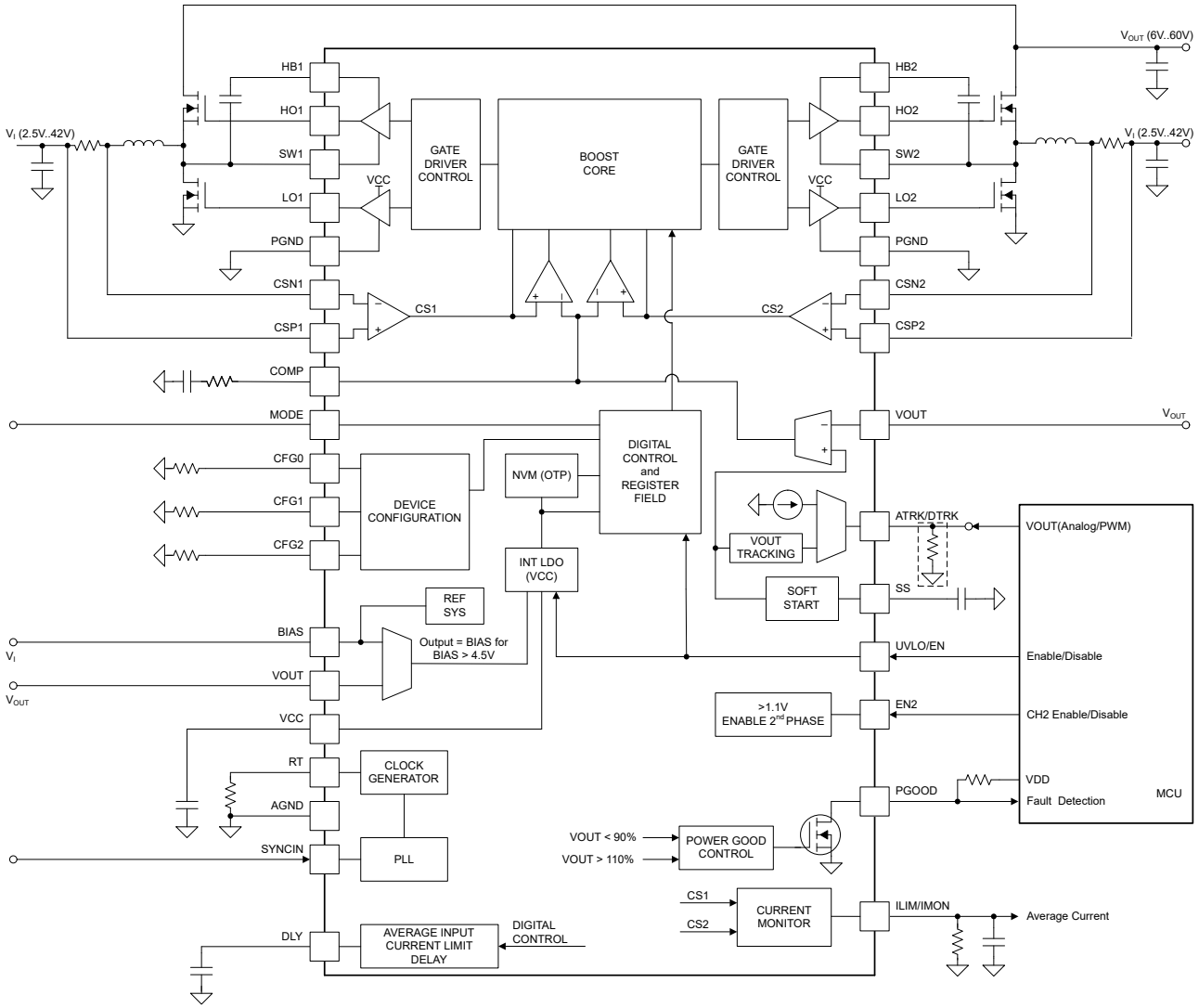

Figure 1-1. LM5125-Q1 Functional Block Diagram

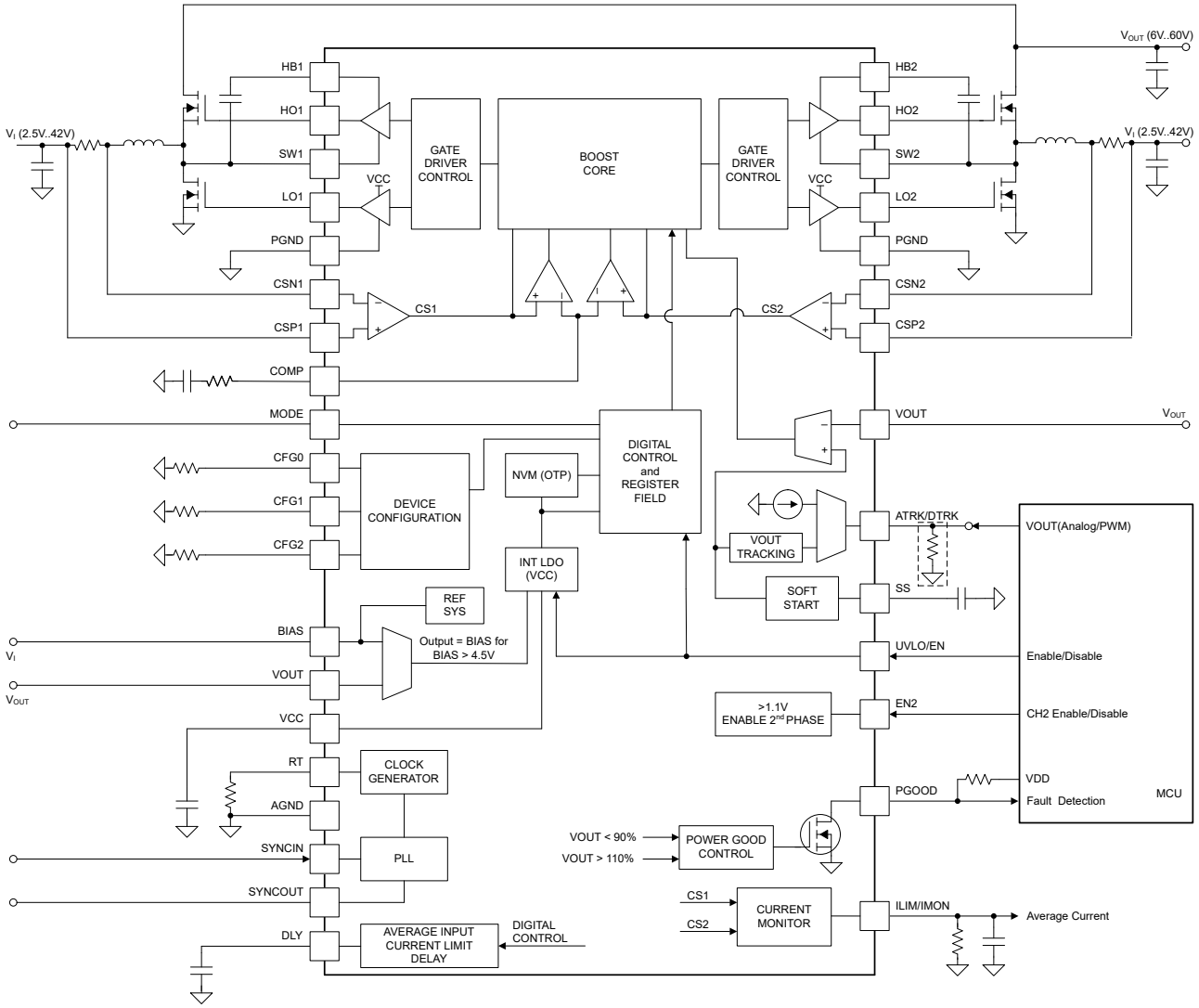

Figure 1-2. LM5125A-Q1 Functional Block Diagram

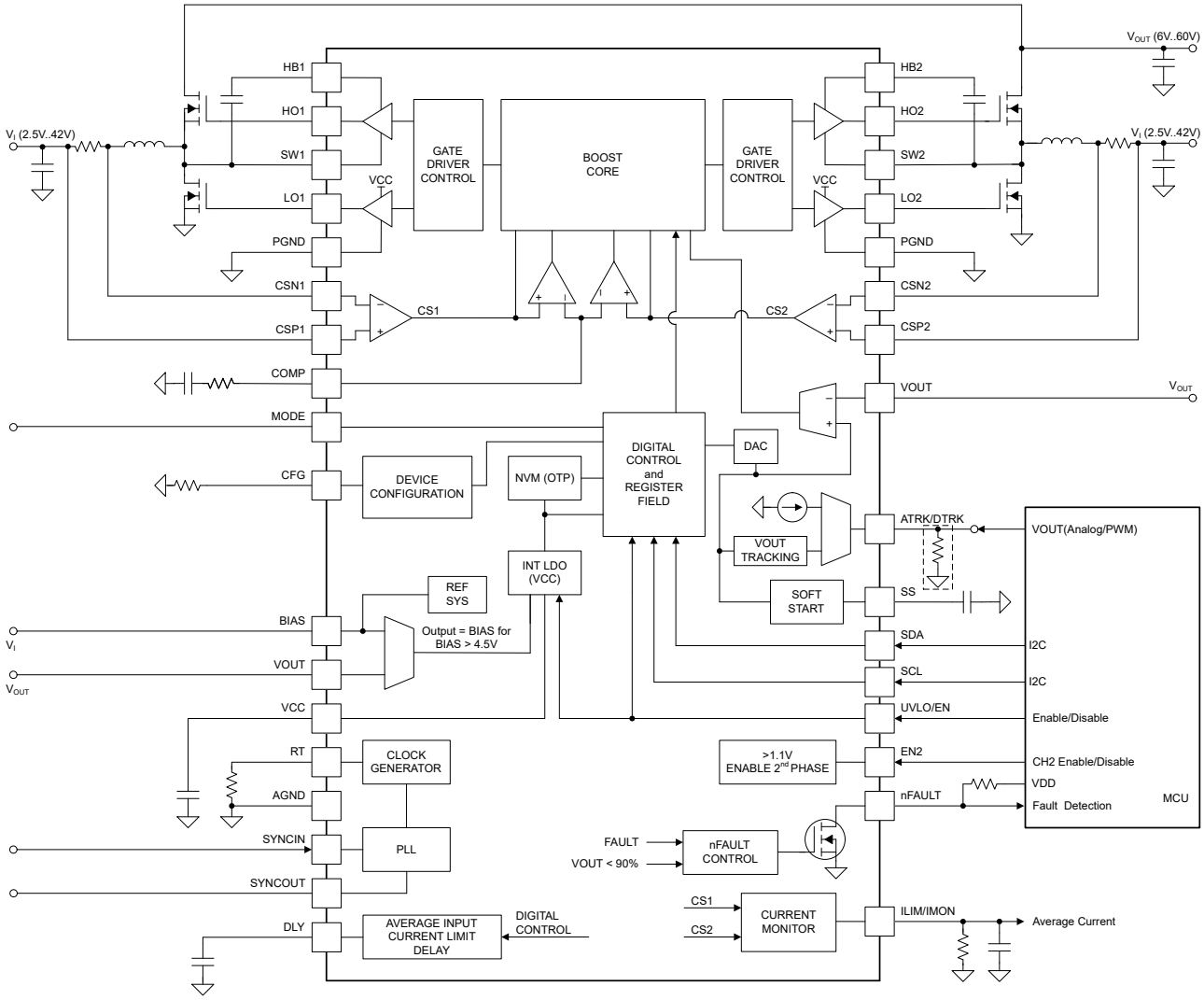

Figure 1-3. LM51251A-Q1 Functional Block Diagram

The LM5125-Q1, LM5125A-Q1, and LM51251A-Q1 devices were developed using a quality-managed development process, but were not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 VQFN Package

This section provides functional safety failure in time (FIT) rates for the VQFN package of LM5125-Q1, LM5125A-Q1, and LM51251A-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	25
Die FIT rate	7
Package FIT rate	18

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 1000mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS ASICs analog and mixed HV >50V supply	N/A	75°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for LM5125-Q1, LM5125A-Q1, and LM51251A-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
HO1 or HO2 (or both) gate drivers are stuck on	5
LO1 or LO2 (or both) gate drivers are stuck on	
HO1 or HO2 (or both) gate drivers are stuck off	15
LO1 or LO2 (or both) gate drivers are stuck off	
HO1 or HO2 (or both) gate drivers are Hi-Z	5
LO1 or LO2 (or both) gate drivers are Hi-Z	
VCC LDO output voltage is out of specification	15
V_{OUT} voltage is out of specification	40
PGOOD/nFAULT false or fails to trip	10
Digital control malfunctions, or electrical parameters are out of specification	10

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of LM5125-Q1, LM5125A-Q1, and LM51251A-Q1 (VQFN package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2, Table 4-6, and Table 4-10)
- Pin open-circuited (see Table 4-3, Table 4-7, and Table 4-11)
- Pin short-circuited to an adjacent pin (see Table 4-4, Table 4-8, and Table 4-12)
- Pin short-circuited to V_I (see Table 4-5, Table 4-9, and Table 4-13)

Table 4-2 through Table 4-13 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The device is used within the *Recommended Operation Conditions* and the *Absolute Maximum Ratings* found in the LM5125-Q1, LM5125A-Q1, and LM51251A-Q1 data sheets.
- For the analysis, the typical application is used as shown in the *Typical Application* section of the LM5125-Q1, LM5125A-Q1, and LM51251A-Q1 data sheets.
- V_{SUPPLY} = 12V
- V_{OUT} = 24V

4.1 LM5125-Q1 (VQFN) Package

Figure 4-1 shows the pin diagram for the LM5125-Q1 device. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the LM5125-Q1 data sheet.

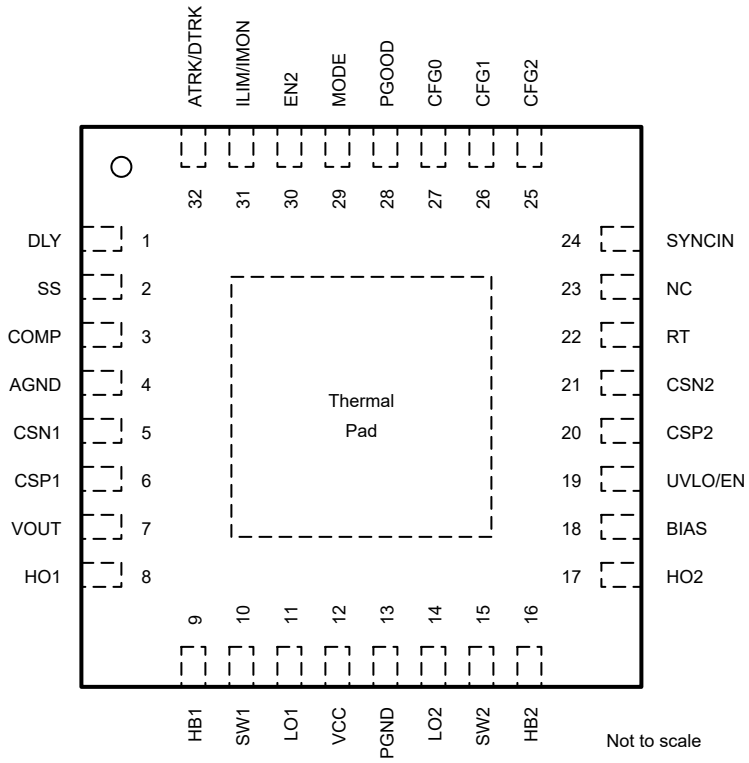

Figure 4-1. Pin Diagram (VQFN) Package

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
DLY	1	The average-input-current loop is not activated when the average-input-current loop feature is used.	B
			D
SS	2	The device does not start; no switching.	B
COMP	3	V_{OUT} is out of regulation; not switching.	B
AGND	4	No effect.	D
CSN1	5	The device is potentially damaged if the differential voltage exceeds the absolute maximum rating of 0.3V.	A
CSP1	6	The device is potentially damaged if the differential voltage exceeds the absolute maximum rating of 0.3V.	A
VOUT	7	The external components are potentially damaged. The device potentially goes into a latch state or does not start.	B
HO1	8	The phase-1 high-side driver is potentially damaged when the device starts switching.	A
HB1	9	The device is potentially damaged when BOOT charging starts.	A
SW1	10	No energy is transferred from the input to the output.	B
LO1	11	The phase-1 low-side driver is potentially damaged when the device starts switching.	A
VCC	12	There is a loss of VCC regulation; no switching.	B
PGND	13	No effect.	D
LO2	14	The phase-1 low-side driver is potentially damaged when the device starts switching.	A
SW2	15	No energy is transferred from the input to the output.	B
HB2	16	The device is potentially damaged when BOOT charging starts.	A
HO2	17	The phase-2 high-side driver is potentially damaged when the device starts switching.	A
BIAS	18	The device is not powered, and therefore, not functional.	B
UVLO/EN	19	The device is disabled.	B
CSP2	20	The device is potentially damaged if the differential voltage exceeds the absolute maximum rating of 0.3V.	A
CSN2	21	The device is potentially damaged if the differential voltage exceeds the absolute maximum rating of 0.3V.	A
RT	22	The device goes to the maximum switching frequency of >2.2MHz.	C
NC	23	No connection.	D
SYNCIN	24	Clock synchronization is disabled; the device uses the internal clock.	C
CFG2	25	Level 1 of the CFG2 pin is forced.	C
CFG1	26	Level 1 of the CFG1 pin is forced.	C
CFG0	27	Level 1 of the CFG0 pin is forced.	C
PGOOD	28	The voltage of the output is correct, but there is a loss of functionality at the PGOOD pin.	B
MODE	29	Diode emulation mode is activated. There is no effect if the device is configured for diode emulation mode (MODE = GND).	C
			D
EN2	30	Second phase is disabled if second phase is used.	C
			D
ILIM/IMON	31	The average-input-current loop is not activated; current monitoring does not work.	B
ATRK/DTRK	32	There is no output voltage regulation. The device enters BYPASS mode after the soft start completes.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
DLY	1	Delayed programming does not work if the delay pin function is used.	B
			D

Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
SS	2	There is a short soft-start time.	C
COMP	3	The device is potentially unstable.	B
AGND	4	Device damage is possible.	A
CSN1	5	There is a loss of the current sense signal for phase 1. Peak-current limit does not work.	B
CSP1	6	There is a loss of the current sense signal for phase 1. Peak-current limit does not work.	B
VOUT	7	The internal feedback voltage for the regulation loop is pulled to GND; V_{OUT} reaches OVP_{max}.	B
HO1	8	There is a loss of the high-side driver.	B
HB1	9	There is a loss of boot voltage, and hence, a loss of the high-side driver.	B
SW1	10	There is a loss of the high-side driver.	B
LO1	11	The low-side MOSFET does not switch for phase 1.	B
VCC	12	The VCC pin is not stable enough to sustain normal operation.	B
PGND	13	Device damage is possible.	A
LO2	14	The low-side MOSFET does not switch for phase 2.	B
SW2	15	There is a loss of the high-side driver.	B
HB2	16	There is a loss of boot voltage, and hence, a loss of the high-side driver.	B
HO2	17	There is a loss of the high-side driver.	B
BIAS	18	The device is not powered, and therefore, not functional.	B
UVLO/EN	19	The device is disabled.	B
CSP2	20	There is a loss of the current sense signal for phase 2. Peak-current limit does not work.	B
CSN2	21	There is a loss of the current sense signal for phase 2. Peak-current limit does not work.	B
RT	22	The minimum frequency is set.	C
NC	23	No connection.	D
SYNCIN	24	Clock synchronization does not work; the device uses the internal clock.	C
CFG2	25	Level 16 of the CFG2 pin is forced.	C
CFG1	26	Level 16 of the CFG1 pin is forced.	C
CFG0	27	Level 16 of the CFG0 pin is forced.	C
PGOOD	28	The output voltage is correct, but there is a loss of functionality at the PGOOD pin.	B
MODE	29	There is no effect if DEM mode is active, otherwise, DEM mode is activated.	D C
EN2	30	Second-phase enable potentially does not function as intended.	C
ILIM/IMON	31	The device operates in an average-input-current limit loop operation; V_{OUT} drops, and therefore, V_{OUT} is out of regulation.	B
ATRK/DTRK	32	The device goes to OVP_{max}.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
DLY	1	SS	There is a loss of the delay function; the average-input-current loop does not function as intended.	B
SS	2	COMP	The device operates in peak-current limit and the output voltage rises to OVP_{max}.	B
COMP	3	AGND	The V_{OUT} regulation loop does not function, the internal supply potentially collapses.	B
AGND	4	CSN1	The device is potentially damaged if the differential voltage exceeds the absolute maximum rating of 0.3V.	A
CSN1	5	CSP1	There is a loss of current sense information. The circuit is potentially unstable.	B
CSP1	6	VOUT	The output is shorted to the input supply. There is no output regulation.	B
VOUT	7	HO1	Device damage is possible as the HO1 pin exceeds the absolute maximum voltage rating to switch.	A
HO1	8	HB1	Device damage is possible when switching starts.	A
HB1	9	SW1	There is a loss of the high-side driver.	B
SW1	10	LO1	Device damage is possible as the absolute maximum rating is exceeded at the LO1 pin.	A
LO1	11	VCC	The LO1 pin does not switch. Device damage is possible when switching starts.	A
VCC	12	PGND	There is no VCC rail; no switching.	B
PGND	13	LO2	Device damaged is possible when switching starts.	A
LO2	14	SW2	Device damage is possible as the absolute maximum rating is exceeded at the LO2 pin.	A
SW2	15	HB2	There is a loss of the high-side driver.	B
HB2	16	HO2	Device damage is possible when switching starts.	A
HO2	17	BIAS	Device damage is possible as the HO2 pin potentially exceeds the absolute maximum voltage ratings at the pin locations of HO2 to SW2.	A
BIAS	18	UVLO/EN	There is a loss of the UVLO function; the device is always enabled.	B C
UVLO/EN	19	CSP2	There is incorrect current sense information, the current limit is potentially incorrect.	B
CSP2	20	CSN2	There is a loss of current sense information. The circuit is potentially unstable.	B
CSN2	21	RT	Device damage is possible. The CSN2 pin exceeds the absolute maximum voltage rating for the RT pin.	A
RT	22	NC	The device potentially operates at the wrong switching frequency.	C
NC	23	SYNCIN	The device potentially loses the frequency synchronization function; switching frequency is unstable.	B
SYNCIN	24	CFG2	There is a loss of the frequency synchronization function or Configuration 2 is incorrect (or both—loss of function and incorrect configuration).	B
CFG2	25	CFG1	Configuration 1 or Configuration 2 (or both) are incorrect for the device.	B
CFG1	26	CFG0	Configuration 1 or Configuration 2 (or both) are incorrect for the device.	B
CFG0	27	PGOOD	The device loses the function of Configuration 0.	B
PGOOD	28	MODE	The MODE function of the device is effected. The device potentially functions in an operation mode that is incorrect based on the PGOOD output.	C
MODE	29	EN2	The incorrect operation MODE or phase 2 enables or disables incorrectly, depending on the voltage that is driven.	B
EN2	30	ILIM/IMON	The device is forced to function in average-input-current limit mode if the EN2 pin is driven high. The function of the ILIM/IMON pin is lost if the EN2 pin is driven low.	B
ILIM/IMON	31	ATRK/DTRK	The voltage of the output is not regulated to target the intended value, and the function of the IMON/ILIM pin is lost.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
ATRK/DTRK	32	DLY	The voltage of the output is not regulated to target the intended value. The average-input-current limit does not work as intended.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to V_I

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
DLY	1	Device damage is possible; exceeds the absolute maximum voltage rating.	A
SS	2	Device damage is possible; exceeds the absolute maximum voltage rating.	A
COMP	3	Device damage is possible; exceeds the absolute maximum voltage rating.	A
AGND	4	Device damage is possible; exceeds the absolute maximum voltage rating.	A
CSN1	5	There is a loss of the current sense signal. The circuit is potentially unstable.	B
CSP1	6	Normal operation.	D
VOUT	7	There is a loss of V_{OUT} regulation as the output voltage is forced to V_I.	B
HO1	8	Device damage is possible as the HO1 pin potentially exceeds the absolute maximum voltage ratings at the pin locations of HO1 to SW1.	A
HB1	9	Device damage is possible as the HB1 pin exceeds the absolute maximum voltage ratings at the pin locations of HB1 to SW1.	A
SW1	10	Energy is not transferred from input to output.	B
LO1	11	Device damage is possible; exceeds the absolute maximum voltage rating.	A
VCC	12	Device damage is possible; exceeds the absolute maximum voltage rating.	A
PGND	13	Device damage is possible.	A
LO2	14	Device damage is possible; exceeds the absolute maximum voltage rating.	A
SW2	15	Energy is not transferred from input to output.	B
HB2	16	Device damage is possible as the HB2 pin potentially exceeds the absolute maximum voltage ratings at the pin locations of HB2 to SW2.	A
HO2	17	Device damage is possible as the HO2 pin potentially exceeds the absolute maximum voltage ratings at the pin locations of HO2 to SW2.	A
BIAS	18	Normal operation.	D
UVLO/EN	19	No UVLO functionality, the device is enabled or disabled with V_I.	B C
CSP2	20	Normal operation.	D
CSN2	21	There is a loss of the current sense signal. The circuit is potentially unstable.	B
RT	22	Device damage is possible; exceeds the absolute maximum voltage rating.	A
NC	23	The device is potentially damaged.	A
SYNCIN	24	Device damage is possible; exceeds the absolute maximum voltage rating.	A
CFG2/SDA	25	Device damage is possible; exceeds the absolute maximum voltage rating.	A
CFG1/SCL	26	Device damage is possible; exceeds the absolute maximum voltage rating.	A
CFG0/CFG	27	Device damage is possible; exceeds the absolute maximum voltage rating.	A
PGOOD	28	Device damage is possible; exceeds the absolute maximum voltage rating.	A
MODE	29	Device damage is possible; exceeds the absolute maximum voltage rating.	A
EN2	30	Device damage is possible; exceeds the absolute maximum voltage rating.	A
ILIM/IMON	31	Device damage is possible; exceeds the absolute maximum voltage rating.	A
ATRK/DTRK	32	Device damage is possible; exceeds the absolute maximum voltage rating.	A

4.2 LM5125A-Q1 (VQFN) Package

Figure 4-2 shows the LM5125A-Q1 pin diagram for the VQFN package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the LM5125A-Q1 data sheet.

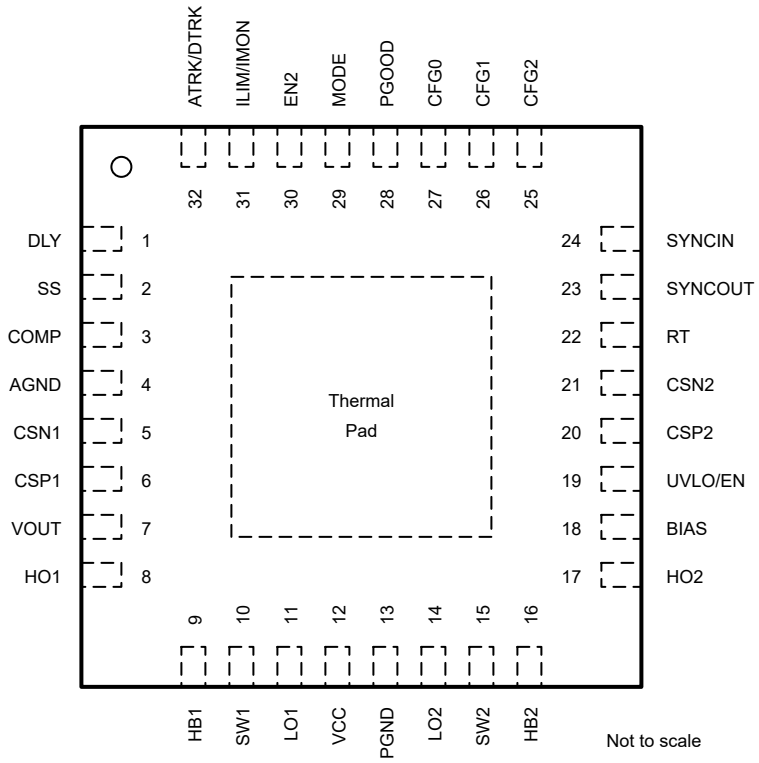

Figure 4-2. Pin Diagram (VQFN) Package

Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
DLY	1	The average-input-current loop is not activated when the average-input-current loop feature is used.	B
			D
SS	2	The device does not start; no switching.	B
COMP	3	V_{OUT} is out of regulation; not switching.	B
AGND	4	No effect.	D
CSN1	5	The device is potentially damaged if the differential voltage exceeds the absolute maximum rating of 0.3V.	A
CSP1	6	The device is potentially damaged if the differential voltage exceeds the absolute maximum rating of 0.3V.	A
VOUT	7	The external components are potentially damaged. The device potentially goes into a latch state or does not start.	B
HO1	8	The phase-1 high-side driver is potentially damaged when the device starts switching.	A
HB1	9	The device is potentially damaged when BOOT charging starts.	A
SW1	10	No energy is transferred from the input to the output.	B
LO1	11	The phase-1 low-side driver is potentially damaged when the device starts switching.	A
VCC	12	There is a loss of VCC regulation; no switching.	B
PGND	13	No effect.	D
LO2	14	The phase-1 low-side driver is potentially damaged when the device starts switching.	A
SW2	15	No energy is transferred from the input to the output.	B
HB2	16	The device is potentially damaged when BOOT charging starts.	A
HO2	17	The phase-2 high-side driver is potentially damaged when the device starts switching.	A
BIAS	18	The device is not powered, and therefore, not functional.	B
UVLO/EN	19	The device is disabled.	B
CSP2	20	The device is potentially damaged if the differential voltage exceeds the absolute maximum rating of 0.3V.	A
CSN2	21	The device is potentially damaged if the differential voltage exceeds the absolute maximum rating of 0.3V.	A
RT	22	The device goes to the maximum switching frequency of >2.2MHz.	C
SYNCOUT	23	The device is potentially damaged if the device configuration has the SYNCOUT function enabled.	A
			D
SYNCIN	24	Clock synchronization is disabled; the device uses the internal clock.	C
CFG2	25	Level 1 of the CFG2 pin is forced.	C
CFG1	26	Level 1 of the CFG1 pin is forced.	C
CFG0	27	Level 1 of the CFG0 pin is forced.	C
PGOOD	28	The voltage of the output is correct, but there is a loss of functionality at the PGOOD pin.	B
MODE	29	Diode emulation mode is activated. There is no effect if the device is configured for diode emulation mode (MODE = GND).	C
			D
EN2	30	Second phase is disabled if second phase is used.	C
			D
ILIM/IMON	31	The average-input-current loop is not activated; current monitoring does not work.	B
ATRK/DTRK	32	There is no output voltage regulation. The device enters BYPASS mode after the soft start completes.	B

Table 4-7. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
DLY	1	Delayed programming does not work if the delay pin function is used.	B
			D
SS	2	There is a short soft-start time.	C
COMP	3	The device is potentially unstable.	B
AGND	4	Device damage is possible.	A
CSN1	5	There is a loss of the current sense signal for phase 1. Peak-current limit does not work.	B
CSP1	6	There is a loss of the current sense signal for phase 1. Peak-current limit does not work.	B
VOUT	7	The internal feedback voltage for the regulation loop is pulled to GND; V_{OUT} reaches OVP_{max}.	B
HO1	8	There is a loss of the high-side driver.	B
HB1	9	There is a loss of boot voltage, and hence, a loss of the high-side driver.	B
SW1	10	There is a loss of the high-side driver.	B
LO1	11	The low-side MOSFET does not switch for phase 1.	B
VCC	12	The VCC pin is not stable enough to sustain normal operation.	B
PGND	13	Device damage is possible.	A
LO2	14	The low-side MOSFET does not switch for phase 2.	B
SW2	15	There is a loss of the high-side driver.	B
HB2	16	There is a loss of boot voltage, and hence, a loss of the high-side driver.	B
HO2	17	There is a loss of the high-side driver.	B
BIAS	18	The device is not powered, and therefore, not functional.	B
UVLO/EN	19	The device is disabled.	B
CSP2	20	There is a loss of the current sense signal for phase 2. Peak-current limit does not work.	B
CSN2	21	There is a loss of the current sense signal for phase 2. Peak-current limit does not work.	B
RT	22	The minimum frequency is set.	C
SYNCOUT	23	The primary device functions normally. The secondary device does not get a switching clock in a multi-device configuration.	C
			B
SYNCIN	24	Clock synchronization does not work; the device uses the internal clock.	C
CFG2	25	Level 16 of the CFG2 pin is forced.	C
CFG1	26	Level 16 of the CFG1 pin is forced.	C
CFG0	27	Level 16 of the CFG0 pin is forced.	C
PGOOD	28	The output voltage is correct, but there is a loss of functionality at the PGOOD pin.	B
MODE	29	There is no effect if DEM mode is active, otherwise, DEM mode is activated.	D
			C
EN2	30	Second-phase enable potentially does not function as intended.	C
ILIM/IMON	31	The device operates in an average-input-current limit loop operation; V_{OUT} drops, and therefore, V_{OUT} is out of regulation.	B
ATRK/DTRK	32	The device goes to OVP_{max}.	B

Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
DLY	1	SS	There is a loss of the delay function; the average-input-current loop does not function as intended.	B
SS	2	COMP	The device operates in peak-current limit and the output voltage rises to OVP_{max}.	B
COMP	3	AGND	The V_{OUT} regulation loop does not function, the internal supply potentially collapses.	B
AGND	4	CSN1	The device is potentially damaged if the differential voltage exceeds the absolute maximum rating of 0.3V.	A
CSN1	5	CSP1	There is a loss of current sense information. The circuit is potentially unstable.	B
CSP1	6	VOUT	The output is shorted to the input supply. There is no output regulation.	B
VOUT	7	HO1	Device damage is possible as the HO1 pin exceeds the absolute maximum voltage rating to switch.	A
HO1	8	HB1	Device damage is possible when switching starts.	A
HB1	9	SW1	There is a loss of the high-side driver.	B
SW1	10	LO1	Device damage is possible as the absolute maximum rating is exceeded at the LO1 pin.	A
LO1	11	VCC	The LO1 pin does not switch. Device damage is possible when switching starts.	A
VCC	12	PGND	There is no VCC rail; no switching.	B
PGND	13	LO2	Device damaged is possible when switching starts.	A
LO2	14	SW2	Device damage is possible as the absolute maximum rating is exceeded at the LO2 pin.	A
SW2	15	HB2	There is a loss of the high-side driver.	B
HB2	16	HO2	Device damage is possible when switching starts.	A
HO2	17	BIAS	Device damage is possible as the HO2 pin potentially exceeds the absolute maximum voltage ratings at the pin locations of HO2 to SW2.	A
BIAS	18	UVLO/EN	There is a loss of the UVLO function; the device is always enabled.	B C
UVLO/EN	19	CSP2	There is incorrect current sense information, the current limit is potentially incorrect.	B
CSP2	20	CSN2	There is a loss of current sense information. The circuit is potentially unstable.	B
CSN2	21	RT	Device damage is possible. The CSN2 pin exceeds the absolute maximum voltage rating for the RT pin.	A
RT	22	SYNCOUT	The device operates at the maximum switching frequency at start-up. When the SYNCOUT pin starts switching, switching is unstable.	C
SYNCOUT	23	SYNCIN	There is a loss of the frequency synchronization function; switching frequency is unstable.	B
SYNCIN	24	CFG2	There is a loss of the frequency synchronization function or Configuration 2 is incorrect (or both—loss of function and incorrect configuration).	B
CFG2	25	CFG1	Configuration 1 or Configuration 2 (or both) are incorrect for the device.	B
CFG1	26	CFG0	Configuration 1 or Configuration 2 (or both) are incorrect for the device.	B
CFG0	27	PGOOD	The device loses the function of Configuration 0.	B
PGOOD	28	MODE	The MODE function of the device is effected. The device potentially functions in an operation mode that is incorrect based on the PGOOD output.	C
MODE	29	EN2	The incorrect operation MODE or phase 2 enables or disables incorrectly, depending on the voltage that is driven.	B
EN2	30	ILIM/IMON	The device is forced to function in average-input-current limit mode if the EN2 pin is driven high. The function of the ILIM/IMON pin is lost if the EN2 pin is driven low.	B
ILIM/IMON	31	ATRK/DTRK	The voltage of the output is not regulated to target the intended value, and the function of the IMON/ILIM pin is lost.	B

Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
ATRK/DTRK	32	DLY	The voltage of the output is not regulated to target the intended value. The average-input-current limit does not work as intended.	B

Table 4-9. Pin FMA for Device Pins Short-Circuited to V_I

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
DLY	1	Device damage is possible; exceeds the absolute maximum voltage rating.	A
SS	2	Device damage is possible; exceeds the absolute maximum voltage rating.	A
COMP	3	Device damage is possible; exceeds the absolute maximum voltage rating.	A
AGND	4	Device damage is possible; exceeds the absolute maximum voltage rating.	A
CSN1	5	There is a loss of the current sense signal. The circuit is potentially unstable.	B
CSP1	6	Normal operation.	D
VOUT	7	There is a loss of V_{OUT} regulation as the output voltage is forced to V_I.	B
HO1	8	Device damage is possible as the HO1 pin potentially exceeds the absolute maximum voltage ratings at the pin locations of HO1 to SW1.	A
HB1	9	Device damage is possible as the HB1 pin exceeds the absolute maximum voltage ratings at the pin locations of HB1 to SW1.	A
SW1	10	Energy is not transferred from input to output.	B
LO1	11	Device damage is possible; exceeds the absolute maximum voltage rating.	A
VCC	12	Device damage is possible; exceeds the absolute maximum voltage rating.	A
PGND	13	Device damage is possible.	A
LO2	14	Device damage is possible; exceeds the absolute maximum voltage rating.	A
SW2	15	Energy is not transferred from input to output.	B
HB2	16	Device damage is possible as the HB2 pin potentially exceeds the absolute maximum voltage ratings at the pin locations of HB2 to SW2.	A
HO2	17	Device damage is possible as the HO2 pin potentially exceeds the absolute maximum voltage ratings at the pin locations of HO2 to SW2.	A
BIAS	18	Normal operation.	D
UVLO/EN	19	No UVLO functionality, the device is enabled or disabled with V_I.	B C
CSP2	20	Normal operation.	D
CSN2	21	There is a loss of the current sense signal. The circuit is potentially unstable.	B
RT	22	Device damage is possible; exceeds the absolute maximum voltage rating.	A
SYNCOUT	23	The device is potentially damaged; exceeds the absolute maximum voltage rating.	A
SYNCIN	24	Device damage is possible; exceeds the absolute maximum voltage rating.	A
CFG2/SDA	25	Device damage is possible; exceeds the absolute maximum voltage rating.	A
CFG1/SCL	26	Device damage is possible; exceeds the absolute maximum voltage rating.	A
CFG0/CFG	27	Device damage is possible; exceeds the absolute maximum voltage rating.	A
PGOOD	28	Device damage is possible; exceeds the absolute maximum voltage rating.	A
MODE	29	Device damage is possible; exceeds the absolute maximum voltage rating.	A
EN2	30	Device damage is possible; exceeds the absolute maximum voltage rating.	A
ILIM/IMON	31	Device damage is possible; exceeds the absolute maximum voltage rating.	A
ATRK/DTRK	32	Device damage is possible; exceeds the absolute maximum voltage rating.	A

4.3 LM51251A-Q1 (VQFN) Package

Figure 4-3 shows the LM51251A-Q1 pin diagram for the VQFN package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the LM51251A-Q1 data sheet.

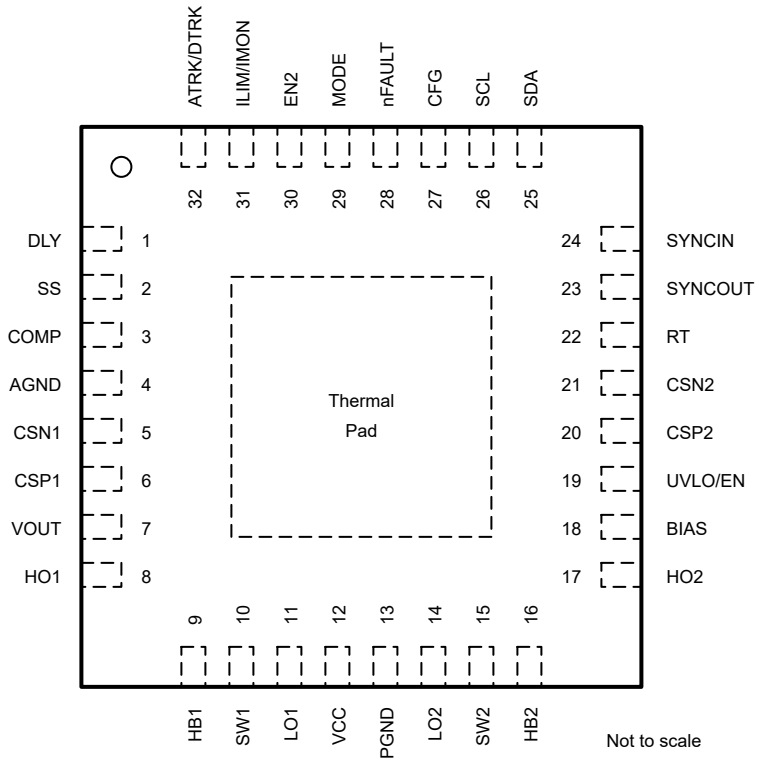

Figure 4-3. Pin Diagram (VQFN) Package

Table 4-10. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
DLY	1	The average-input-current loop is not activated when the average-input-current loop feature is used.	B
			D
SS	2	The device does not start; no switching.	B
COMP	3	V_{OUT} is out of regulation; not switching.	B
AGND	4	No effect.	D
CSN1	5	The device is potentially damaged if the differential voltage exceeds the absolute maximum rating of 0.3V.	A
CSP1	6	The device is potentially damaged if the differential voltage exceeds the absolute maximum rating of 0.3V.	A
VOUT	7	The external components are potentially damaged. The device potentially goes into a latch state or does not start.	B
HO1	8	The phase-1 high-side driver is potentially damaged when the device starts switching.	A
HB1	9	The device is potentially damaged when BOOT charging starts.	A
SW1	10	No energy is transferred from the input to the output.	B
LO1	11	The phase-1 low-side driver is potentially damaged when the device starts switching.	A
VCC	12	There is a loss of VCC regulation; no switching.	B
PGND	13	No effect.	D
LO2	14	The phase-1 low-side driver is potentially damaged when the device starts switching.	A
SW2	15	No energy is transferred from the input to the output.	B
HB2	16	The device is potentially damaged when BOOT charging starts.	A
HO2	17	The phase-2 high-side driver is potentially damaged when the device starts switching.	A
BIAS	18	The device is not powered, and therefore, not functional.	B
UVLO/EN	19	The device is disabled.	B
CSP2	20	The device is potentially damaged if the differential voltage exceeds the absolute maximum rating of 0.3V.	A
CSN2	21	The device is potentially damaged if the differential voltage exceeds the absolute maximum rating of 0.3V.	A
RT	22	The device goes to the maximum switching frequency of >2.2MHz.	C
SYNCOUT	23	The device is potentially damaged if the device configuration has the SYNCOUT function enabled.	A
			D
SYNCIN	24	Clock synchronization is disabled; the device uses the internal clock.	C
SDA	25	I2C communication does not work.	B
SCL	26	I2C communication does not work.	B
CFG	27	Level 1 of the CFG pin is forced.	C
nFAULT	28	The voltage of the output is correct, but there is a loss of functionality at the nFAULT pin.	B
MODE	29	Diode emulation mode is activated. There is no effect if the device is configured for diode emulation mode (MODE = GND).	C
			D
EN2	30	Second phase is disabled if second phase is used.	C
			D
ILIM/IMON	31	The average-input-current loop is not activated; current monitoring does not work.	B
ATRK/DTRK	32	There is no output voltage regulation. The device enters BYPASS mode after the soft start completes.	B

Table 4-11. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
DLY	1	Delayed programming does not work if the delay pin function is used.	B
			D
SS	2	There is a short soft-start time.	C
COMP	3	The device is potentially unstable.	B
AGND	4	Device damage is possible.	A
CSN1	5	There is a loss of the current sense signal for phase 1. Peak-current limit does not work.	B
CSP1	6	There is a loss of the current sense signal for phase 1. Peak-current limit does not work.	B
VOUT	7	The internal feedback voltage for the regulation loop is pulled to GND; V_{OUT} reaches OVP_{max}.	B
HO1	8	There is a loss of the high-side driver.	B
HB1	9	There is a loss of boot voltage, and hence, a loss of the high-side driver.	B
SW1	10	There is a loss of the high-side driver.	B
LO1	11	The low-side MOSFET does not switch for phase 1.	B
VCC	12	The VCC pin is not stable enough to sustain normal operation.	B
PGND	13	Device damage is possible.	A
LO2	14	The low-side MOSFET does not switch for phase 2.	B
SW2	15	There is a loss of the high-side driver.	B
HB2	16	There is a loss of boot voltage, and hence, a loss of the high-side driver.	B
HO2	17	There is a loss of the high-side driver.	B
BIAS	18	The device is not powered, and therefore, not functional.	B
UVLO/EN	19	The device is disabled.	B
CSP2	20	There is a loss of the current sense signal for phase 2. Peak-current limit does not work.	B
CSN2	21	There is a loss of the current sense signal for phase 2. Peak-current limit does not work.	B
RT	22	The minimum frequency is set.	C
SYNCOUT	23	The primary device functions normally. The secondary device does not get a switching clock in a multi-device configuration.	C
			B
SYNCIN	24	Clock synchronization does not work; the device uses the internal clock.	C
SDA	25	I2C communication does not work.	B
SCL	26	I2C communication does not work.	B
CFG	27	Level 16 of the CFG pin is forced.	C
nFAULT	28	The output voltage is correct, but there is a loss of functionality at the nFAULT pin.	B
MODE	29	There is no effect if DEM mode is active, otherwise, DEM mode is activated.	D
			C
EN2	30	Second-phase enable potentially does not function as intended.	C
ILIM/IMON	31	The device operates in an average-input-current limit loop operation; V_{OUT} drops, and therefore, V_{OUT} is out of regulation.	B
ATRK/DTRK	32	The device goes to OVP_{max}.	B

Table 4-12. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
DLY	1	SS	There is a loss of the delay function; the average-input-current loop does not function as intended.	B
SS	2	COMP	The device operates in peak-current limit and the output voltage rises to OVP_{max}.	B
COMP	3	AGND	The V_{OUT} regulation loop does not function, the internal supply potentially collapses.	B
AGND	4	CSN1	The device is potentially damaged if the differential voltage exceeds the absolute maximum rating of 0.3V.	A
CSN1	5	CSP1	There is a loss of current sense information. The circuit is potentially unstable.	B
CSP1	6	VOUT	The output is shorted to the input supply. There is no output regulation.	B
VOUT	7	HO1	Device damage is possible as the HO1 pin exceeds the absolute maximum voltage rating to switch.	A
HO1	8	HB1	Device damage is possible when switching starts.	A
HB1	9	SW1	There is a loss of the high-side driver.	B
SW1	10	LO1	Device damage is possible as the absolute maximum rating is exceeded at the LO1 pin.	A
LO1	11	VCC	The LO1 pin does not switch. Device damage is possible when switching starts.	A
VCC	12	PGND	There is no VCC rail; no switching.	B
PGND	13	LO2	Device damaged is possible when switching starts.	A
LO2	14	SW2	Device damage is possible as the absolute maximum rating is exceeded at the LO2 pin.	A
SW2	15	HB2	There is a loss of the high-side driver.	B
HB2	16	HO2	Device damage is possible when switching starts.	A
HO2	17	BIAS	Device damage is possible as the HO2 pin potentially exceeds the absolute maximum voltage ratings at the pin locations of HO2 to SW2.	A
BIAS	18	UVLO/EN	There is a loss of the UVLO function; the device is always enabled.	B C
UVLO/EN	19	CSP2	There is incorrect current sense information, the current limit is potentially incorrect.	B
CSP2	20	CSN2	There is a loss of current sense information. The circuit is potentially unstable.	B
CSN2	21	RT	Device damage is possible. The CSN2 pin exceeds the absolute maximum voltage rating for the RT pin.	A
RT	22	SYNCOUT	The device operates at the maximum switching frequency at start-up. When the SYNCOUT pin starts switching, switching is unstable.	C
SYNCOUT	23	SYNCIN	There is a loss of the frequency synchronization function; switching frequency is unstable.	B
SYNCIN	24	SDA	I2C communication does not working when an external clock is used or the SYNCIN pin is connected to GND. I2C operates normally when the SYNCIN pin is left floating. The device potentially synchronizes to the SDA signal when clock synchronization is enabled. There is a loss of the frequency synchronization function.	B
SDA	25	SCL	I2C communication does not work.	B
SCL	26	CFG	I2C communication does not work for the device if the resistance of the CFG pin is strong enough to pull down the I2C clock. The device configuration for the CFG pin is incorrect.	B
CFG	27	nFAULT	The device loses the function of the configuration.	B
nFAULT	28	MODE	The MODE function of the device is effected. The device potentially functions in an operation mode that is incorrect based on the nFAULT output.	C
MODE	29	EN2	The incorrect operation MODE or phase 2 enables or disables incorrectly depending on the voltage that is driven.	B

Table 4-12. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
EN2	30	ILIM/IMON	The device is forced to function in average-input-current limit mode if the EN2 pin is driven high. The function of the ILIM/IMON pin is lost if the EN2 pin is driven low.	B
ILIM/IMON	31	ATRK/DTRK	The voltage of the output is not regulated to target the intended value, and the function of the IMON/ILIM pin is lost.	B
ATRK/DTRK	32	DLY	The voltage of the output is not regulated to target the intended value. The average-input-current limit does not work as intended.	B

Table 4-13. Pin FMA for Device Pins Short-Circuited to V_I

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
DLY	1	Device damage is possible; exceeds the absolute maximum voltage rating.	A
SS	2	Device damage is possible; exceeds the absolute maximum voltage rating.	A
COMP	3	Device damage is possible; exceeds the absolute maximum voltage rating.	A
AGND	4	Device damage is possible; exceeds the absolute maximum voltage rating.	A
CSN1	5	There is a loss of the current sense signal. The circuit is potentially unstable.	B
CSP1	6	Normal operation.	D
VOUT	7	There is a loss of V_{OUT} regulation as the output voltage is forced to V_I.	B
HO1	8	Device damage is possible as the HO1 pin potentially exceeds the absolute maximum voltage ratings at the pin locations of HO1 to SW1.	A
HB1	9	Device damage is possible as the HB1 pin exceeds the absolute maximum voltage ratings at the pin locations of HB1 to SW1.	A
SW1	10	Energy is not transferred from input to output.	B
LO1	11	Device damage is possible; exceeds the absolute maximum voltage rating.	A
VCC	12	Device damage is possible; exceeds the absolute maximum voltage rating.	A
PGND	13	Device damage is possible.	A
LO2	14	Device damage is possible; exceeds the absolute maximum voltage rating.	A
SW2	15	Energy is not transferred from input to output.	B
HB2	16	Device damage is possible as the HB2 pin potentially exceeds the absolute maximum voltage ratings at the pin locations of HB2 to SW2.	A
HO2	17	Device damage is possible as the HO2 pin potentially exceeds the absolute maximum voltage ratings at the pin locations of HO2 to SW2.	A
BIAS	18	Normal operation.	D
UVLO/EN	19	No UVLO functionality, the device is enabled or disabled with V_I.	B C
CSP2	20	Normal operation.	D
CSN2	21	There is a loss of the current sense signal. The circuit is potentially unstable.	B
RT	22	Device damage is possible; exceeds the absolute maximum voltage rating.	A
SYNCOUT	23	The device is potentially damaged; exceeds the absolute maximum voltage rating.	A
SYNCIN	24	Device damage is possible; exceeds the absolute maximum voltage rating.	A
SDA	25	Device damage is possible; exceeds the absolute maximum voltage rating.	A
SCL	26	Device damage is possible; exceeds the absolute maximum voltage rating.	A
CFG	27	Device damage is possible; exceeds the absolute maximum voltage rating.	A
nFAULT	28	Device damage is possible; exceeds the absolute maximum voltage rating.	A
MODE	29	Device damage is possible; exceeds the absolute maximum voltage rating.	A
EN2	30	Device damage is possible; exceeds the absolute maximum voltage rating.	A
ILIM/IMON	31	Device damage is possible; exceeds the absolute maximum voltage rating.	A

Table 4-13. Pin FMA for Device Pins Short-Circuited to V_I (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
ATRK/DTRK	32	Device damage is possible; exceeds the absolute maximum voltage rating.	A

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2024) to Revision A (September 2025)	Page
• Added the LM5125A-Q1 and LM51251A-Q1 devices	2

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