Functional Safety Information

LM5125-Q1 Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

1 Overview 2
2 Functional Safety Failure In Time (FIT) Rates 3
2.1 VQFN Package 3
3 Failure Mode Distribution (FMD) 4
4 Pin Failure Mode Analysis (Pin FMA) 5
4.1 VQFN Package 5
5 Revision History 9

Trademarks

1 Overview

This document contains information for the LM5125-Q1 (VQFN package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

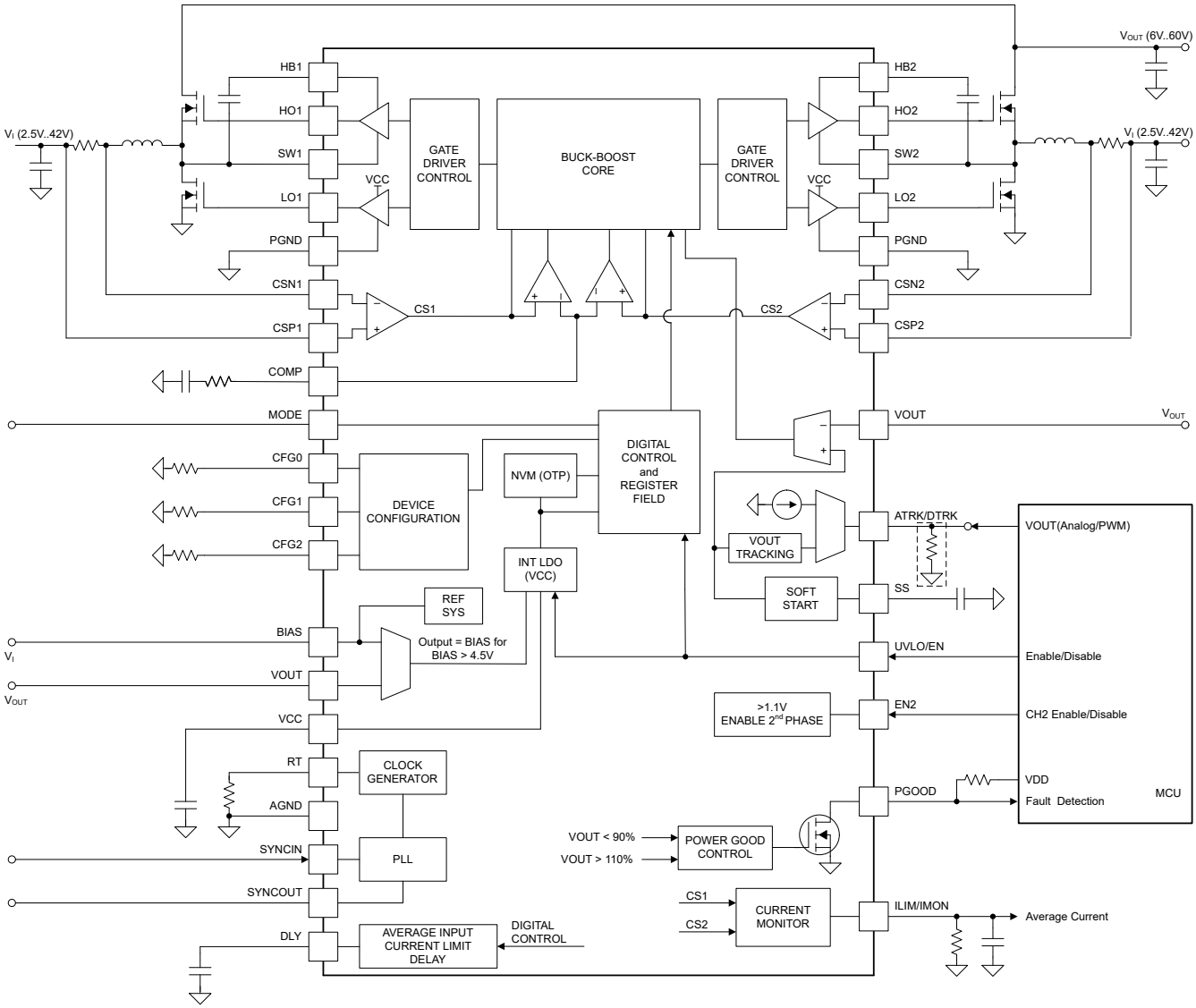

Figure 1-1. Functional Block Diagram

The LM5125-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 VQFN Package

This section provides functional safety failure in time (FIT) rates for the VQFN package of the LM5125-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	25
Die FIT rate	7
Package FIT rate	18

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 1000mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS/BICMOS ASICs analog and mixed HV >50V supply	-	75°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the LM5125-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
HO1/2 or LO1/2 gate driver is stuck on	5
HO1/2 or LO1/2 gate driver is stuck off	15
HO1/2 or LO1/2 gate driver is Hi-Z	5
VCC LDO output voltage out of specification	15
V_{OUT} voltage out of specification	40
PGOOD false or fails to trip	10
Digital control malfunctions or electrical parameters out of specification	10

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the LM5125-Q1 (VQFN package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to V_I (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Device used within the *Recommended Operation Conditions* and the *Absolute Maximum Ratings* found in the LM5125-Q1 data sheet
- For the analysis, the typical application is used as shown in the *Typical Application* section of the LM5125-Q1
- V_{SUPPLY} = 12V
- V_{OUT} = 24V

4.1 VQFN Package

Figure 4-1 shows the LM5125-Q1 pin diagram for the VQFN package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the LM5125-Q1 data sheet.

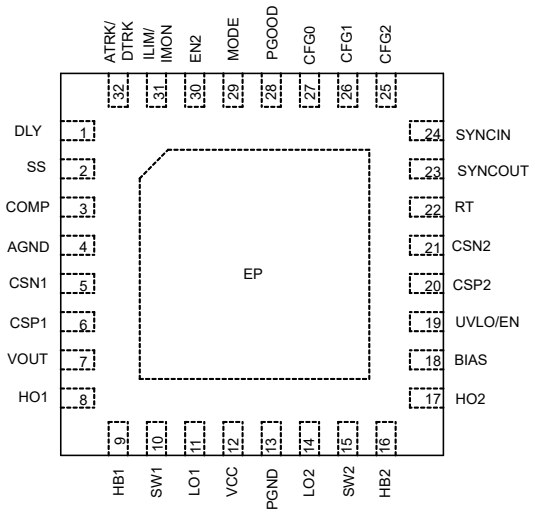

Figure 4-1. Pin Diagram (VQFN) Package

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
DLY	1	If average input current loop feature is used the average input current loop is not get activated.	B D
SS	2	Device does not start, no switching.	B
COMP	3	V_{OUT} out of regulation, not switching.	B
AGND	4	No effect.	D
CSN1	5	Device can be damaged if the differential voltage exceeds the 0.3V absolute maximum rating.	A
CSP1	6	Device can be damaged if the differential voltage exceeds the 0.3V absolute maximum rating.	A
VOUT	7	External components can be damaged. Device potentially goes into latch state or does not start.	B
HO1	8	Phase 1 high-side driver can be damaged when device starts switching.	A
HB1	9	Device can be damaged when BOOT charging starts.	A
SW1	10	No energy transferred from input to output.	B
LO1	11	Phase 1 low-side driver can be damaged when device starts switching.	A
VCC	12	Loss of VCC regulation, no switching.	B
PGND	13	No effect.	D
LO2	14	Phase 1 low-side driver can be damaged when device starts switching.	A
SW2	15	No energy transferred from input to output.	B
HB2	16	Device can be damaged when BOOT charging starts.	A
HO2	17	Phase 2 high-side driver can be damaged when device starts switching.	A
BIAS	18	Device not powered and therefore not functional.	B
UVLO/EN	19	Device is disabled.	B
CSP2	20	Device can be damaged if the differential voltage exceeds the 0.3V absolute maximum rating.	A
CSN2	21	Device can be damaged if the differential voltage exceeds the 0.3V absolute maximum rating.	A
RT	22	Device goes to maximum switching frequency >2.2MHz.	C
SYNCOUT	23	SYNCOUT-pin can be damaged if device configuration has SYNCOUT function enabled.	A D
SYNCIN	24	Clock synchronization is disabled, device uses internal clock.	C
CFG2	25	CFG2 level-1 is forced.	C
CFG1	26	CFG1 level-1 is forced.	C
CFG0	27	CFG0 level-1 is forced.	C
PGOOD	28	Correct output voltage, but loss of power-good functionality.	B
MODE	29	Diode emulation mode is activated. No effect if the device is configured for diode emulation mode (MODE = GND).	C D
EN2	30	If second phase is used, second phase is disabled.	C D
ILIM/IMON	31	Average input current loop is not activated. Current monitoring is not working.	B
ATRK/DTRK	32	No output voltage regulation. Device enters BYPASS mode after soft start is complete.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
DLY	1	If delay pin function is used, the delay programming does not work.	B D
SS	2	Short soft-start time.	C
COMP	3	Device can be unstable.	B
AGND	4	Possible device damage.	A

Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
CSN1	5	Loss of current sense signal for phase 1. Peak current limit does not work.	B
CSP1	6	Loss of current sense signal for phase 1. Peak current limit does not work.	B
VOUT	7	Internal feedback voltage for regulation loop is pulled to GND, V_{OUT} reaches OVP_max.	B
HO1	8	Loss of high-side driver.	B
HB1	9	Loss of boot voltage and hence high-side driver.	B
SW1	10	Loss of high-side driver.	B
LO1	11	Low-side MOSFET never switched for phase 1.	B
VCC	12	No stable VCC to sustain normal operation.	B
PGND	13	Possible device damage.	A
LO2	14	Low-side MOSFET never switched for phase 2.	B
SW2	15	Loss of high-side driver.	B
HB2	16	Loss of boot voltage and hence high side driver.	B
HO2	17	Loss of high side driver.	B
BIAS	18	Device not powered and therefore not functional.	B
UVLO/EN	19	Device is disabled.	B
CSP2	20	Loss of current sense signal for phase 2. Peak current limit does not work.	B
CSN2	21	Loss of current sense signal for phase 2. Peak current limit does not work.	B
RT	22	Minimum frequency is set.	C
SYNCOUT	23	Primary functions normally. Secondary does not get clock in multi-device configuration.	C B
SYNCIN	24	Clock synchronization is not working, device uses internal clock.	C
CFG2	25	CFG2 level-16 is forced.	C
CFG1	26	CFG1 level-16 is forced.	C
CFG0	27	CFG0 level-16 is forced.	C
PGOOD	28	Correct output voltage, but loss of power-good functionality.	B
MODE	29	No effect if DEM mode is active, otherwise DEM mode is activated.	D C
EN2	30	Second phase enable potentially does not function as intended.	C
ILIM/IMON	31	Device operates in average input current limit loop operation, V_{OUT} drops and is therefore out of regulation.	B
ATRK/DTRK	32	Device goes to OVP_{max}.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
DLY	1	SS	Loss of delay function, average input current loop does not function as intended.	B
SS	2	COMP	Device operates in peak current limit and output voltage rises to OVP_{max}.	B
COMP	3	AGND	V_{OUT} regulation loop does not function, internal supply can collapse.	B
AGND	4	CSN1	Device can be damaged due to the differential voltage exceeds the 0.3V absolute maximum rating.	A
CSN1	5	CSP1	Loss of current sense information. Circuit possibly unstable.	B
CSP1	6	VOUT	Output shorted to input supply. No output regulation.	B
VOUT	7	HO1	Possible device damage as HO to switch exceeds absolute maximum voltage rating.	A
HO1	8	HB1	Possible device damage when switching starts.	A
HB1	9	SW1	Loss of high side driver.	B
SW1	10	LO1	Possible device damage as absolute maximum rating exceeded at LO-pin.	A
LO1	11	VCC	LO not switching. Possible device damage when switching starts.	A
VCC	12	PGND	No VCC rail, no switching.	B
PGND	13	LO2	Device can be damaged when switching starts.	A
LO2	14	SW2	Possible device damage as absolute maximum rating exceeded at LO-pin.	A
SW2	15	HB2	Loss of high side driver.	B
HB2	16	HO2	Possible device damage when switching starts.	A
HO2	17	BIAS	Possible damage as HO2-pin can exceed the HO2 to SW2 absolute maximum voltage rating.	A
BIAS	18	UVLO/EN	Loss of UVLO function, device always enabled.	B
				C
UVLO/EN	19	CSP2	Wrong current sense information, current limit can be wrong.	B
CSP2	20	CSN2	Loss of current sense information. Circuit possibly unstable.	B
CSN2	21	RT	Possible device damage. Exceeds absolute maximum voltage rating for RT.	A
RT	22	SYNCOUT	Device operates at maximum switching frequency at start-up. When SYNCOUT starts switching, switching is unstable.	C
SYNCOUT	23	SYNCIN	Loss of frequency sync function, unstable switching frequency.	B
SYNCIN	24	CFG2	Loss of frequency sync function and/or wrong configuration 2.	B
CFG2	25	CFG1	Wrong configuration 1 and/or configuration 2.	B
CFG1	26	CFG0	Wrong configuration 1 and/or configuration 0.	B
CFG0	27	PGOOD	Loss of configuration 0 function.	B
PGOOD	28	MODE	MODE function effected, device can function in incorrect operation mode based on PGOOD output.	C
MODE	29	EN2	Wrong operation MODE or phase 2 enabled or disabled incorrectly depending on what voltage is driven.	B
EN2	30	ILIM/IMON	If EN2 is driven high, then the device is forced to function in average input current limit mode. If driven low, loss of ILIM/IMON function.	B
ILIM/IMON	31	ATRK/DTRK	Output voltage not regulated to target intended value and loss of IMON/ILIM function.	B
ATRK/DTRK	32	DLY	Output voltage is not regulated to target intended value, average input current limit does not work as intended.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to V_I

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
DLY	1	Possible device damage. Exceeds absolute maximum voltage rating.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to V_I (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
SS	2	Possible device damage. Exceeds absolute maximum voltage rating.	A
COMP	3	Possible device damage. Exceeds absolute maximum voltage rating.	A
AGND	4	Possible device damage. Exceeds absolute maximum voltage rating.	A
CSN1	5	Loss of current sense signal. Circuit possibly unstable.	B
CSP1	6	Normal operation.	D
VOUT	7	Loss of V_{OUT} regulation as output voltage is forced to V_I.	B
HO1	8	Possible device damage as HO1-pin can exceed the HO1 to SW1 absolute maximum voltage rating.	A
HB1	9	Possible device damage as HB1 exceeds HB1 to SW1 absolute maximum voltage rating.	A
SW1	10	No energy is transferred from input to output.	B
LO1	11	Possible device damage. Exceeds absolute maximum voltage rating.	A
VCC	12	Possible device damage. Exceeds absolute maximum voltage rating.	A
PGND	13	Possible device damage.	A
LO2	14	Possible device damage. Exceeds absolute maximum voltage rating.	A
SW2	15	No energy is transferred from input to output.	B
HB2	16	Possible device damage as HB2 exceeds HB2 to SW2 absolute maximum voltage rating.	A
HO2	17	Possible device damage as HO2 pin can exceed the HO2 to SW2 absolute maximum voltage rating.	A
BIAS	18	Normal operation.	D
UVLO/EN	19	No UVLO functionality, device is enabled or disabled with V_I.	B
			C
CSP2	20	Normal operation.	D
CSN2	21	Loss of current sense signal. Circuit possibly unstable.	B
RT	22	Possible device damage. Exceeds absolute maximum voltage rating.	A
SYNCOUT	23	Possible device damage. Exceeds absolute maximum voltage rating.	A
SYNCIN	24	Possible device damage. Exceeds absolute maximum voltage rating.	A
CFG2	25	Possible device damage. Exceeds absolute maximum voltage rating.	A
CFG1	26	Possible device damage. Exceeds absolute maximum voltage rating.	A
CFG0	27	Possible device damage. Exceeds absolute maximum voltage rating.	A
PGOOD	28	Possible device damage. Exceeds absolute maximum voltage rating.	A
MODE	29	Possible device damage. Exceeds absolute maximum voltage rating.	A
EN2	30	Possible device damage. Exceeds absolute maximum voltage rating.	A
ILIM/IMON	31	Possible device damage. Exceeds absolute maximum voltage rating.	A
ATRK/DTRK	32	Possible device damage. Exceeds absolute maximum voltage rating.	A

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2024	*	Initial Release

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265