Functional Safety Information

TSD5402-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for TSD5402-Q1 (16-pin PWP package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

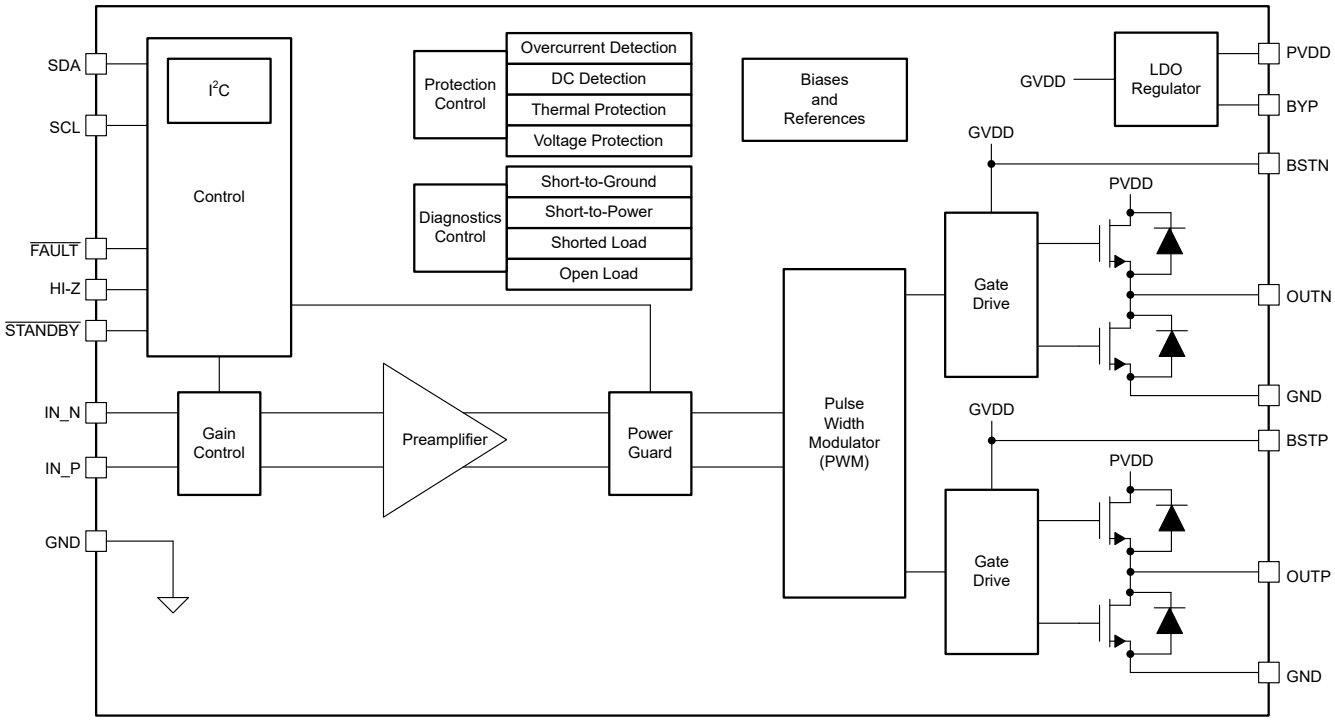

Figure 1-1. Functional Block Diagram

TSD5402-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for TSD5402-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	13
Die FIT rate	4
Package FIT rate	9

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 425mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS/BICMOS ASICs Analog and Mixed =<50V supply	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TSD5402-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Safe failure modes	50
Unsafe failure modes	50

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TSD5402-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (PVDD) (see Table 4-5)

Table 4-2 through Table 4-5 indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the TSD5402-Q1 pin diagram. For a detailed description of the device pins, refer to the *Pin Configuration and Functions* section in the TSD5402-Q1 data sheet.

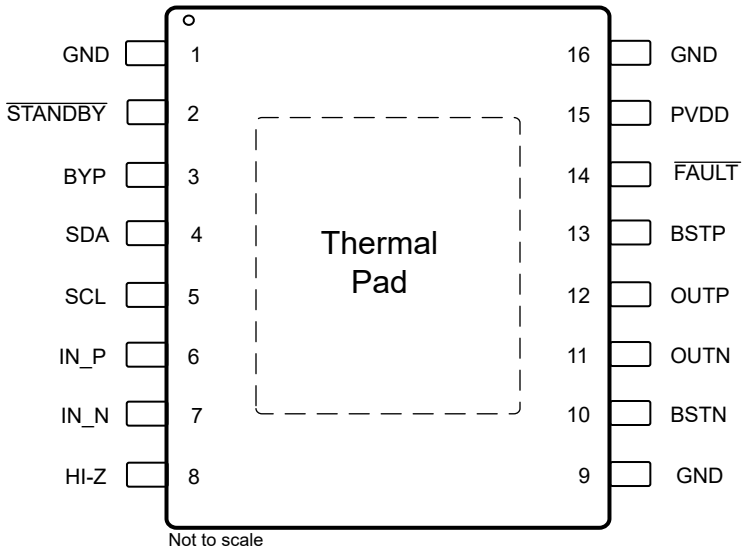

Figure 4-1. TSD5402-Q1 Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- T_C = 25 °C
- PVDD = 4.5V - 18V
- R_L = 4Ω
- P_{OUT} = 1W
- AES17 Filter, Default I^2C settings
- Output channel in DRIVE mode

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
GND	1	No effects.	D
/STANDBY	2	Device is in standby mode.	B
BYP	3	LDO trigger current limit protection, if under continuous stress, can heat up.	B

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
SDA	4	I^2C interface does not work.	B
SCL	5	I^2C interface does not work.	B
IN_P	6	Device not able to deliver power.	B
IN_N	7	Device not able to deliver power.	B
HI-Z	8	No effects.	D
GND	9	No effects.	D
BSTN	10	Output cannot be driven to logic-1 (PVDD). Can trigger overcurrent protection.	B
OUTN	11	Output overcurrent protection. Device shutdown. Fault latches.	B
OUTP	12	Output overcurrent protection. Device shutdown. Fault latches.	B
BSTP	13	Output cannot be driven to logic-1 (PVDD). Can trigger overcurrent protection.	B
/FAULT	14	FAULT cannot assert correctly, can affect the system MCU.	B
PVDD	15	No damage to device considering power and ground are at same potential.	B
GND	16	No effects.	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
GND	1	If all GNDs are disconnected, device damage is possible. If only one GND is disconnected, the device is functional but performance can degrade.	A
/STANDBY	2	Internal pull-down resistor is standby the device.	B
BYP	3	Driver potentially does not work correctly and can trigger overcurrent protection.	B
SDA	4	Device does not respond to I^2C command.	B
SCL	5	Device does not respond to I^2C command.	B
IN_P	6	Device is not able to deliver power.	B
IN_N	7	Device is not able to deliver power.	B
HI-Z	8	Device can be in Hi-z state.	B
GND	9	If all GNDs are disconnected, device damage is possible. If only one GND is not connected, device is functional but performance can degrade.	A
BSTN	10	Output cannot be driven to logic-1 (PVDD).	B
OUTN	11	Open-load condition.	C
OUTP	12	Open-load condition.	C
BSTP	13	Output cannot be driven to logic-1 (PVDD).	B
/FAULT	14	FAULTZ cannot be reported to the system.	B
PVDD	15	Device does not start up.	B
GND	16	If all GNDs are disconnected, device damage is possible. If only one GND is disconnected, device is functional but performance can degrade.	A

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
GND	1	2	Device is in standby mode.	B
/STANDBY	2	3	Device is in standby mode.	B
BYP	3	4	LDO trigger current limit protection, if under continuous stress, can heat up.	B
SDA	4	5	Device does not respond to I^2C command.	B
SCL	5	6	Device does not respond to I^2C command.	B
IN_P	6	7	Amplifier gain is not correct.	

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
IN_N	7	8	Amplifier gain is not correct.	B
HI-Z	8	9	Device can be in Hi-z state.	B
GND	9	10	Signal performance degradation.	C
BSTN	10	11	Output cannot be driven to logic-1 (PVDD). Can trigger overcurrent protection.	B
OUTN	11	12	Report overcurrent fault.	B
OUTP	12	13	Report overcurrent fault.	B
BSTP	13	14	Output cannot be driven to logic-1 (PVDD). Can trigger overcurrent protection.	B
/FAULT	14	15	FAULT cannot assert correctly, can affect system MCU.	B
PVDD	15	16	Device does not start up.	B
GND	16	15	Device does not start up.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to PVDD

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
GND	1	System-level fault. Power short to ground.	B
/STANDBY	2	Device damage is possible.	A
BYP	3	Device damage is possible.	A
SDA	4	Device damage is possible.	A
SCL	5	Device damage is possible.	A
IN_P	6	Device damage is possible.	A
IN_N	7	Device damage is possible.	A
HI-Z	8	Device damage is possible.	A
GND	9	System-level fault. Power short to ground.	B
BSTN	10	Device damage is possible.	A
OUTN	11	Output S2P event, protected if short after filter.	B
OUTP	12	Output S2P event, protected if short after filter.	B
BSTP	13	Device damage is possible.	A
/FAULT	14	FAULT cannot assert correctly and can affect system MCU.	B
PVDD	15	No effect.	D
GND	16	System-level fault. Power short to ground.	B

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