Functional Safety Information

TMP411-Q1
Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

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1 Overview

This document contains information for TMP411-Q1 (SOT563-6 package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

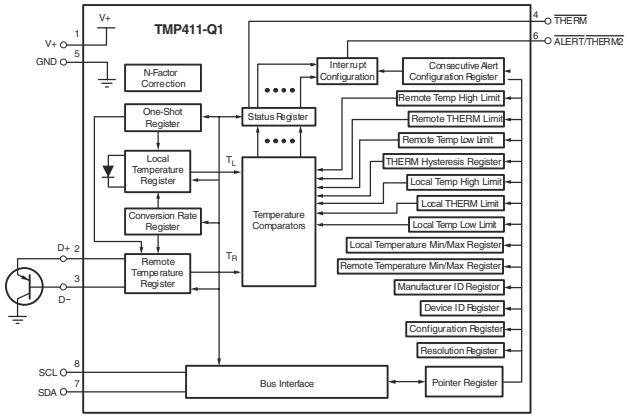

Figure 1-1. Functional Block Diagram

TMP411-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for TMP411-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	6
Die FIT rate	2
Package FIT rate	4

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 1.0mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	60 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TMP411-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Local temperature conversion error	20
Remote temperature conversion error	10
Serial communication error	10
ADC offset out of specification	10
ADC gain out of specification	10
ADC conversion output code bit error	20
ADC incorrect input channel selected	5
Register bank data bit error	10
ALERT/THERM2 or THERM false trip, fails to trip	5

The FMD in Table 3-1 excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to IEC 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TMP411-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the TMP411-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TMP411-Q1 data sheet.

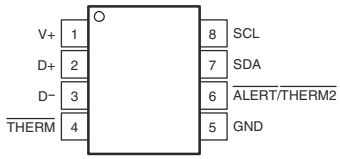

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Device is the only target on the I2C bus
- External pull-up resistor on SCL and SDA pins

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
V+	1	The device is not powered. The device is not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise, device damage is plausible.	A
D+	2	The positive remote connection is stuck low. The remote temperature measurement is out of specification.	B
D-	3	No effect. Normal operation.	D
THERM	4	THERM is stuck low. Not functional. A false thermal limit triggers.	B
GND	5	No effect. Normal operation.	D
ALERT/THERM2	6	ALERT/THERM2 is stuck low. Not functional. A false thermal limit triggers.	B
SDA	7	SDA is stuck low. I2C communication with the device is not possible.	B
SCL	8	SCL is stuck low. I2C communication with the device is not possible.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
V+	1	The functionality of the device is undetermined. The device is not powered if all external analog and digital pins are held low. If voltages are present on any of the analog or digital pins above the power-on reset threshold for the device, the device can potentially power up through internal ESD diodes to V+.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
D+	2	The positive remote connection is undetermined. The remote temperature measurement is out of specification.	B
D-	3	The reference of remote connection is undetermined. The remote temperature measurement is out of specification.	B
THERM	4	The state of THERM is undetermined. A false thermal limit can trigger.	B
GND	5	The functionality of the device is undetermined. The device can be not powered or connected to ground internally through an alternate pin ESD diode and powered up.	B
ALERT/THERM2	6	The state of ALERT/THERM2 is undetermined. A false thermal limit can trigger.	B
SDA	7	The state of SDA is undetermined. I2C communication with the device is not possible.	B
SCL	8	The state of SCL is undetermined. I2C communication with the device is not possible.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
V+	1	D+	The positive remote connection is stuck high. The remote temperature measurement is out of specification.	B
D+	2	D-	The positive remote connection and the reference of remote connection is shorted. The remote temperature measurement is out of specification.	B
D-	3	THERM	The reference of remote connection is stuck high or low. The remote temperature measurement is out of specification.	B
GND	4	ALERT/THERM2	ALERT is stuck low. Not functional. A false thermal limit triggers.	B
ALERT/THERM2	5	SDA	The SDA communication line is stuck high or low. I2C communication with the device is not possible.	B
SDA	6	SCL	The communication lines are shorted. I2C communication with the device is not possible.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
V+	1	No effect. Normal operation.	D
D+	2	The positive remote connection is stuck high. The remote temperature measurement is out of specification.	B
D-	3	The reference of remote connection is stuck high. The remote temperature measurement is out of specification.	B
THERM	4	THERM is stuck high. Not functional. The thermal limit does not trigger.	B
GND	5	The device functionality is undetermined. Observe that the absolute maximum ratings for all pins of the device are met, otherwise, device damage is plausible.	A
ALERT/THERM2	6	ALERT/THERM2 is stuck high. Not functional. The thermal limit does not trigger.	B
SDA	7	SDA is stuck high. I2C communication with the device is not possible.	B
SCL	8	SCL is stuck high. I2C communication with the device is not possible.	B

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
February 2025	*	Initial Release

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