Functional Safety Information

TPS6291x-Q1 Functional Safety FIT Rate and Pin FMA

Table of Contents

1 Overview....2
2 Functional Safety Failure In Time (FIT) Rates....3
3 Pin Failure Mode Analysis (Pin FMA)....4

Trademarks

All trademarks are the property of their respective owners.

1 Overview

This document contains information for the TPS6291x-Q1 (VQFN-HR package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

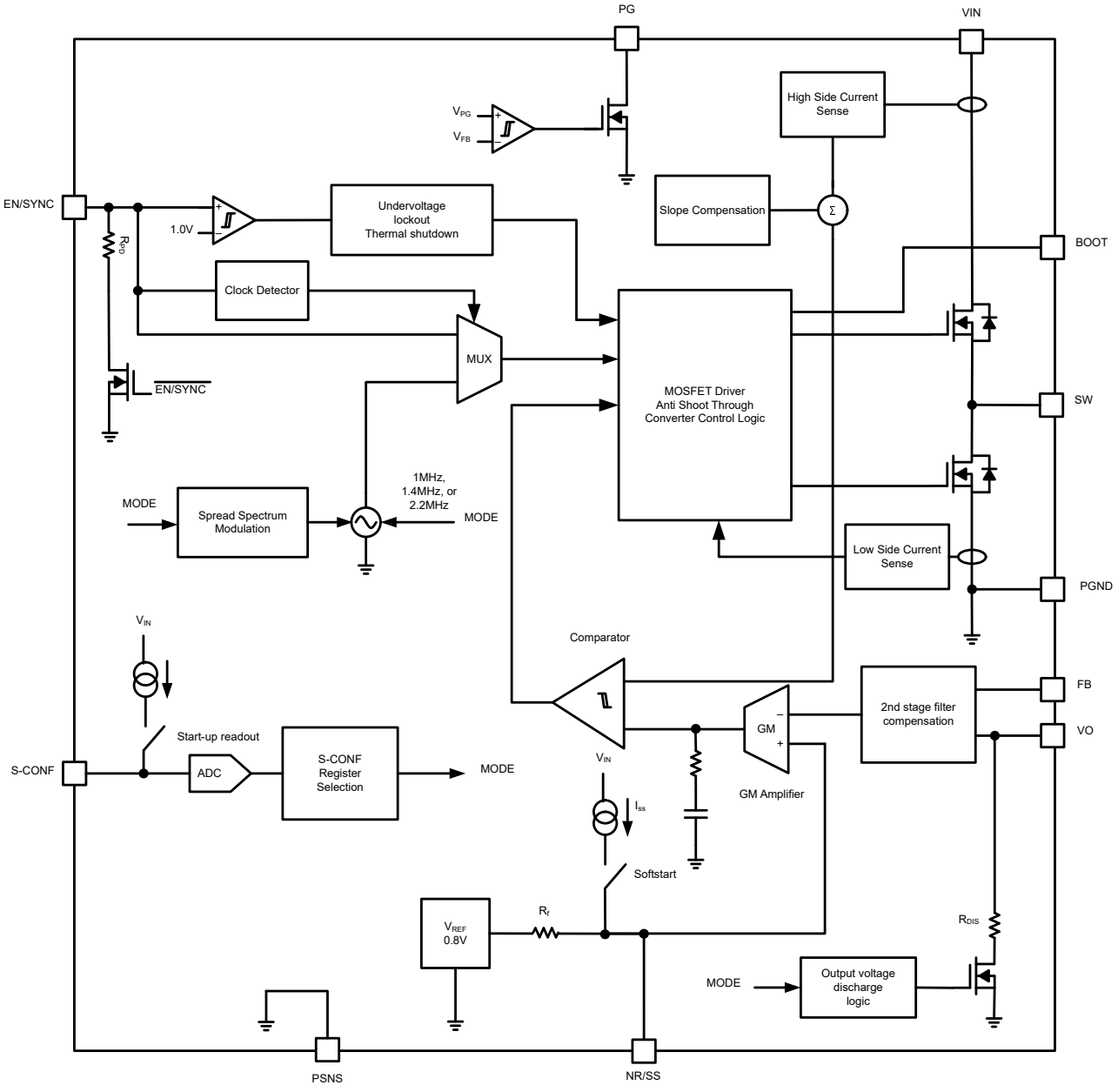

Figure 1-1. Functional Block Diagram

The TPS6291x-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

ADVANCE INFORMATION for preproduction products; subject to change without notice.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the TPS6291x-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)		
Power Dissipation	**0.5W**	**1.0W**	**1.5W**
Total component FIT rate	12	26	59
Die FIT rate	8	22	55
Package FIT rate	4	4	4

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Automotive control
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2T

Table	Category	Reference FIT Rate	Reference Virtual T_j
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_j (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS6291x-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 3-2)
- Pin open-circuited (see Table 3-3)
- Pin short-circuited to an adjacent pin (see Table 3-4)
- Pin short-circuited to VIN (see Table 3-5)

Table 3-2 through Table 3-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 3-1.

Table 3-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 3-1 shows the TPS6291x-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TPS6291x-Q1 data sheet.

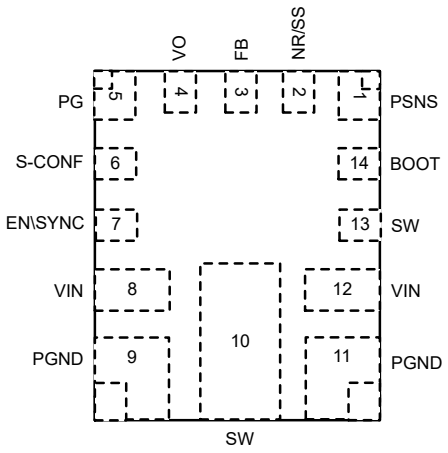

Figure 3-1. Pin Diagram

Following is the assumption of use and the device configuration assumed for the pin FMA in this section:

- The device is operating in one of the typical application configurations show in Figure 3-2.

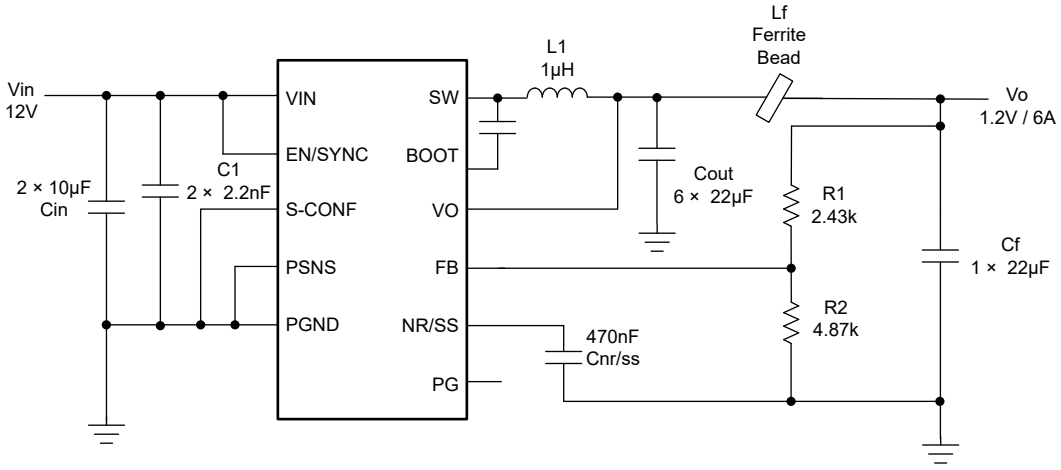

Figure 3-2. Typical Schematic

Table 3-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
PSNS	1	Intended pin connection.	D
NR/SS	2	The device does not power on.	B
FB	3	Loss of output voltage regulation. Output voltage goes to V_{in}. Device damage is possible.(1) Absolute maximum voltage can be exceeded.	A
VO	4	Loss of output voltage.	B
PG	5	Loss of PG functionality.	C
S-CONF	6	The device runs at 1MHz f_{SW}, spread spectrum off, output discharge off, sync disabled.(2)	C (2)
EN/SYNC	7	The device does not power on for both EN and SYNC functions.	B
VIN	8, 12	The device does not power on.	B
PGND	9, 11	Intended pin connection.	D
SW	10, 13	Device damage is possible.	A
BOOT	14	Device damage is possible.	A

Table 3-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
PSNS	1	Device damage is possible.	A
NR/SS	2	Allowable pin condition. Soft-start time is minimized. Minimum noise filtering.	D
FB	3	Loss of output voltage regulation. Output voltage goes to V_{in}. Device damage is possible.(1) Absolute maximum voltage can be exceeded.	A
VO	4	Open loop operation. Undetermined output voltage behavior.	B
PG	5	Loss of PG functionality.	C
S-CONF	6	The device runs at 2.2Mhz f_{SW}, spread spectrum random, output discharge on, sync disabled.(2)	C
EN/SYNC	7	The device does not power on for both EN and SYNC functions.	B
VIN	8, 12	The device does not power on.	B
PGND	9, 11	Device damage is possible.	A
SW	10, 13	Loss of output voltage regulation.	B
BOOT	14	Loss of output voltage regulation.	B

Table 3-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
PSNS	1	NR/SS	The device does not power on.	B
NR/SS	2	FB	Loss of output voltage regulation.	B
FB	3	VO	Loss of output voltage regulation.	B
VO	4	PG	Loss of output voltage regulation. Device damage is possible.(1) Absolute maximum voltage can be exceeded if PG is connected to VIN through a resistor.	A
PG	5	S-CONF	The device operating mode is indeterminate. (2)	C (2)
S-CONF	6	EN/SYNC	The device operating mode is indeterminate. (2)	C (2)
EN/SYNC	7	VIN	The device cannot be disabled. If using SYNC functionality, loss of output voltage regulation occurs.	B
VIN	8	PGND	Device damage is possible.	A
PGND	9	SW	Device damage is possible.	A
SW	10	PGND	Device damage is possible.	A
PGND	11	VIN	Device damage is possible.	A
VIN	12	SW	Device damage is possible.	A
SW	13	BOOT	Device damage is possible.	A
BOOT	14	PSNS	Device damage is possible.	A

Table 3-5. Pin FMA for Device Pins Short-Circuited to VIN

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
PSNS	1	Device damage is possible.	A
NR/SS	2	Device damage is possible.(1) Absolute maximum voltage can be exceeded.	A
FB	3	Loss of output voltage regulation. Output voltage goes to V_{in}. Device damage is possible.(1) Absolute maximum voltage can be exceeded.	A
VO	4	Device damage is possible.(1) Absolute maximum voltage can be exceeded.	A
PG	5	Device damage is possible. Absolute maximum current rating for the pin can be exceeded.	A
S-CONF	6	The device runs at 2.2MHz f_{SW}, spread spectrum off, output discharge off, sync disabled.(2)	D (2)
EN/SYNC	7	The device cannot be disabled. If using SYNC functionality, loss of output voltage regulation occurs.	B
VIN	8, 12	Intended pin connection.	D
PGND	9, 11	Device damage is possible.	A
SW	10, 13	Device damage is possible.	A
BOOT	14	Device damage is possible.	A

(1) Damage occurs if V_{IN} is greater than the 6V absolute maximum rating for the pin.
(2) Assumes pin FMA condition occurs prior to device being enabled. If Pin FMA condition occurs after the device is operating, the device continues operating as previously configured.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265