Functional Safety Information

TLC3555-Q1
Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

Trademarks

1 Overview

This document contains information for the TLC3555-Q1 (SOIC DDF package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

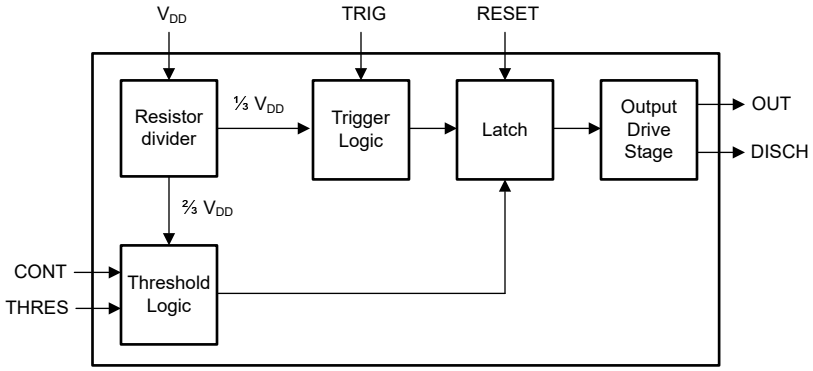

Figure 1-1. Functional Block Diagram

The TLC3555-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates - SOIC

2.1 Functional Safety Failure in Time (FIT) Rates For the TLC3555-Q1

This section provides functional safety failure in time (FIT) rates for the TLC3555-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	10
Die FIT rate	3
Package FIT rate	7

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 6.48mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TLC3555-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Output open (Hi-Z)	20
Output saturated high	25
Output saturated low	25
Output functional, not in specification voltage or timing	30

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TLC3555-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the TLC3555-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TLC3555-Q1 data sheet.

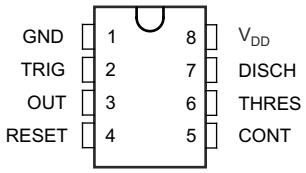

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- *Short circuit to Power* means short to V_{DD}
- *Short circuit to GND or Ground* means short to GND

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
TRIG	2	Depending on the circuit configuration, the application is not likely to function because of unexpected output behavior. If RESET is high, the output is forced high and the discharge transistor is turned off. Depending on the circuit configuration, the application is not likely to function as expected due to the fixed output behavior.	B
OUT	3	Depending on the circuit configuration, the device is likely forced into a short-circuit condition with the OUT voltage ultimately forced to the GND voltage. Prolonged exposure to short-circuit conditions can result in long-term reliability issues.	A
RESET	4	The device is forced into the *reset* state, with the output forced low and the discharge transistor turned on. Depending on the circuit configuration, the application is not likely to function as expected due to the fixed output behavior.	B
CONT	5	Depending on the circuit configuration, the application is not likely to function because of unexpected output behavior and spiked current dissipated though the device.	B
DISCH	6	Depending on the circuit configuration, the application is not likely to function because of an inability to discharge the timing capacitors.	B
THRES	7	Depending on the circuit configuration, the application is not likely to function because of unexpected output behavior.	B
V_{DD}	8	Timer supplies are shorted together leaving the V_{DD} pin at some voltage between the V_{DD} and GND sources (depending on the source impedance).	A

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
GND	1	Negative supply is left floating. The timer ceases to function because no current can source or sink to the device. There is a potential for damage if any input pins are biased.	A
TRIG	2	Depending on the circuit configuration, the application is not likely to function because of unexpected output behavior.	B
OUT	3	No negative feedback or ability for OUT to drive the application.	B
RESET	4	Leaving the RESET pin floating can effect application performance. The weak 1MΩ internal pull-up resistor to the positive supply holds the RESET pin high under most conditions, but can be momentarily overpowered in an electrically noisy environment, possibly causing irregular toggling of the output.	C
CONT	5	Depending on the circuit configuration, the application is not likely to function because of unexpected output behavior.	B
DISCH	6	Depending on the circuit configuration, the application is not likely to function because of an inability to discharge the timing capacitors.	B
THRES	7	Depending on the circuit configuration, the application is not likely to function because of unexpected output behavior.	B
V_{DD}	8	Positive supply is left floating. The timer ceases to function because no current can source or sink to the device. There is a potential for damage if any input pins are biased.	A

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
GND	1	2	Depending on the circuit configuration, the application is not likely to function because of unexpected output behavior.	B
TRIG	2	3	Depending on the circuit configuration, the application is not likely to function because of unexpected output behavior.	B
OUT	3	4	Depending on the circuit configuration, the application is not likely to function because of unexpected output behavior.	B
RESET	4	5	If the CONT pin is driven externally by a low-impedance source, the RESET pin is pulled to the voltage of the CONT source. If the CONT pin is floating, the RESET pin is pulled to 0.67% of V_{DD}. The resulting value at the RESET pin either forces the device into the *reset* state, prevents the device from going into the *reset* state, or possibly causes the *reset* state to toggle, depending on the exact value. The application is not likely to function properly because of unpredictable behavior.	B
CONT	5	6	Depending on the circuit configuration, the application is not likely to function because of unexpected output behavior.	B
DISCH	6	7	Depending on the circuit configuration, the application is not likely to function because of unexpected output behavior.	B
THRES	7	8	Depending on the circuit configuration, the application is not likely to function because of unexpected output behavior.	B
V_{DD}	8	1	Timer supplies are shorted together, leaving the V_{DD} pin at some voltage between the GND and V_{DD} sources (depending on the source impedance).	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
GND	1	Timer supplies are shorted together, leaving the GND pin at some voltage between the GND and V_{DD} sources (depending on the source impedance).	A
TRIG	2	Depending on the circuit configuration, the application is not likely to function because of unexpected output behavior.	B
OUT	3	Depending on the circuit configuration, the device is likely forced into a short-circuit condition with the OUT voltage ultimately forced to the V_{DD} voltage. Prolonged exposure to short-circuit conditions can result in long-term reliability issues.	A
RESET	4	The device is unable to enter the *reset* state. If the application configuration requires the *reset* state to be asserted, the application does not function as expected.	B
CONT	5	Depending on the circuit configuration, the application is likely not to function due to unexpected output behavior.	B
DISCH	6	Depending on the circuit configuration, the application is not likely to function because of an inability to discharge the timing capacitors. Potential for damage is high because of large currents flowing through the discharge transistor.	A
THRES	7	Depending on the circuit configuration, the application is not likely to function because of unexpected output behavior.	B

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265