*Functional Safety Information*

# *ISOTMP35-Q1 Functional Safety FIT Rate, FMD and Pin FMA*

## Table of Contents



## Trademarks

# 1 Overview

This document contains information for the ISOTMP35-Q1 (DFQ package) to aid in functional safety system designs. This document discusses:

- Functional safety failure In time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards in combination with expert judgement
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

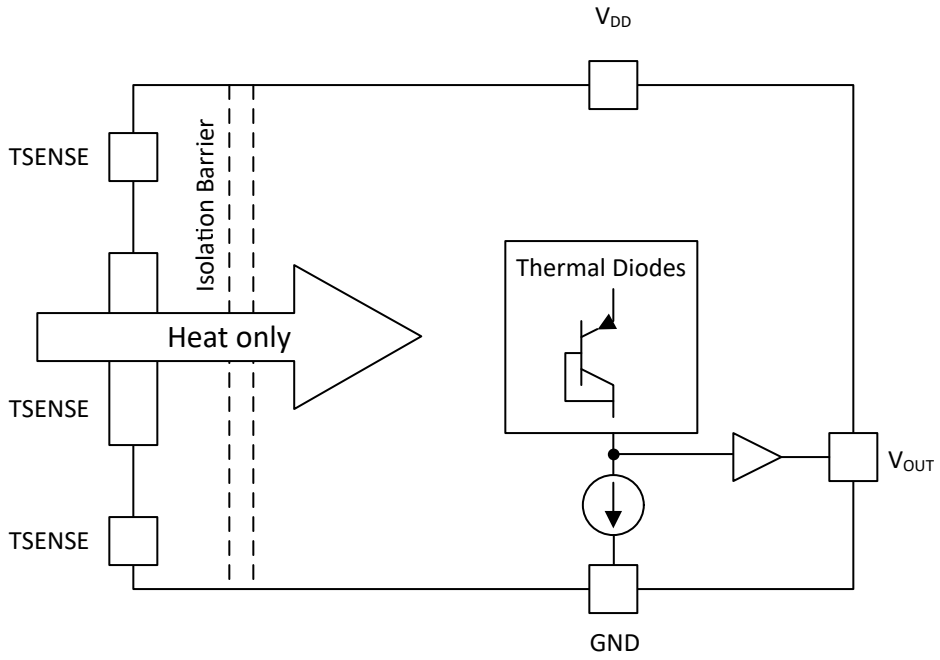


**Figure 1-1. Functional Block Diagram**

The ISOTMP35-Q1 was developed using a quality-managed development process, but was not developed in accordance with the ISO 26262 standards.

## 2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for ISOTMP35-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

**Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11**

| FIT IEC TR 62380 / ISO 26262 | FIT (Per $10^9$ Hours) |
|---|---|
| Total Component FIT Rate | 8 |
| Die FIT Rate | 2 |
| Package FIT Rate | 6 |

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from Table 11
- Power dissipation: 2 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

**Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2**

| Table | Category | Reference FIT Rate | Reference Virtual $T_J$ |
|---|---|---|---|
| 5 | CMOS/BICMOS ASICs Analog & Mixed ≤ 50V supply | 25 | 55 |

The reference FIT rate and reference virtual TJ (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

# 3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for ISOTMP35-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

**Table 3-1. Die Failure Modes and Distribution**

| Die Failure Modes | Failure Mode Distribution (%) |
|---|---|
| VOUT open (HIZ) | 20% |
| VOUT short to VDD | 10% |
| VOUT short to GND | 10% |
| VOUT not in specification | 60% |

The FMD in Table 3-1 excludes short-circuit faults across the isolation barrier. Faults for short circuits across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a safety-separated extra low voltage (SELV) or protective extra low voltage (PELV) power supply is used, pollution degree 2 / OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

# 4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the ISOTMP35-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

**Table 4-1. TI Classification of Failure Effects**

| Class | Failure Effects |
|---|---|
| A | Potential device damage that affects functionality. |
| B | No device damage, but loss of functionality. |
| C | No device damage, but performance degradation. |
| D | No device damage, no impact to functionality or performance. |

Figure 4-1 shows the DFQ package pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the ISOTMP35-Q1 data sheet.

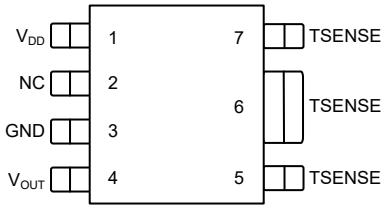


**Figure 4-1. Pin Diagram**

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Bypass capacitor on the input voltage pin of 0.01µF.
- Series resistors are sized to limit the input currents to the analog inputs to < 5mA.
- Capacitive loading on output pin is limited to 1100pF.

**Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground**

| Pin Name | Pin No. | Description of Potential Failure Effects | Failure Effect Class |
|---|---|---|---|
| VDD | 1 | Device unpowered. Device not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage is plausible. | A |
| NC | 2 | No effect. Normal operation. | D |
| GND | 3 | No effect. Normal operation. | D |
| VOUT | 4 | Output stuck low. No analog output present on device. | B |
| TSENSE | 5 | No effect. Normal operation. | D |
| TSENSE | 6 | No effect. Normal operation. | D |
| TSENSE | 7 | No effect. Normal operation. | D |

**Table 4-3. Pin FMA for Device Pins Open-Circuited**

| Pin Name | Pin No. | Description of Potential Failure Effects | Failure Effect Class |
|---|---|---|---|
| VDD | 1 | Device functionality undetermined. | B |

**Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)**

| Pin Name | Pin No. | Description of Potential Failure Effects | Failure Effect Class |
|---|---|---|---|
| NC | 2 | No effect. Normal operation. | D |
| GND | 3 | Device functionality undetermined. Device is unpowered or connect to ground internally through alternate pin ESD diode and power up. | B |
| VOUT | 4 | No effect. Normal operation. | D |
| TSENSE | 5 | No effect. Normal operation. | D |
| TSENSE | 6 | No effect. Normal operation. | D |
| TSENSE | 7 | No effect. Normal operation. | D |

**Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin**

| Pin Name | Pin No. | Shorted to | Description of Potential Failure Effects | Failure Effect Class |
|---|---|---|---|---|
| VDD | 1 | NC | No effect. Normal operation. | D |
| NC | 2 | GND | No effect. Normal operation. | D |
| GND | 3 | VOUT | Output stuck low. No analog output present on device. | B |
| TSENSE | 5 | TSENSE | No effect. Normal operation. | D |
| TSENSE | 6 | TSENSE | No effect. Normal operation. | D |

**Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply**

| Pin Name | Pin No. | Description of Potential Failure Effects | Failure Effect Class |
|---|---|---|---|
| VDD | 1 | No effect. Normal operation. | D |
| NC | 2 | No effect. Normal operation. | D |
| GND | 3 | Device functionality undetermined. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage is plausible. | A |
| VOUT | 4 | Output stuck high. | B |
| TSENSE | 5 | No effect. Normal operation. | D |
| TSENSE | 6 | No effect. Normal operation. | D |
| TSENSE | 7 | No effect. Normal operation. | D |

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265