Functional Safety Information

UCC273x1A-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for the UCC273x1A-Q1 (SOIC and VSON packages) to aid in a functional safety system design. Only the VSON package product supports EN function. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

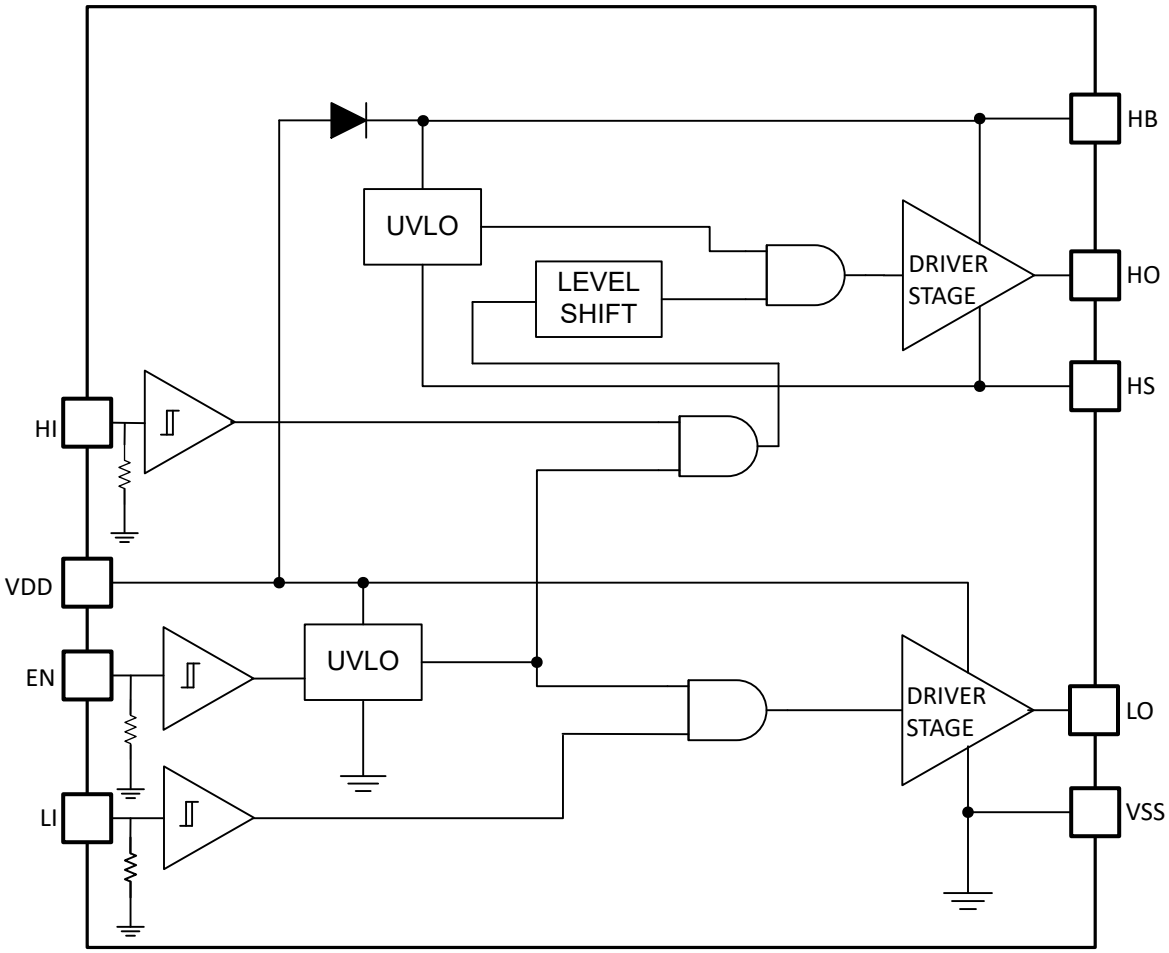

Figure 1-1. Functional Block Diagram of UCC27301A-Q1

Only the VSON package product supports EN function.

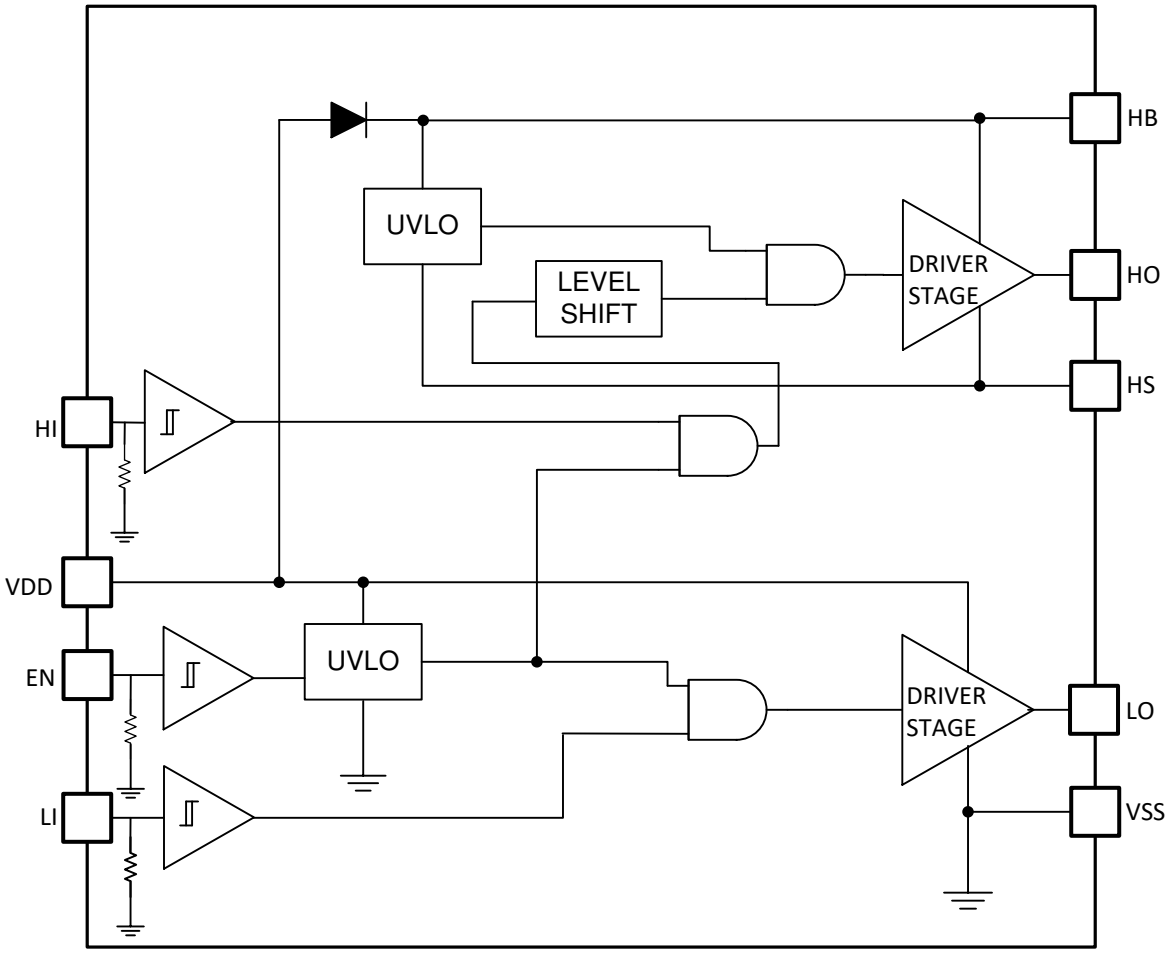

Figure 1-2. Functional Block Diagram of UCC27311A-Q1

The UCC273x1A-Q1 were developed using a quality-managed development process, but were not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 SOIC Package

This section provides functional safety failure in time (FIT) rates for the SOIC package of the UCC273x1A-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. UCC27301A-Q1 Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	Power Dissipation (mW)	FIT (Failures Per 10^9 Hours)
Total component FIT rate	10	10
	400	11
Die FIT rate	10	3
	400	4
Package FIT rate	10	7
	400	7

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 10 mW, 400 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. UCC27301A-Q1 Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	20 FIT	55 °C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 VSON Package

This section provides functional safety failure in time (FIT) rates for the VSON package of the UCC273x1A-Q1 based on two different industry-wide used reliability standards:

- Table 2-3 and Table 2-4 provide FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-5 and Table 2-6 provide FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. UCC27301A-Q1 Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	7
	9
Die FIT rate	3
	5
Package FIT rate	4
	4

The failure rate and mission profile information in Table 2-3 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 10 mW, 400 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. UCC27311A-Q1 Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	Power Dissipation (mW)	FIT (Failures Per 10^9 Hours)
Total component FIT rate	10	7
	400	9
Die FIT rate	10	3
	400	5
Package FIT rate	10	4
	400	4

The failure rate and mission profile information in Table 2-4 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 10 mW, 400 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-5. UCC27301A-Q1 Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	20 FIT	55 °C

Table 2-6. UCC27311A-Q1 Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	20 FIT	55 °C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-5 and Table 2-6 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the UCC273x1A-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. UCC27301A-Q1 VSON Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
HS stuck high	16.5
LO stuck high	16.5
HS stuck low	16.5
LO stuck low	16.5
HS unknown or outside of specified range	16.5
LS unknown or outside of specified range	16.5
UVLO not functional	<1
EN not functional	<1
Others	<1

Table 3-2. UCC27311A-Q1 VSON Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
HS stuck high	16.5
LO stuck high	16.5
HS stuck low	16.5
LO stuck low	16.5
HS unknown or outside of specified range	16.5
LS unknown or outside of specified range	16.5
UVLO not functional	<1
EN not functional	<1
Others	<1

Table 3-3. UCC27301A-Q1 SOIC Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
HS stuck high	16.5
LO stuck high	16.5
HS stuck low	16.5
LO stuck low	16.5
HS unknown or outside of specified range	16.5
LS unknown or outside of specified range	16.5
UVLO not functional	<1
Others	<1

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the UCC273x1A-Q1 (SOIC and VSON packages). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2 and Table 4-6.)
- Pin open-circuited (see Table 4-3 and Table 4-7)
- Pin short-circuited to an adjacent pin (see Table 4-4 and Table 4-8)
- Pin short-circuited to supply (see Table 4-5 and Table 4-9)

Table 4-2 through Table 4-9 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The device operates within the conditions specified in the data sheet.
- For SOIC, the following failure assumptions apply:
  - Short between pin one and pin eight is out of scope.
  - Short between pin four and pin five is out of scope.
  - Short to supply for HI and LI assumes a short to 5V supply.
  - Short to supply for others pins assumes a short to VDD.
- For VSON, the following assumptions apply:
  - Short between pin one and pin ten is out of scope.
  - Short between pin five and pin six is out of scope.
  - Short to supply for HI, LI, and EN assumes a short to 5V supply.
  - Short to supply for others pins assumes a short to VDD.

4.1 SOIC Package

Figure 4-1 shows the UCC27311A-Q1 pin diagram for the SOIC package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the UCC27311A-Q1 data sheet.

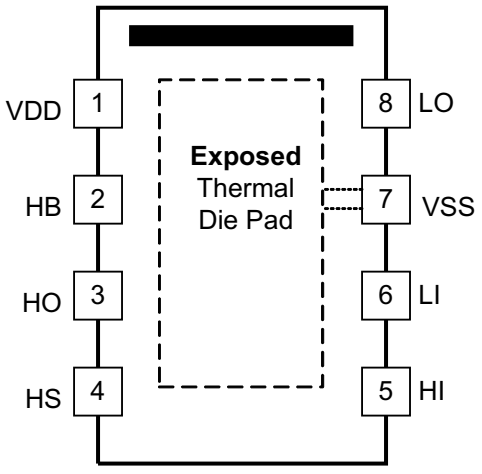

Figure 4-1. Pin Diagram (SOIC) Package

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VDD	1	No power is applied to the device. HO and LO are in a low state.	B
HB	2	HO and LO are in unknown state.	A
HO	3	HO and LO are in unknown state.	A
HS	4	HO and LO are in unknown state.	A
HI	5	HO is in a low state.	B
LI	6	LO is in a low state.	B
VSS	7	No impact.	D
LO	8	HO and LO are in unknown state.	A

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VDD	1	No power is applied to the device. HO and LO are in a low state.	B
HB	2	HO is pulled to HS potential.	B
HO	3	HO is disconnected from the system.	B
HS	4	HO is pulled to HB potential.	B
HI	5	HO is in a low state.	B
LI	6	LO is in a low state.	B
VSS	7	HO is in a low state. LO is pulled to VDD.	B
LO	8	HO is disconnected from the system.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
VDD	1	HB	HO and LO are in unknown state.	A
HB	2	HO	HO is in unknown state.	A
HO	3	HS	HO is in unknown state.	A
HS	4	N/A	N/A	D
HI	5	LI	LO and HO follows the logic truth table per the data sheet. The input states depends on the system.	B
LI	6	VSS	LO is in a low state.	B
VSS	7	LO	LO is in unknown state.	A
LO	8	N/A	N/A	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VDD	1	N/A	D
HB	2	HO and LO are in unknown state.	A
HO	3	HO and LO are in unknown state.	A
HS	4	HO and LO are in unknown state.	A
HI	5	HO and LO follow the logic truth table per the data sheet with LI stuck in a high state.	B
LI	6	HO and LO follow the logic truth table per the data sheet with LI stuck in a high state.	B
VSS	7	HO is in a low state. LO is pulled to VDD.	B
LO	8	HO and LO are in unknown state.	A

4.2 VSON Package

Figure 4-2 shows the UCC273x1A-Q1 pin diagram for the VSON package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the UCC273x1A-Q1 data sheet.

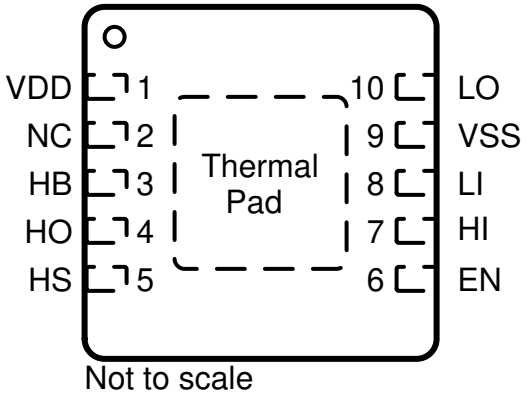

Figure 4-2. Pin Diagram (VSON Package)

Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VDD	1	No power is applied to the device. HO and LO are in a low state.	B
NC	2	No impact.	D
HB	3	HO and LO are in unknown state.	A
HO	4	HO and LO are in unknown state.	A
HS	5	HO and LO are in unknown state.	A
EN	6	HO and LO are in a low state.	B
HI	7	HO is in a low state.	B
LI	8	LO is in a low state.	B
VSS	9	N/A	D
LO	10	HO and LO are in unknown state.	A

Table 4-7. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VDD	1	No power is applied to the device. HO and LO are in a low state.	B
NC	2	No impact.	D
HB	3	HO is pulled to HS potential.	B
HO	4	HO is disconnected from the system.	B
HS	5	HO is pulled to HB potential.	B
EN	6	HO and LO are in a low state.	B
HI	7	HO is in a low state.	B
LI	8	LO is in a low state.	B
VSS	9	HO is in a low state. LO is pulled to VDD.	B
LO	10	LO is disconnected from the system.	B

Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
VDD	1	NC	No impact	D
NC	2	HB	No impact	D
HB	3	HO	HO is in unknown state.	A
HO	4	HS	HO is in unknown state.	A
HS	5	N/A	N/A	D
EN	6	HI	HO and LO follows the logic truth table per the data sheet with EN and HI same potential. The logic states of EN and HI depends on the system.	B
HI	7	LI	HO and LO follows the logic truth table per the data sheet with LI and HI same potential. The logic states of EN and HI depends on the system.	B
LI	8	VSS	LO is in a low state.	B
VSS	9	LO	LO is in unknown state.	A
LO	10	N/A	N/A	D

Table 4-9. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VDD	1	N/A	D
NC	2	N/A	D
HB	3	HO and LO are in unknown state.	A
HO	4	HO and LO are in unknown state.	A
HS	5	HO and LO are in unknown state.	A
EN	6	LO and HO follow the truth table specified in the data sheet with EN stuck in a high state.	B
HI	7	LO and HO follow the truth table specified in the data sheet with HI stuck in a high state.	B
LI	8	LO and HO follow the truth table specified in the data sheet with LI stuck in a high state.	B
VSS	9	Supply short condition. LO and HO states depend on the system. If VSS is pulled to VDD, LO is pulled to VDD and HO is in a low state.	B
LO	10	HO and LO are in unknown state.	A

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