Functional Safety Information

LDC0851 Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for the LDC0851 (WSON package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards

Figure 1-1 shows the device functional block diagram for reference.

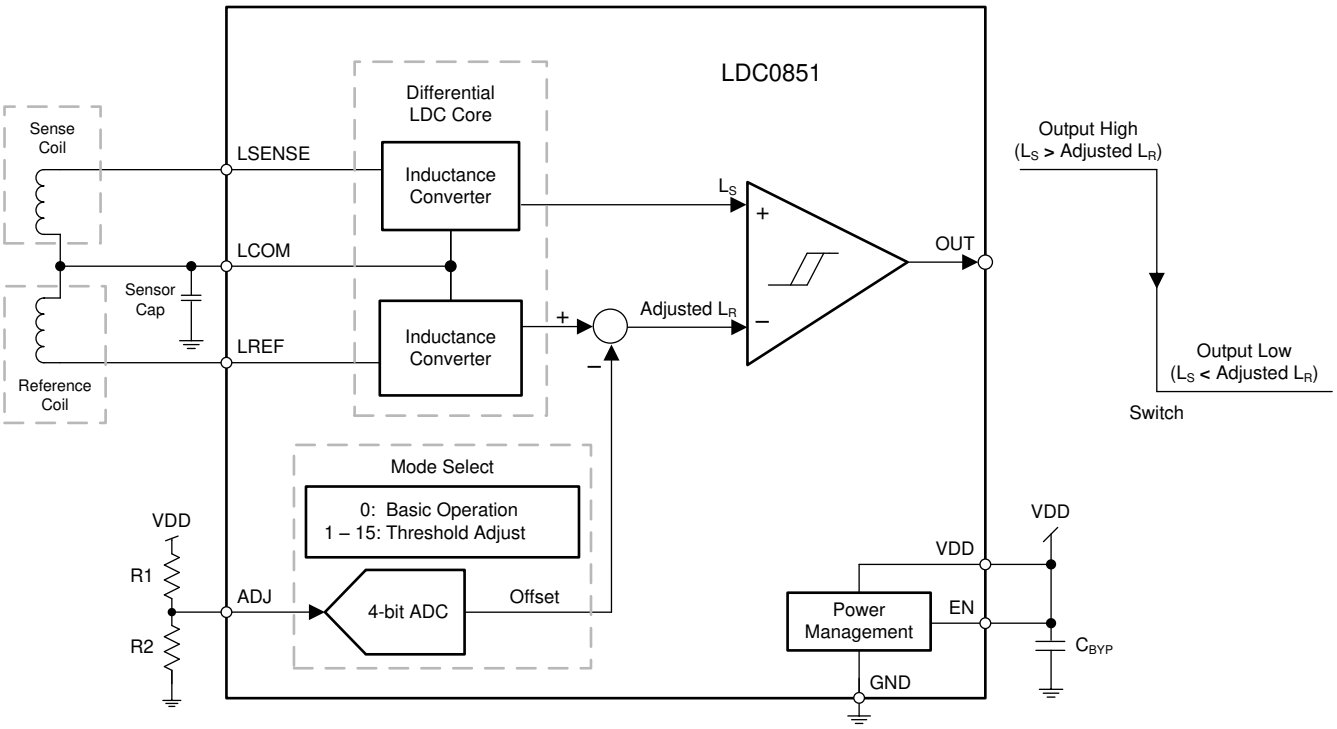

Figure 1-1. Functional Block Diagram

The LDC0851 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the LDC0851 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	4
Die FIT rate	2
Package FIT rate	2

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 40.4 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS/BICMOS ASICS Analog & Mixed ≤50V Supply	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the LDC0851 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Output stuck in HIGH state	35
Output stuck in LOW state	15
Output stuck Hi-Z	5
Switching Distance error (Output switches at incorrect threshold)	45

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the LDC0851. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the LDC0851 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the LDC0851 data sheet.

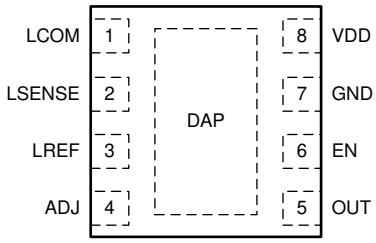

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Application circuit similar to the one found int the LDC0851 data sheet.
- Voltage supply capable of sourcing a lot of current like a battery.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
LCOM	1	LC tank oscillating signal expected to collapse while short present. While oscillator signal not properly functioning, switch not expected to trigger when target is present.	B
LSENSE	2	LC tank oscillating signal expected to collapse while short present. While oscillator signal not properly functioning, switch not expected to trigger when target is present.	B
LREF	3	LC tank oscillating signal expected to collapse while short present. While oscillator signal not properly functioning, switch not expected to trigger when target is present.	B
ADJ	4	Sets improper threshold at startup. Intended threshold not used until short removed and enable toggled.	B or C
OUT	5	Device output pulled low. How low the potential pulled depends on the resistance of the short. For a strong short, switch output behavior completely lost.	B or C
EN	6	Acceptable operating mode, device will remain in shutdown mode. No meaningful measurement data can be collected. Device will output high.	B
GND	7	Normal Operation	D
VDD	8	A lot of current may be sourced external to the device, with the current only being limited by the source that supplies VDD and the resistance of the short. Depending on the layout and where the short is and the duration of the short, the part may heat up and be damaged. Thermal damage expected if the supply can source high current, there is a very low resistance path between the supply and LDC0851 supply pin, and the short is directly at the LDC0851 pins, and the short lasts for an order longer than a few microseconds.	A or B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
LCOM	1	Irregular signals expected between LCOM and LSENSE as well as LCOM and LREF. Proper functionality lost.	B
LSENSE	2	Irregular signal between LSENSE and LCOM expected; device not functioning as intended.	B
LREF	3	Irregular signal between LREF and LCOM expected; device not functioning as intended.	B
ADJ	4	Switching distance unpredictable	C
OUT	5	Device not damaged, equivalent to connecting to a high input impedance. System likely affected, but not device.	D
EN	6	Enable potential undefined; can remain in shutdown mode or active mode. System unable to control device state and adjust target thresholds.	B
GND	7	Not functional and not damaged.	B
VDD	8	Device not properly powered, intended operation not expected.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
LCOM	1	2-LSENSE	LC tank signal collapses while short present. Output low regardless of metal target present or not.	B
LSENSE	2	3-LREF	Inductances in parallel, potentially insufficient inductance. Sense inductance and Ref inductance identical, output should remain whether target present or not.	B
LREF	3	4-ADJ	Sets improper threshold at startup. Intended threshold not used until short removed and enable toggled.	C
ADJ	4	5-OUT	ADJ setting undefined. Device may not trigger for intended range.	C
OUT	5	6-EN	OUT railing low or High depending on the setting for EN, board trace resistance and supply's ability to source current . If EN open circuited, erratic behavior expected.	B
EN	6	7-GND	Acceptable operating mode; device will remain in shutdown mode. No meaningful measurement data can be collected. Device will output high.	B
GND	7	8-VDD	A lot of current may be sourced external to the device, with the current only being limited by the source that supplies VDD and the resistance of the short. Depending on the layout and where the short is and the duration of the short, the part may heat up and be damaged. Thermal damage expected if the supply can source high current, there is a very low resistance path between the supply and LDC0851 supply pin, and the short is directly at the LDC0851 pins, and the short lasts for an order longer than a few microseconds.	A or B
VDD	8	1-LCOM	LC tank oscillating signal expected to collapse while short present. While oscillator signal not properly functioning, switch not expected to trigger when target is present.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
LCOM	1	LC tank oscillating signal expected to collapse while short present. While oscillator signal not properly functioning; switch is not expected to trigger when target is present.	B
LSENSE	2	LC tank oscillating signal expected to collapse while short present. While oscillator signal not properly functioning; switch is not expected to trigger when target is present.	B
LREF	3	LC tank oscillating signal expected to collapse while short present. While oscillator signal not properly functioning; switch is not expected to trigger when target is present.	B
ADJ	4	ADJ voltage potentially exceeding absolute maximum rating if VDD > 2V, short strong, and VDD capable of sourcing a lot of current. If device continues to operate, ADJ will be set to the highest value, switching distance will be maximally reduced. Device may never trigger for intended range.	A or B
OUT	5	When target present ($f_{Sense} > f_{Ref}$, $L_{sense} < L_{ref}$), device expected to sink more current, but not so much as to exceed 5mA.	B
EN	6	Acceptable operating mode. Device will always be enabled. This can be detrimental to device attempting to toggle EN pin, but not to LDC0851. LDC0851 shutdown capability lost; typical system current budget can increase.	B or D
GND	7	A lot of current may be sourced external to the device, with the current only being limited by the source that supplies VDD and the resistance of the short. Depending on the layout and where the short is and the duration of the short, the part can heat up and sustain damage. Thermal damage expected if the supply can source high current, there is a very low resistance path between the supply and LDC0851 supply pin, and the short is directly at the LDC0851 pins, and the short lasts for an order longer than a few microseconds.	B
VDD	8	Normal operation.	D

5 Revision History

Changes from Revision * (February 2024) to Revision A (April 2024)	Page
• Added *Failure Mode Distribution (FMD)* section to document	4
• Added *Pin FMA* section to document	5

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