Functional Safety Information

SN74AXC4T245-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for the SN74AXC4T245-Q1 (TSSOP, WQFN, and UQFN packages) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

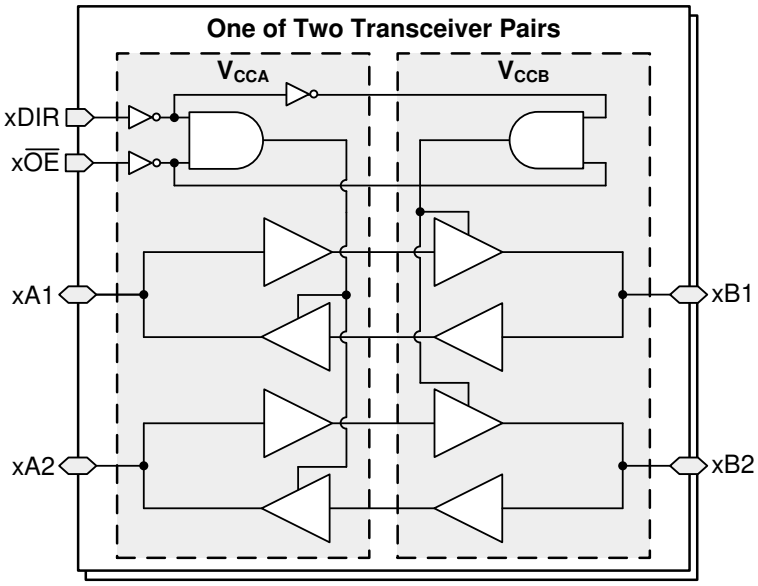

Figure 1-1. Functional Block Diagram

The SN74AXC4T245-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 TSSOP Package

This section provides functional safety failure in time (FIT) rates for the TSSOP package of the SN74AXC4T245-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	15
Die FIT rate	2
Package FIT rate	13

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: motor control from table 11
- Power dissipation: 20 mW
- Climate type: world-wide table 8
- Package factor (lambda 3): table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	5 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 WQFN Package

This section provides functional safety failure in time (FIT) rates for the WQFN package of the SN74AXC4T245-Q1 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	7
Die FIT rate	2
Package FIT rate	5

The failure rate and mission profile information in Table 2-3 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: motor control from table 11
- Power dissipation: 20 mW
- Climate type: world-wide table 8
- Package factor (lambda 3): table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	5 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.3 UQFN Package

This section provides functional safety failure in time (FIT) rates for the UQFN package of the SN74AXC4T245-Q1 based on two different industry-wide used reliability standards:

- Table 2-5 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-6 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-5. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	6
Die FIT rate	2
Package FIT rate	4

The failure rate and mission profile information in Table 2-5 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: motor control from table 11
- Power dissipation: 20 mW
- Climate type: world-wide table 8
- Package factor (lambda 3): table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-6. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-6 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for SN74AXC4T245-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Driver HIZ no output	18%
Output functional – out of specification timing or voltage	27%
Driver stuck at fault high	21%
Driver stuck at fault low	24%
Driver stuck at undetermined state	10%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the SN74AXC4T245-Q1 (TSSOP, WQFN and UQFN packages). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5 and Table 4-6)

Table 4-2 through Table 4-6 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1 .

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- External pullup resistor on $\overline{CS}$ to VDD
- RC filter on every analog input, AINx. Series resistors are sized to limit the input currents into the analog inputs to < 10mA in all circumstances (for example, in case the device is unpowered and the input signal is applied).
- The device is the only slave on the SPI bus.

4.1 TSSOP Package

Figure 4-1 shows the SN74AXC4T245-Q1 pin diagram for the TSSOP package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the SN74AXC4T245-Q1 data sheet.

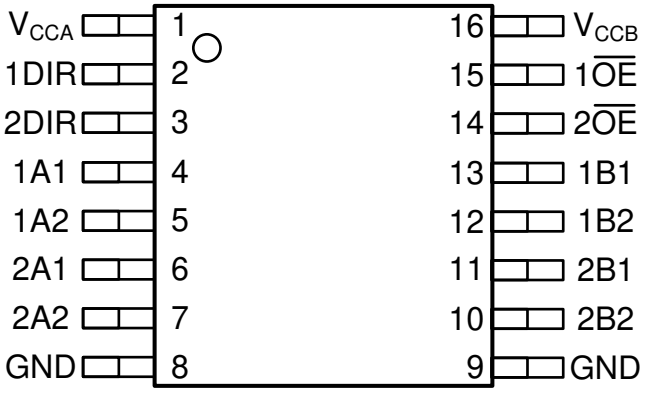

Figure 4-1. Pin Diagram (TSSOP) Package

4.2 WQFN Package

Figure 4-2 shows the SN74AXC4T245-Q1 pin diagram for the WQFN package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the SN74AXC4T245-Q1 data sheet.

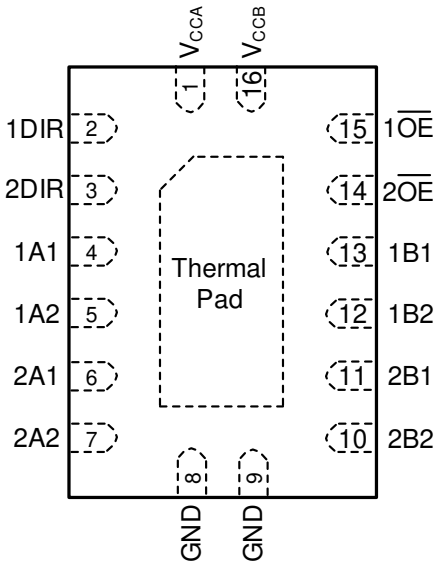

Figure 4-2. Pin Diagram (WQFN Package)

4.3 UQFN Package

Figure 4-3 shows the SN74AXC4T245-Q1 pin diagram for the UQFN package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the SN74AXC4T245-Q1 data sheet.

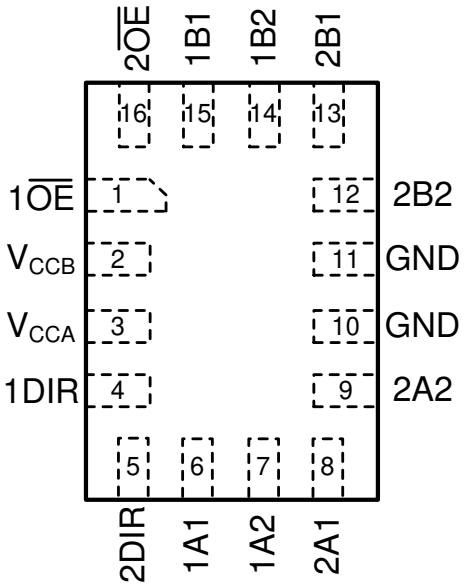

Figure 4-3. Pin Diagram (UQFN) Package

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VCCA	1	GND short to VCC, device will be bypassed - may cause system damage, but not device damage	B
DIR	2-3	Direction control will fix B --> A direction	B
1A1 - 2A2	4- 7	If configured as an output then damage is possible. If configured as input, no damage, but output will not switch	A
GND	8 - 9	Normal Operation	D
2B2 - 1B1	10 - 13	If configured as an output then damage is possible. If configured as input, no damage, but output will not switch	A
OE (active low)	14-15	Outputs will remain enabled	B
VCCB	16	GND short to VCC, device will be bypassed - may cause system damage, but not device damage	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VCCA	1	Device will not be powered	B
DIR	2-3	Direction control will fix B --> A direction	B
1A1 - 2A2	4- 7	If configured as output, normal operation. If configured as input, no damage, but output will not switch	B
GND	8 - 9	Device will not be powered	B
2B2 - 1B1	10 - 13	If configured as output, normal operation. If configured as input, no damage, but output will not switch	B
OE (active low)	14-15	Outputs will remain enabled	B
VCCB	16	Device will not be powered	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
VCCA	1	DIR1	Direction control will fix A --> B direction	B
1DIR	2-3	DIR2	If both HIGH, direction control will fix A --> B direction. If both LOW, direction control will fix B --> A direction. If one DIR is HIGH and the other is LOW, bus contention during transitions could occur and may cause high current	A
1A1	4 - 5	1A2	If 1A1 and 1A2 are configured as outputs then damage is possible. If configured as inputs, both bits will have the same value always	A
2A1	6-7	2A2	If 2A1 and 2A2 are configured as outputs then damage is possible. If configured as inputs, both bits will have the same v	A
GND	8 - 9	GND	Normal Operation	D
GND	9-10	2B2	If 2B2 is configured as an output then damage is possible. If configured as input, output 2A2 will be fixed LOW	A
2B2 or 2B1	10 - 13	1B2 or 1B1	If 2B2, 2B1, 1B2 and/or 1B1 are configured as outputs then damage is possible. If configured as inputs, both shorted bits will have the same value always	A
1B1	13-14	2OE (active low)	If 1B1 is configured as an output then damage is possible. If configured as input, no damage, but output 1A1 will remain HIGH or LOW dependent on 2OE (active low)	A
2OE (active low)	14-15	1OE (active low)	If 2OE and 1OE are configured as HIGH and LOW damage is possible. If configured as HIGH or LOW, both bits will have the same value always	A
1OE (active low)	24	VCCA	All associated outputs will be inactive and cannot be enabled	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to VCCA

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VCCA	1	Normal Operation	D
DIR	2-3	Direction control will fix A --> B direction	B
1A1 - 2A2	4- 7	If configured as an output then damage is possible. If configured as input, no damage, but output will not switch	A
GND	8 - 9	GND short to VCC, device will be bypassed - may cause system damage, but not device damage	B
2B2 - 1B1	10 - 13	If configured as an output then damage is possible. If configured as input, damage is possible if VIH/VIL not met	A
OE (active low)	14-15	Outputs will remain disabled	B
VCCB	16	VCCA short to VCCB, device will be bypassed - may cause system damage, but not device damage	B

Table 4-6. Pin FMA for Device Pins Short-Circuited to VCCB

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VCCA	1	VCCB short to VCCA, device will be bypassed - may cause system damage, but not device damage	B
DIR	2-3	If VCCA is greater than VCCB, then the direction control will fix B-->A, If VCCA is less than VCCB, damage is possible if VIH/VIL not met	A
1A1 - 2A2	4- 7	If A1 is configured as an output then damage is possible. If configured as input, damage is possible if VIH/VIL not met	A
GND	8 - 9	GND short to VCC, device will be bypassed - may cause system damage, but not device damage	B
2B2 - 1B1	10 - 13	If B2 is configured as an output then damage is possible. If configured as input, no damage, but output will not switch	A
OE (active low)	14-15	If VCCA is greater than VCCB, then the outputs will remain disabled, If VCCA is less than VCCB, damage is possible if VIH/VIL not met	A
VCCB	16	Normal Operation	D

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265