Functional Safety Information

TLV710-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for the TLV710-Q1 (SON package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

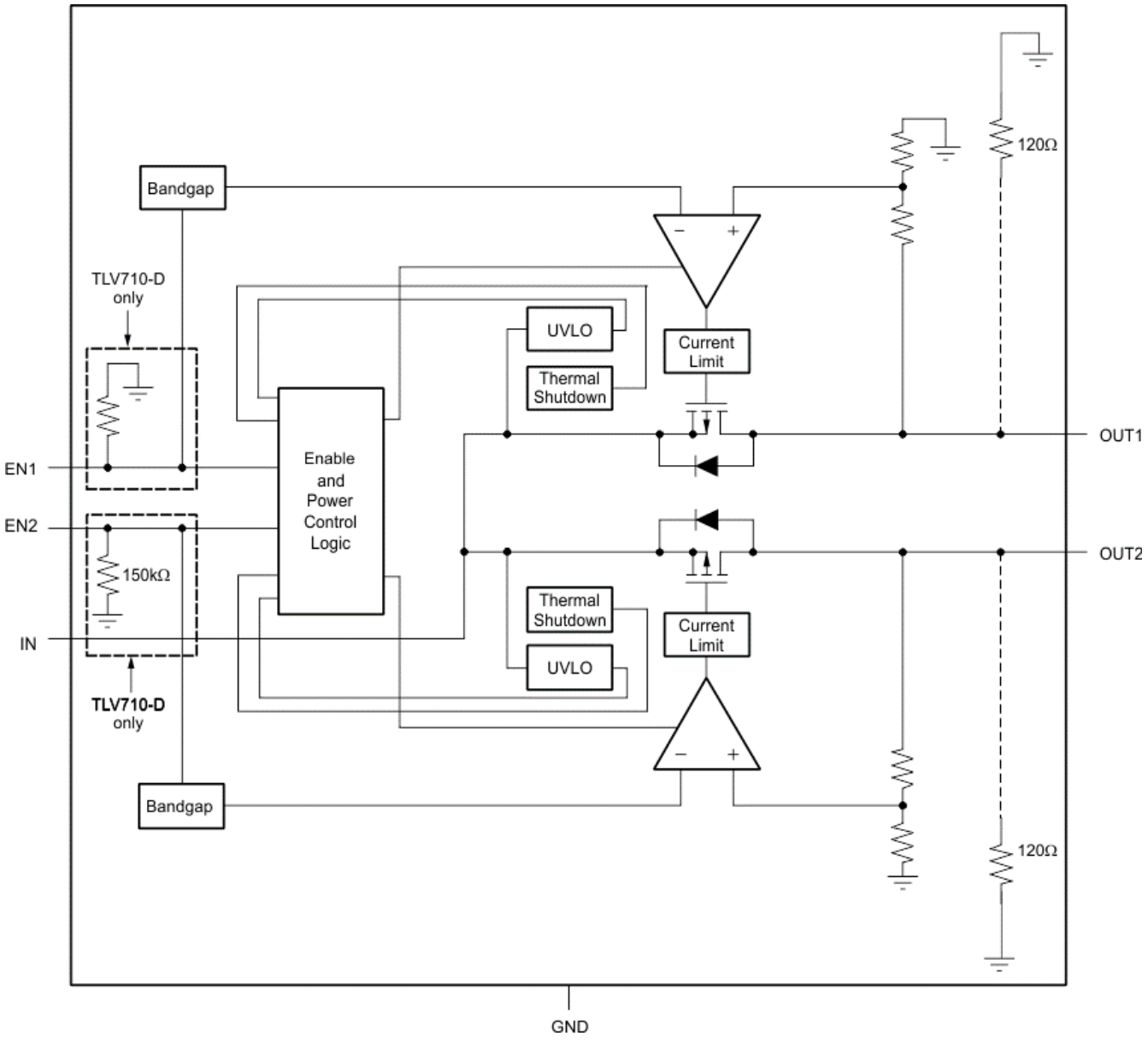

Figure 1-1. Functional Block Diagram

The TLV710-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the TLV710-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	8
Die FIT rate	6
Package FIT rate	2

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 250mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TLV710-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
VOUT high (following VIN)	40
VOUT not in specification (voltage or timing)	10
VOUT low (no output)	40
Short circuit any two pins	10

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TLV710-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to VIN (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the TLV710-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TLV710-Q1 data sheet.

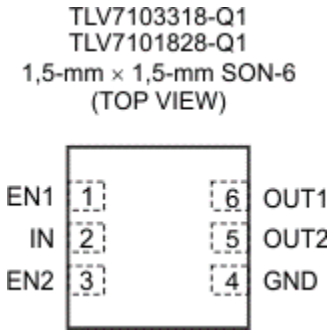

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Device contains DSE pin configuration. Device operates at free-air temperatures between -40°C and 125°C.
- Device operates at an input voltage less than 5.5V and more than 2V.
- Device operates according to all recommended operating conditions and does not exceed the absolute maximum ratings.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
EN1	1	LDO 1 is always off due to EN being grounded.	B
IN	2	Output voltage is at or near ground.	B
EN2	3	LDO 2 is always off due to EN being grounded.	B
GND	4	No effect. Normal operation.	D
OUT2	5	Output voltage 2 is at or near ground. Device is in current limit. The device can cycle in and out of thermal shutdown depending on power dissipation.	B
OUT1	6	Output voltage 1 is at or near ground. Device is in current limit. The device can cycle in and out of thermal shutdown depending on power dissipation.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
EN1	1	LDO is in unknown state.	B
IN	2	No input to LDO. Output is at or near ground.	B
EN2	3	LDO is in unknown state.	B
GND	4	There is no current loop for internal biasing; device cannot operate.	B
OUT2	5	Device 2 output is unregulated and the load is not powered.	B
OUT1	6	Device 1 output is unregulated and the load is not powered.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
EN1	1	IN	If EN is positive voltage above the IN absolute maximum rating, IN can be damaged.	A
IN	2	EN2	If EN is positive voltage above the IN absolute maximum rating, IN can be damaged.	A
GND	4	OUT2	Output voltage is at or near ground. Device is in current limit. The device can cycle in and out of thermal shutdown depending on power dissipation.	B
OUT2	5	OUT1	Output voltage is driven to unknown voltage. High current drive between pins is possible leading to potential thermal shutdown.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to VIN

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
EN1	1	If EN is positive voltage above the IN absolute maximum rating, IN can be damaged.	A
IN	2	No effect. Normal operation.	D
EN2	3	If EN is positive voltage above the IN absolute maximum rating, IN can be damaged.	A
GND	4	Output voltage is at or near ground.	B
OUT2	5	Regulation for LDO 2 is not possible. The output voltage equals input voltage.	B
OUT1	6	Regulation for LDO 1 is not possible. The output voltage equals input voltage.	B

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265