Functional Safety Information

TPS65219-Q1
Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

Trademarks

1 Overview

This document contains information for the TPS65219-Q1 (QFN package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

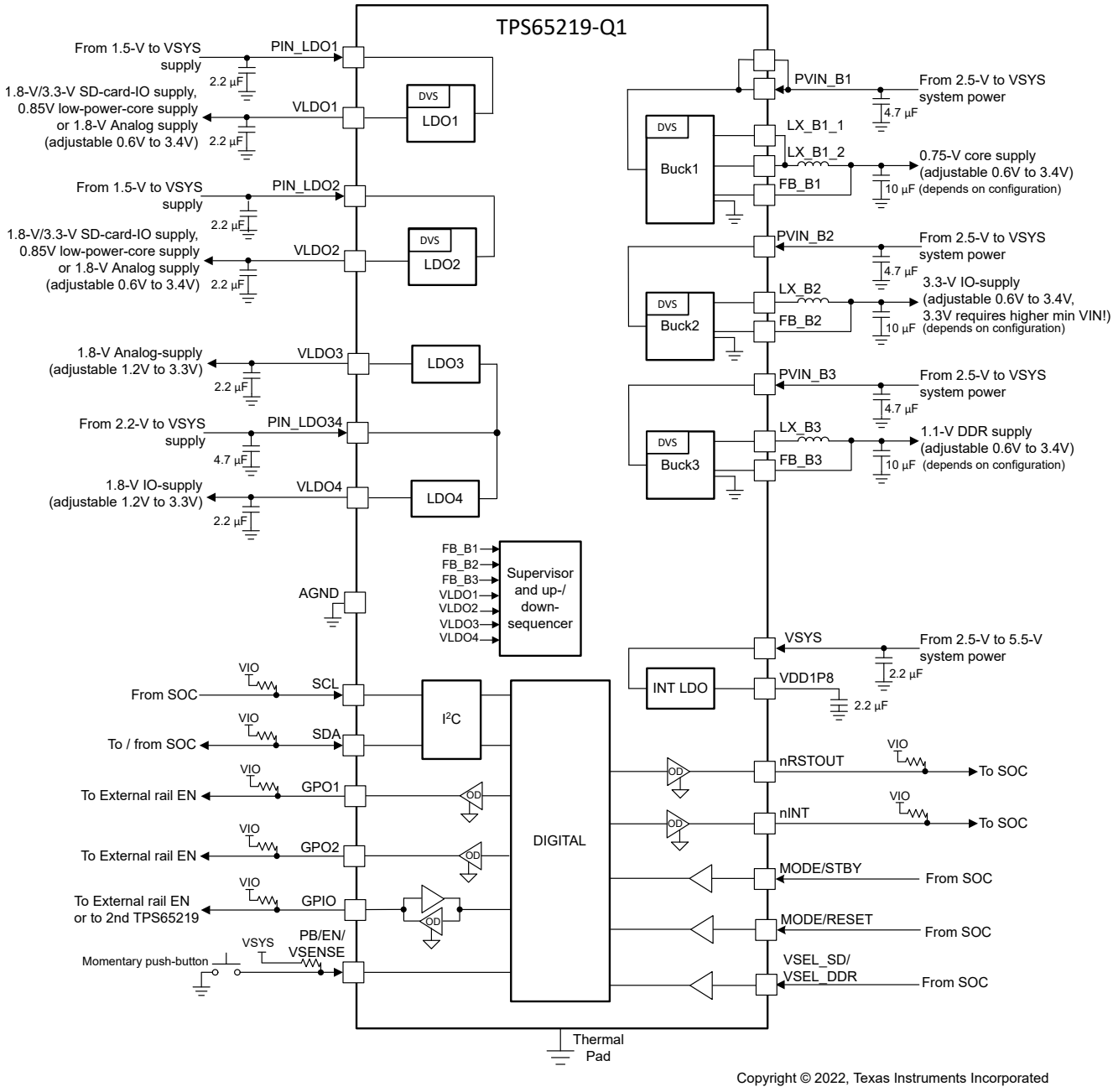

Figure 1-1. Functional Block Diagram

The TPS65219-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the TPS65219-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours) QFN Package
Total component FIT rate	28
Die FIT rate	8
Package FIT rate	20

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 2000mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	60 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TPS65219-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Reference system failure	3.73
Temperature monitor failure	0.46
BUCK1 failure	18.22
BUCK2 failure	12.88
BUCK3 failure	12.88
LDO1 failure	7.83
LDO2 failure	7.83
LDO3 failure	6.22
LDO4 failure	6.22
VDD1P8 failure	3.40
Oscillator failure	0.74
I2C interface failure	0.11
IO driver failure	1.85
nINT or nRSTOUT driver failure	0.76
NVM LDO failure	1.22
EEPROM failure	3.82
Digital logic failure	11.83

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS65219-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the TPS65219-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS65219-Q1 data sheet.

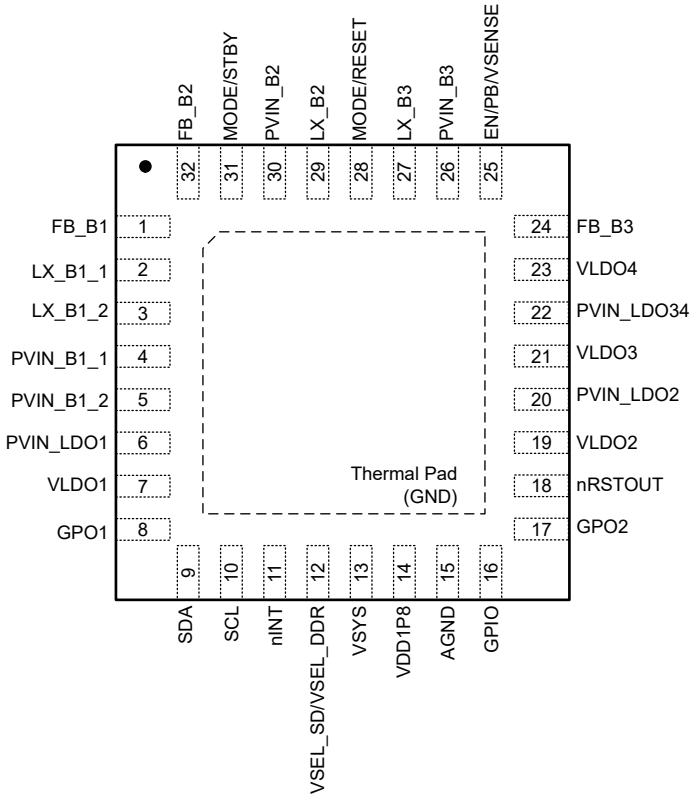

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The VSYS, PVIN_B1_1, PVIN_B1_2, PVIN_B2, PVIN_B3, PVIN_LDO1, PVIN_LDO2, and PVIN_LDO34 pins are all connected to a single input power supply.
- Multiple pin faults do not occur simultaneously.
- External pull-up and pull-down resistors are much larger than internal regulator discharge resistors.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
FB_B1	1	FB_B1 level is ground, Buck1 output is GND. Increased supply current.	B
LX_B1_1	2	LX_B1 voltage level is ground, output of Buck1 is ground. Potential permanent damage.	A
LX_B1_2	3	LX_B1 voltage level is ground, output of Buck1 is ground. Potential permanent damage (excessive current through high-side FET).	A
PVIN_B1_1	4	PVIN_B1 voltage level is ground, output of Buck1 is ground.	B
PVIN_B1_2	5	PVIN_B1 voltage level is ground, output of Buck1 is ground.	B
PVIN_LDO1	6	PVIN_LDO1 voltage level is ground, output of LDO1 is ground.	B
VLDO1	7	VLDO1 voltage level is ground.	B
GPO1	8	GPO voltage level is ground. External rail is permanently disabled.	B
SDA	9	SDA voltage level is ground, I2C communication is not possible.	B
SCL	10	SCL voltage level is ground, I2C communication is not possible.	B
nINT	11	nINT is permanently asserted low.	B
VSEL_SD/ VSEL_DDR	12	Configured as VSEL_SD: The LDO, configured as SD-card supply, delivers 1.8V or 3.3V permanently (VSEL_SD/VSEL_DDR is polarity dependent).	B
		Configured as VSEL_DDR and short occurs before ON request: Buck, configured as DDR supply, delivers BUCKx_VOUT.	C
		Configured as VSEL_DDR and short occurs after ON request: The pin state is only sensed at power-up, so shorts are ignored after.	D
VSYS	13	Short-circuit between VSYS and GND, likely causes an undervoltage (UV) on VSYS supply. Device enters OFF state (VSYS_POR).	B
VDD1P8	14	Internal LDO shorted. Potential damage (short-to-ground of VDD1P8 causing excessive current).	A
AGND	15	Normal operation.	D
GPIO	16	Configured for a multiple PMIC operation and short occurs before ON request: Synchronization with second PMIC is not possible, device does not power-up.	B
		Configured for a multiple PMIC operation and short occurs after ON request: Device powers-down asynchronously.	B
		Configured as GPO: External rail (if any) cannot be enabled.	B
GPO2	17	GPO voltage level is ground. External rail is permanently disabled.	B
nRSTOUT	18	nRSTOUT voltage level is ground. System is permanently held in RESET.	B
VLDO2	19	VLDO1 voltage level is ground.	B
PVIN_LDO2	20	PVIN_LDO2 voltage level is ground, output of LDO2 is ground.	B
VLDO3	21	VLDO3 voltage level is ground.	B
PVIN_LDO34	22	PVIN_LDO34 voltage level is ground, output of LDO3 and LDO4 is ground.	B
VLDO4	23	VLDO4 voltage level is ground.	B
FB_B3	24	FB_B3 level is ground, Buck3 output is ground.	B
EN/PB/VSENSE	25	Configured as EN or VSENSE and the device is unable to power-up (if short occurs before ON request) or powers-down (if short occurs after ON request).	B
EN/PB/VSENSE	25	Configured as PB and the device powers up once VSYS is applied and remains powered up (if short occurs before ON request) or powers down (if short occurs after ON request).	B
PVIN_B3	26	PVIN_B3 voltage level is ground, output of Buck3 is ground.	B
LX_B3	27	LX_B3 voltage level is ground, output of Buck3 is ground. Potential permanent damage.	A
MODE/RESET	28	Configured as MODE: Device operates in forced PWM or automatic PFM, dependent on MODE polarity, irrespective of pullup or pulldown.	C
		Configured as RESET: Device executes RESET once with no further pin triggered RESET (if pin is configured active-low polarity) or RESET cannot be triggered by the pin (if pin is configured active-high polarity).	B
LX_B2	29	LX_B2 voltage level is ground, output of Buck2 is ground. Potential permanent damage.	A
PVIN_B2	30	PVIN_B2 voltage level is ground, output of Buck2 is ground.	B

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
MODE/STBY	31	Configured as MODE and device operates in forced PWM or automatic PFM, dependent on MODE polarity, irrespective of pullup or pulldown.	C
		Configured as STBY and the device enters the STBY state immediately after power up and remains in STBY (if pin is configured active-low polarity), or STBY cannot be triggered by the pin (if the pin is configured active-high polarity).	B
FB_B2	32	FB_B2 level is ground, Buck2 output is ground. Increased supply current.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
FB_B1	1	Buck1 output voltage is rising up to PVIN_B1. Potential damage to system components.	B
LX_B1_1	2	Normal operation, lower efficiency, higher power dissipation and heating.	C
LX_B1_2	3	Normal operation, lower efficiency, higher power dissipation and heating.	C
PVIN_B1_1	4	Normal operation, lower efficiency, higher power dissipation and heating.	C
PVIN_B1_2	5	Normal operation, lower efficiency, higher power dissipation and heating.	C
PVIN_LDO1	6	PVIN_LDO1 voltage level is undetermined. LDO1 output not available.	B
VLDO1	7	VLDO1 voltage level is undetermined.	B
GPO1	8	No control over external rail. Rail status depends on external configuration.	B
SDA	9	SDA voltage level is undetermined, I2C communication is not possible.	B
SCL	10	SCL voltage level is undetermined, I2C communication is not possible.	B
nINT	11	nINT signal invalid, device cannot trigger the interrupt of the SoC.	B
VSEL_SD/ VSEL_DDR	12	Configured as VSEL_SD: The pin voltage level is undetermined. The LDO configured as SD-card supply can transition between 1.8V and 3.3V if noise on the pin is above thresholds and duration > deglitch time.	B
		Configured as VSEL_DDR and short occurs before ON request: Buck configured as DDR supply delivers 1.2V.	C
		Configured as VSEL_DDR and short occurs after ON request: The pin is only sensed at power-up, so shorts are ignored after.	D
VSYS	13	PMIC not supplied. No power-up possible. Potential damage (violating VSYS versus PVIN voltage ratings).	A
VDD1P8	14	VDD1P8 output can oscillate, shut off, or not power up. Potential damage.	A
AGND	15	Increased noise, as PGND needs to serve as analog GND.	C
GPIO	16	Configured for a multiple PMIC operation: Synchronization with second PMIC is not possible, no controlled power down is possible, device with fault sequences down.	B
		Configured as GPO: No control over external rail. Rail status depends on external configuration.	B
GPO2	17	No control over external rail. Rail status depends on external configuration.	B
nRSTOUT	18	nRSTOUT voltage level is undetermined. nRSTOUT signal invalid, system can shut down, not come out of RESET, or come out of RESET too early.	B
VLDO2	19	VLDO2 voltage level is undetermined.	B
PVIN_LDO2	20	PVIN_LDO2 voltage level is undetermined. LDO2 output not available.	B
VLDO3	21	VLDO3 voltage level is undetermined.	B
PVIN_LDO34	22	PVIN_LDO34 voltage level is undetermined. LDO3 and LDO4 output not available.	B
VLDO4	23	VLDO4 voltage level is undetermined.	B
FB_B3	24	Buck3 output voltage is rising up to PVIN_B3. Potential damage to system components.	B
EN/PB/VSENSE	25	No valid ON request possible. ON request can only trigger on noise if beyond thresholds for longer than deglitch time.	B
PVIN_B3	26	PVIN_B3 voltage level is undetermined. Buck3 output is off.	B
LX_B3	27	LX_B3 voltage level is undetermined. Output of Buck3 is determined by external circuitry.	B
MODE/RESET	28	Configured as MODE: Pin level is undetermined, the device can operate in forced PWM or automatic PFM.	C
		Configured as RESET: Pin level is undetermined, RESET can be triggered by noise, if above threshold and deglitch time.	B
LX_B2	29	LX_B2 voltage level is undetermined. Output of Buck2 is determined by external circuitry.	B
PVIN_B2	30	PVIN_B2 voltage level is undetermined. Buck2 output is off.	B
MODE/STBY	31	Configured as MODE: Device operates in forced PWM or automatic PFM, dependent on MODE polarity.	C
		Configured as STBY: Device transitions to STBY state.	B
FB_B2	32	Buck2 output voltage is rising up to PVIN_B2. Potential damage to system components.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
FB_B1	1	LX_B1_1	FB_B1 voltage is LX_B1_1. Buck1 is not able to regulate the output voltage. Potential damage to system components.	B
LX_B1_1	2	LX_B1_2	Normal operation.	D
LX_B1_2	3	PVIN_B1_1	LX_B1 voltage level is PVIN_B1, output of Buck1 is PVIN_B1. Potential permanent damage (excessive current through low-side FET).	A
PVIN_B1_1	4	PVIN_B1_2	Normal operation.	D
PVIN_B1_2	5	PVIN_LDO1	Normal operation, potentially higher power dissipation and higher temperature.	C
PVIN_LDO1	6	VLDO1	VLDO1 voltage level is PVIN_LDO1 (LDO output = LDO input voltage). Potential damage to system components.	B
VLDO1	7	GPO1	GPO voltage level is VLDO1. External regulator (if present) is enabled when LDO1 is enabled (provided Vout_LDO1 is sufficiently high). Potential violation of sequence. Potential LDO1 undervoltage detection.	B
GPO1	8	SDA	GPO voltage level is VSYS. External rail can be enabled based on the average voltage level of SDA. I2C communication is unavailable if GPO1 is driven low.	B
SDA	9	SCL	SCL voltage level is dependent on both signal levels, I2C interface not available.	B
SCL	10	nINT	SCL and nINT voltage level is dependent on both signal levels, I2C interface not available, nINT level undetermined. If nINT is driven low, I2C communication is not available.	B
nINT	11	VSEL_SD/ VSEL_DDR	Configured as VSEL_SD: The LDO, configured as SD-card supply, delivers 1.8V or 3.3V based on nINT and VSEL_SD pin status. nINT can be falsely triggered or released even though an INT_SOURCE bit is set (VSEL_SD/ VSEL_DDR is polarity dependent).	B
			Configured as VSEL_DDR and short is applied before ON request: Buck, configured as DDR supply, delivers BUCKx_VOUT or 1.35V, based on nINT and VSEL_DDR pin status.	C
			Configured as VSEL_DDR, and short is applied after ON request: VSEL_DDR is only sensed at power-up, so shorts are ignored after.	B
VSEL_SD/ VSEL_DDR	12	VSYS	Configured as VSEL_SD: The LDO, configured as SD-card supply, delivers 1.8V or 3.3V permanently (VSEL_SD/VSEL_DDR is polarity dependent).	B
			Configured as VSEL_DDR and short occurs before ON request: Buck, configured as DDR supply, delivers 1.35V.	C
			Configured as VSEL_DDR and short occurs after ON request: The pin is only sensed at power up, so shorts are ignored after.	D
VSYS	13	VDD1P8	Short-circuit between VSYS and VDD1P8 causes a VDD1P8 fault. Device enters OFF state. Potential damage.	A
VDD1P8	14	AGND	Internal LDO shorted. Potential damage (short-to-ground of VDD1P8 causing excessive current).	A
AGND	15	GPIO	Configured for a multiple PMIC operation and short occurs before ON request: Synchronization with second PMIC is not possible, device does not power up.	B
			Configured for a multiple PMIC operation and short occurs after ON request: Device powers down asynchronously.	B
			Configured as GPO: External rail (if any) cannot be enabled.	B
GPIO	16	GPO2	Configured for a multiple PMIC operation and short occurs before ON request: Device does not power up.	B
			Configured for a multiple PMIC operation and short occurs after ON request: If GPO2 is driven low, PMICs sequence down. GPIO communication toggles the GPO2-controlled external rail on and off.	B
			Configured as GPO: Driving one GPO low disables both external rails.	B
GPO2	17	nRSTOUT	GPO2 level is dependent on nRSTOUT and vice-versa. System can enter reset or disable an external rail unexpectedly.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
nRSTOUT	18	VLDO2	nRSTOUT voltage level is VLDO2. nRSTOUT is pulled high once VLDO2 ramps up. System can come out of reset prematurely or not at all if VLDO is not sequenced or has too low output voltage.	B
VLDO2	19	PVIN_LDO2	PVIN_LDO2 and VLDO2 voltage level is PVIN_LDO2 (LDO output = LDO input voltage). Potential damage to system components.	B
PVIN_LDO2	20	VLDO3	PVIN_LDO2 and VLDO3 voltage level is PVIN_LDO2 (LDO3 output = LDO2 input voltage). Potential damage to system components.	B
VLDO3	21	PVIN_LDO34	PVIN_LDO34 and VLDO3 voltage level is PVIN_LDO34 (LDO output = LDO input voltage). Potential damage to system components.	B
PVIN_LDO34	22	VLDO4	PVIN_LDO34 and VLDO4 voltage level is PVIN_LDO34 (LDO output = LDO input voltage). Potential damage to system components.	B
VLDO4	23	FB_B3	Undervoltage detection on LDO4 or BUCK3.	B
FB_B3	24	EN/PB/VSENSE	Configured as EN/VSENSE: Pin voltage level is FB_B3. An OFF request or permanent ON request is triggered depending on BUCK3 output voltage. Pulling the pin low is not possible or loads Buck3.	B
			Configured as PB and short occurs before ON request: Pin voltage level is ground. An ON request is triggered. Pulling the pin low is not possible or loads Buck3.	B
			Configured as PB and short occurs after ON request: Pin voltage level is FB_B3. An OFF request is triggered if the BUCK3 output voltage is below threshold. Pulling the pin low is not possible or loads Buck3.	B
EN/PB/VSENSE	25	PVIN_B3	Configured as EN/VSENSE and short occurs before ON request: Device immediately powers up.	B
			Configured as EN/VSENSE and short occurs after ON request: Device ignores OFF requests from the pin.	B
			Configured as PB and short occurs before ON request: ON request using PB press is not possible or loads Buck3 supply.	B
			Configured as PB and short occurs after ON request: OFF request using PB press is not possible or loads Buck3-supply.	B
PVIN_B3	26	LX_B3	LX_B3 voltage level is PVIN_B3 voltage. Potential damage to system components.	B
LX_B3	27	MODE/RESET	Configured as MODE: Device operates in forced PWM or automatic PFM, dependent on MODE polarity and Buck3 output voltage.	C
			RESET is determined by Buck3 voltage and RESET polarity.	B
MODE/RESET	28	LX_B2	Configured as MODE: Device operates in forced PWM or automatic PFM, dependent on MODE polarity and Buck2 output voltage.	C
			RESET is determined by Buck2 voltage and RESET polarity.	B
LX_B2	29	PVIN_B2	LX_B2 voltage level is PVIN_B2, output of Buck2 is V(PVIN_B2). Potential permanent damage (exceeding absolute maximum rating of FB_B2 pin) to device and system components.	A
PVIN_B2	30	MODE/STBY	Configured as MODE: Device operates in forced PWM or automatic PFM, dependent on MODE polarity, irrespective of pullup or pulldown.	C
			Configured as STBY: Device powers up and immediately enters STBY permanently, or STBY cannot be triggered by the pin, depending on STBY polarity.	B
MODE/STBY	31	FB_B2	Configured as MODE: Device operates in forced PWM or automatic PFM, dependent on MODE polarity and FB_B2 voltage, regarding the MODE/STBY threshold, irrespective of pullup or pulldown.	C
			Configured as STBY: Device powers up and immediately enters STBY permanently, or STBY cannot be triggered by the pin, depending on STBY polarity and FB_B2 voltage, regarding the MODE/STBY threshold.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
FB_B2	32	FB_B1	BUCK1 and BUCK2 have the same output voltage: BUCK1 and BUCK2 regulate to the common output voltage.	B
			BUCK1 and BUCK2 have different output voltages: One or both regulators detect UV or OC faults, or both.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
FB_B1	1	FB_B1 voltage level is VSYS.	B
LX_B1_1	2	LX_B1 voltage level is VSYS, output of Buck1 is VSYS. Potential permanent damage (excessive current through low-side FET).	A
LX_B1_2	3	LX_B1 voltage level is VSYS, output of Buck1 is VSYS. Potential permanent damage (excessive current through low-side FET).	A
PVIN_B1_1	4	Normal operation.	D
PVIN_B1_2	5	Normal operation.	D
PVIN_LDO1	6	Normal operation, potentially higher power dissipation and higher temperature.	C
VLDO1	7	VLDO1 voltage level is VSYS. Potential damage to system components.	B
GPO1	8	GPO voltage level is VSYS. External rail is enabled once VSYS is applied.	B
SDA	9	SDA voltage level is VSYS, I2C communication is not possible.	B
SCL	10	SCL voltage level is VSYS, I2C communication is not possible.	B
nINT	11	nINT permanently pulled high, device cannot trigger the interrupt of the SoC.	B
VSEL_SD/ VSEL_DDR	12	Configured as VSEL_SD: The LDO, configured as SD-card supply, delivers permanently 1.8V or 3.3V (VSEL_SD/VSEL_DDR is polarity dependent).	B
		Configured as VSEL_DDR and short occurs before ON request: Buck, configured as DDR supply, delivers 1.35V.	C
		Configured as VSEL_DDR and short occurs after ON request: The pin is only sensed at power up, so shorts are ignored after.	D
VSYS	13	Normal operation.	D
VDD1P8	14	Internal LDO overdriven. Device enters OFF state. Potential damage (violating absolute maximum of VDD1P8).	A
AGND	15	Short-circuit between VSYS and GND likely causes a fault on the VSYS supply. Device enters OFF state (VSYS_POR).	B
GPIO	16	Configured for a multiple PMIC operation and short applied before ON request: The short initiates power up but GPIO cannot pull low.	B
		Configured for a multiple PMIC operation and short applied after ON request: High current through GPIO output stage, potential permanent damage.	D
		Configured as GPO: External rail (if any) is permanently enabled, once VSYS is present.	B
GPO2	17	GPO voltage level is VSYS. External rail is enabled once VSYS is applied.	B
nRSTOUT	18	nRSTOUT voltage level is VSYS. System is prematurely released out of RESET once VSYS is applied.	B
VLDO2	19	VLDO2 voltage level is VSYS. Potential damage to system components.	B
PVIN_LDO2	20	Normal operation, potentially higher power dissipation and higher temperature.	C
VLDO3	21	VLDO3 voltage level is VSYS. Potential damage to system components.	B
PVIN_LDO34	22	Normal operation, potentially higher power dissipation and higher temperature.	C
VLDO4	23	VLDO4 voltage level is VSYS. Potential damage to system components.	B
FB_B3	24	FB_B3 voltage level is VSYS. Potential damage to system components.	B
EN/PB/VSENSE	25	Configured as EN: Device powers up once VSYS is applied and ignores EN-OFF request.	B
EN/PB/VSENSE	25	Configured as PB: Press causes a short-circuit between VSYS and GND and likely causes a fault on VSYS supply.	B
PVIN_B3	26	Normal operation.	D
LX_B3	27	LX_B3 voltage level is VSYS, output of Buck3 is VSYS. Potential permanent damage (exceeding absolute maximum rating of FB_B3 pin) to device and system components.	A
MODE/RESET	28	Configured as MODE: Device operates in forced PWM or automatic PFM, dependent on MODE polarity, irrespective of pullup or pulldown.	C
		Configured as RESET: RESET cannot be triggered by the pin (if RESET is configured active-low polarity), or device executes RESET once with no further pin-triggered RESET (if RESET is configured active-high polarity).	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
LX_B2	29	LX_B2 voltage level is VSYS, output of Buck2 is VSYS. Potential permanent damage (exceeding absolute maximum rating of FB_B2 pin) to device and system components.	A
PVIN_B2	30	Normal operation.	D
MODE/STBY	31	Configured as MODE: Device operates in forced PWM or automatic PFM, dependent on MODE polarity, irrespective of pullup or pulldown.	C
		Configured as STBY: Device powers up and immediately enters STBY permanently, or STBY cannot be triggered by the pin, depending on STBY polarity.	B
FB_B2	32	FB_B2 voltage level is VSYS. Potential damage to system components.	B

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (September 2023) to Revision A (May 2025)	Page
• First public release	2

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