*Functional Safety Information*

# *UCC1413x-Q1 Functional Safety FIT Rate, FMD, and Pin FMA*

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# 1 Overview

This document contains information for the UCC1413x-Q1 (DWN-36 package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

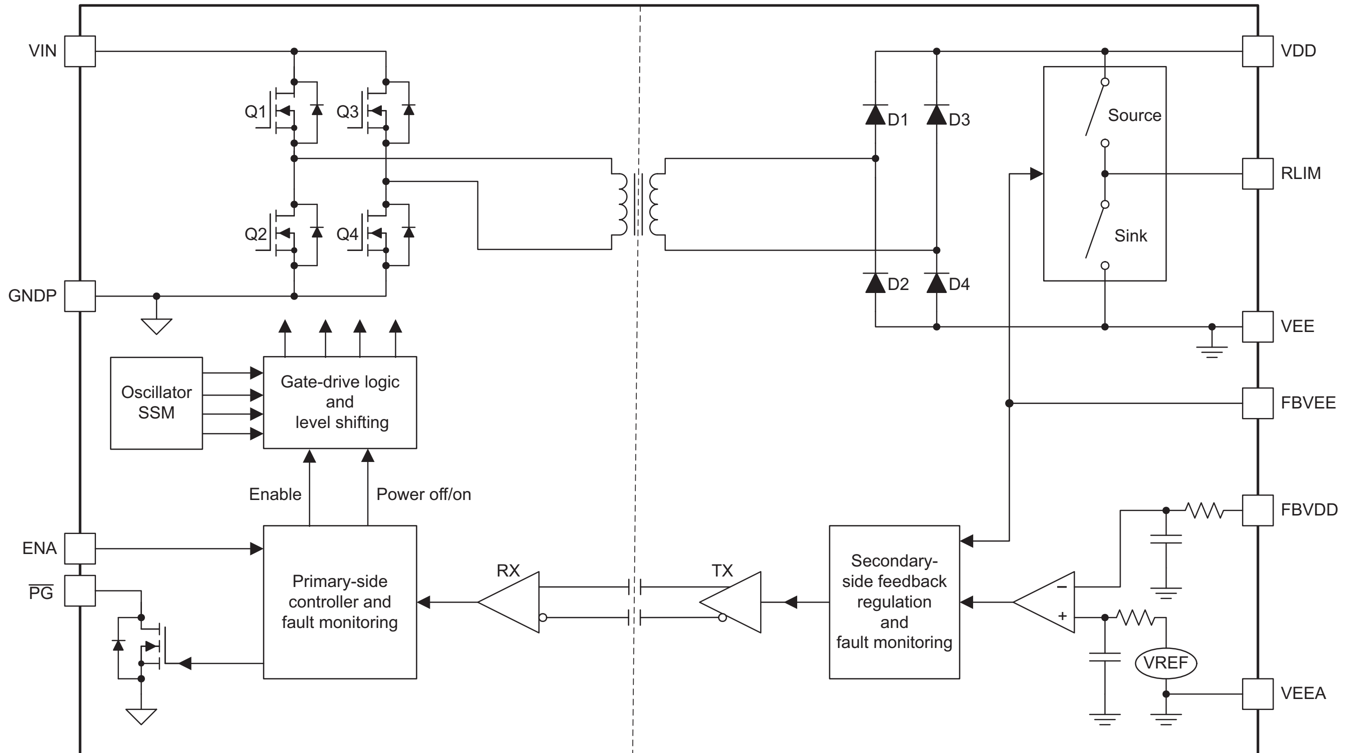


**Figure 1-1. Functional Block Diagram**

The UCC1413x-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.



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# 2 Functional Safety Failure In Time (FIT) Rates

## 2.1 DWN-36 Package

This section provides functional safety failure in time (FIT) rates for the DWN-36 package of the UCC1413x-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

**Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11**

| FIT IEC TR 62380 / ISO 26262 | FIT (Failures Per $10^9$ Hours) |
|---|---|
| Total component FIT rate (1500 mW, 1000 mW, 500 mW) | 43, 39, 35 |
| Die FIT rate (1500 mW, 1000 mW, 500 mW) | 8, 6, 4 |
| Package FIT rate (1500 mW, 1000 mW, 500 mW) | 35, 33, 31 |

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 1500 mW, 1000 mW, 500 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

**Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2**

| Table | Category | Reference FIT Rate | Reference Virtual $T_J$ |
|---|---|---|---|
| 5 | CMOS, BICMOS<br>Digital, analog, or mixed | 60 FIT | 70°C |

The reference FIT rate and reference virtual $T_J$ (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.



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# 3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the UCC1413x-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

**Table 3-1. Die Failure Modes and Distribution**

| Die Failure Modes | Failure Mode Distribution (%) |
|---|---|
| VDD or VEE has no power | 59 |
| VDD or VEE accuracy not meeting spec | 25 |
| PG indicates wrong state | 10 |
| Degraded EMI performance | 3 |
| No effect | 3 |

The FMD in Table 3-1 excludes short-circuit faults across the isolation barrier. Faults for short circuits across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a safety-separated extra low voltage (SELV) or protective extra low voltage (PELV) power supply is used, pollution degree 2 / OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.



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# 4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the UCC1413x-Q1 (DWN-36 package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3 )
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5 )

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

**Table 4-1. TI Classification of Failure Effects**

| Class | Failure Effects |
|---|---|
| A | Potential device damage that affects functionality |
| B | No device damage, but loss of functionality |
| C | No device damage, but performance degradation |
| D | No device damage, no impact to functionality or performance |

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The device is configured as Dual Adjustable Output Configuration diagram in the Typical Application sestion of the datasheet
- VIN is considered as the supply pin for primary-side pins
- GNDP is considered as the ground pin for primary-side pins
- VDD is considered as the supply pin for secondary-side pins
- VEE is considered as the ground pin for secondary-side pins

## 4.1 DWN-36 Package

Figure 4-1 shows the UCC1413x-Q1 pin diagram for the DWN-36 package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the UCC1413x-Q1 data sheet.

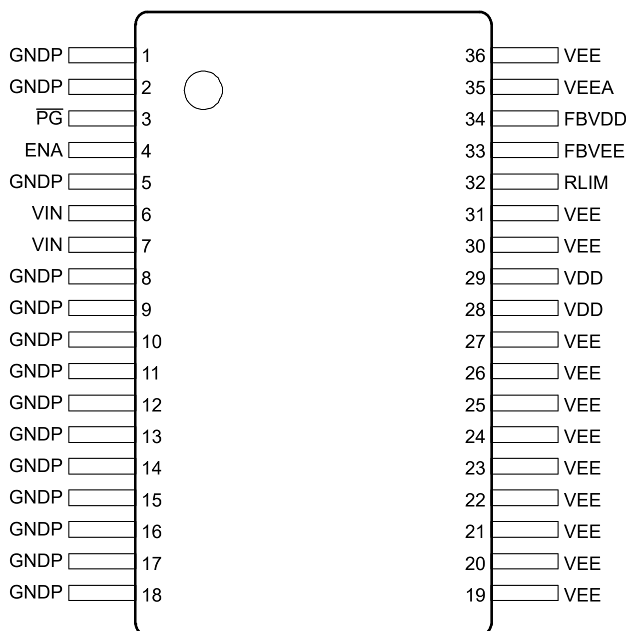


**Figure 4-1. Pin Diagram (DWN-36) Package**


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### Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| GNDP | 1 | No effect. | D |
| GNDP | 2 | No effect. | D |
| $\overline{PG}$ | 3 | $\overline{PG}$ is always low. MCU can't detect the status of the bias supply. | C |
| ENA | 4 | Device is disabled. No output. | B |
| GNDP | 5 | No effect. | D |
| VIN | 6 | Device is not powered. No output. | B |
| VIN | 7 | Device is not powered. No output. | B |
| GNDP | 8 | No effect. | D |
| GNDP | 9 | No effect. | D |
| GNDP | 10 | No effect. | D |
| GNDP | 11 | No effect. | D |
| GNDP | 12 | No effect. | D |
| GNDP | 13 | No effect. | D |
| GNDP | 14 | No effect. | D |
| GNDP | 15 | No effect. | D |
| GNDP | 16 | No effect. | D |
| GNDP | 17 | No effect. | D |
| GNDP | 18 | No effect. | D |
| VEE | 19 | No effect. | D |
| VEE | 20 | No effect. | D |
| VEE | 21 | No effect. | D |
| VEE | 22 | No effect. | D |
| VEE | 23 | No effect. | D |
| VEE | 24 | No effect. | D |
| VEE | 25 | No effect. | D |
| VEE | 26 | No effect. | |
| VEE | 27 | No effect. | D |
| VDD | 28 | Device is disabled. No output. | B |
| VDD | 29 | Device is disabled. No output. | B |
| VEE | 30 | No effect. | D |
| VEE | 31 | No effect. | D |
| RLIM | 32 | Device is disabled. No output. | B |
| FBVEE | 33 | Device is disabled. No output. | B |
| FBVDD | 34 | Device is disabled. No output. | B |
| VEEA | 35 | No effect. | D |
| VEE | 36 | No effect. | D |


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**Table 4-3. Pin FMA for Device Pins Open-Circuited**

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| GNDP | 1 | No effect. | D |
| GNDP | 2 | No effect. | D |
| $\overline{PG}$ | 3 | MCU can't detect the status of the bias supply. | C |
| ENA | 4 | Undetermined state. The device could be on or off, depending on the noise on ENA pin. | B |
| GNDP | 5 | No effect. | D |
| VIN | 6 | Device is disabled. No output. | B |
| VIN | 7 | Device is disabled. No output. | B |
| GNDP | 8 | Voltage ringing will increase above normal increasing voltage stress at maximum VIN voltage. | C |
| GNDP | 9 | Voltage ringing will increase above normal increasing voltage stress at maximum VIN voltage. | C |
| GNDP | 10 | No effect. | D |
| GNDP | 11 | No effect. | D |
| GNDP | 12 | No effect. | D |
| GNDP | 13 | No effect. | D |
| GNDP | 14 | No effect. | D |
| GNDP | 15 | No effect. | D |
| GNDP | 16 | No effect. | D |
| GNDP | 17 | No effect. | D |
| GNDP | 18 | No effect. | D |
| VEE | 19 | No effect. | D |
| VEE | 20 | No effect. | D |
| VEE | 21 | No effect. | D |
| VEE | 22 | No effect. | D |
| VEE | 23 | No effect. | D |
| VEE | 24 | No effect. | D |
| VEE | 25 | No effect. | D |
| VEE | 26 | No effect. | D |
| VEE | 27 | No effect. | D |
| VDD | 28 | Voltage ringing will increase above normal increasing voltage stress at maximum VIN voltage. | C |
| VDD | 29 | Voltage ringing will increase above normal increasing voltage stress at maximum VIN voltage. | C |
| VEE | 30 | Voltage ringing will increase above normal increasing voltage stress at maximum VIN voltage. | C |
| VEE | 31 | Voltage ringing will increase above normal increasing voltage stress at maximum VIN voltage. | C |
| RLIM | 32 | Device is disabled. No output. | B |
| FBVEE | 33 | Device is disabled. No output. | B |
| FBVDD | 34 | Device is disabled. No output. | B |
| VEEA | 35 | No effect. | D |
| VEE | 36 | No effect. | D |


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**Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin**

| Pin Name | Pin No. | Shorted to | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|---|
| GNDP | 1 | GNDP | No effect. | D |
| GNDP | 2 | $\overline{PG}$ | Device is disabled. No output. | B |
| $\overline{PG}$ | 3 | ENA | Device can't stay on because once output voltage is generated, $\overline{PG}$ will disable the device | B |
| ENA | 4 | GNDP | Device is disabled. No output. | B |
| GNDP | 5 | VIN | Device is not powered. No output. | B |
| VIN | 6 | VIN | No effect. | D |
| VIN | 7 | GNDP | Device is not powered. No output. | B |
| GNDP | 8 | GNDP | No effect. | D |
| GNDP | 9 | GNDP | No effect. | D |
| GNDP | 10 | GNDP | No effect. | D |
| GNDP | 11 | GNDP | No effect. | D |
| GNDP | 12 | GNDP | No effect. | D |
| GNDP | 13 | GNDP | No effect. | D |
| GNDP | 14 | GNDP | No effect. | D |
| GNDP | 15 | GNDP | No effect. | D |
| GNDP | 16 | GNDP | No effect. | D |
| GNDP | 17 | GNDP | No effect. | D |
| GNDP | 18 | N/A | N/A | N/A |
| VEE | 19 | VEE | No effect. | D |
| VEE | 20 | VEE | No effect. | D |
| VEE | 21 | VEE | No effect. | D |
| VEE | 22 | VEE | No effect. | D |
| VEE | 23 | VEE | No effect. | D |
| VEE | 24 | VEE | No effect. | D |
| VEE | 25 | VEE | No effect. | D |
| VEE | 26 | VEE | No effect. | D |
| VEE | 27 | VDD | Device is disabled. No output. | B |
| VDD | 28 | VDD | No effect. | D |
| VDD | 29 | VEE | Device is disabled. No output. | B |
| VEE | 30 | VEE | No effect. | D |
| VEE | 31 | RLIM | Device is disabled. No output. | B |
| RLIM | 32 | FBVEE | RLIM will not regulate correctly. | B |
| FBVEE | 33 | FBVDD | VDD and RLIM can't regulate correctly. | B |
| FBVDD | 34 | VEEA | Device is disabled. No output. | B |
| VEEA | 35 | VEE | No effect. | D |
| VEE | 36 | N/A | N/A | N/A |


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**Table 4-5. Pin FMA for Device Pins Short-Circuited to supply**

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| GNDP | 1 | Device is not powered. No output. | B |
| GNDP | 2 | Device is not powered. No output. | B |
| $\overline{PG}$ | 3 | Exceed pin abs. max rating. Device damage is possible. | A |
| ENA | 4 | Device is always enabled. Pin voltage exceeds abs. max rating. Device damage is possible. | A |
| GNDP | 5 | Device is not powered. No output. | B |
| VIN | 6 | No effect. | D |
| VIN | 7 | No effect. | D |
| GNDP | 8 | Device is not powered. No output. | B |
| GNDP | 9 | Device is not powered. No output. | B |
| GNDP | 10 | Device is not powered. No output. | B |
| GNDP | 11 | Device is not powered. No output. | B |
| GNDP | 12 | Device is not powered. No output. | B |
| GNDP | 13 | Device is not powered. No output. | B |
| GNDP | 14 | Device is not powered. No output. | B |
| GNDP | 15 | Device is not powered. No output. | B |
| GNDP | 16 | Device is not powered. No output. | B |
| GNDP | 17 | Device is not powered. No output. | B |
| GNDP | 18 | Device is not powered. No output. | B |
| VEE | 19 | Device is disabled. No output. | B |
| VEE | 20 | Device is disabled. No output. | B |
| VEE | 21 | Device is disabled. No output. | B |
| VEE | 22 | Device is disabled. No output. | B |
| VEE | 23 | Device is disabled. No output. | B |
| VEE | 24 | Device is disabled. No output. | B |
| VEE | 25 | Device is disabled. No output. | B |
| VEE | 26 | Device is disabled. No output. | B |
| VEE | 27 | Device is disabled. No output. | B |
| VDD | 28 | No effect. | D |
| VDD | 29 | No effect. | D |
| VEE | 30 | Device is disabled. No output. | B |
| VEE | 31 | Device is disabled. No output. | B |
| RLIM | 32 | Device is disabled. No output. | B |
| FBVEE | 33 | Device is disabled. No output. | B |
| FBVDD | 34 | Device is disabled. No output. | B |
| VEEA | 35 | Device is disabled. No output. | B |
| VEE | 36 | Device is disabled. No output. | B |



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