Functional Safety Information

TPS7B83-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for the TPS7B83-Q1 (SOT-223 package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

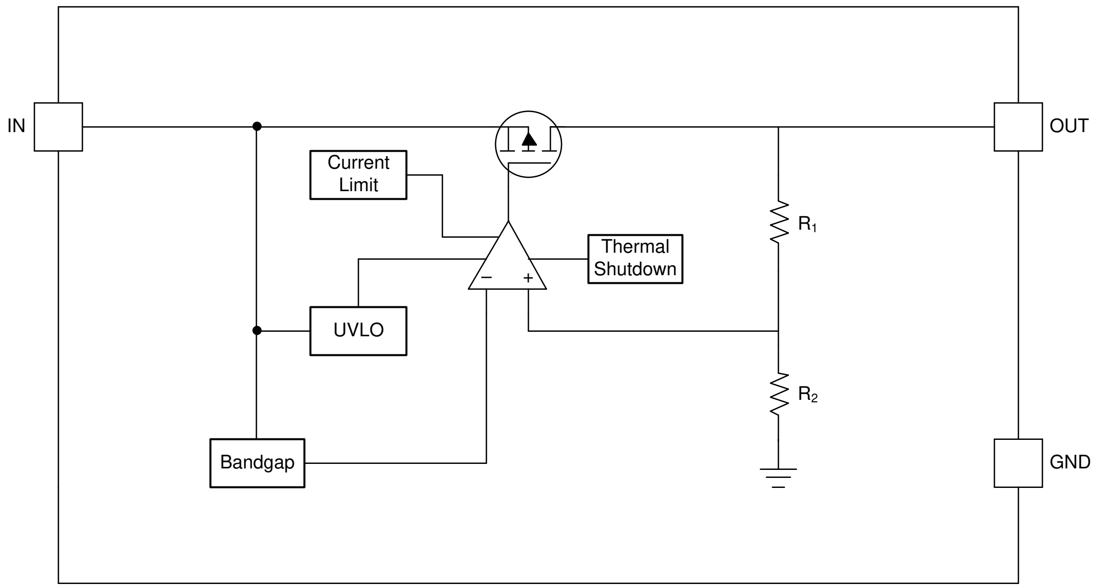

Figure 1-1. Functional Block Diagram

The TPS7B83-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the TPS7B83-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	20
Die FIT rate	8
Package FIT rate	12

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 500 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS ASICs analog and mixed ≤ 50-V supply	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TPS7B83-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
V_{OUT} high (following V_{IN})	40
V_{OUT} not in specification (voltage or timing)	15
V_{OUT} low (no output)	40
Short circuit any two pins	5

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS7B83-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the TPS7B83-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS7B83-Q1 data sheet.

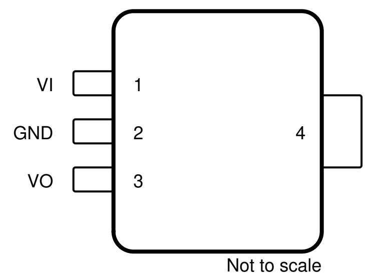

Figure 4-1. Pin Diagram

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN	1	No output voltage. System performance depends on upstream current limiting.	B
GND	2	No effect. Normal operation.	D
OUT	3	Current limit is triggered, and the device can repeatedly enter and exit thermal shutdown depending on power dissipation.	B
GND	4	No effect. Normal operation.	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN	1	Power is not supplied to the device, resulting in no output voltage.	B
GND	2	A floating GND pin can result in incorrect voltage regulation or no output voltage.	B
OUT	3	The output is disconnected from the load.	B
GND	4	A floating GND pin can result in incorrect voltage regulation or no output voltage.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
IN	1	GND	No output voltage. System performance depends on upstream current limiting.	B
GND	2	OUT	Current limit is triggered, and the device can repeatedly enter and exit thermal shutdown depending on power dissipation.	B
OUT	3	GND	Current limit is triggered, and the device can repeatedly enter and exit thermal shutdown depending on power dissipation.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN	1	No effect. Normal operation.	D
GND	2	No output voltage. System performance depends on upstream current limiting.	B
OUT	3	The output is not regulated. V_{OUT} = V_{IN}. The OUT pin can be damaged if the absolute maximum rating (7 V) is violated.	B/A
GND	4	No output voltage. System performance depends on upstream current limiting.	B

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