Functional Safety Information

ISOUSB211
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for the ISOUSB211 (DP-28 package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and the failure mode distribution (FMD) is based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

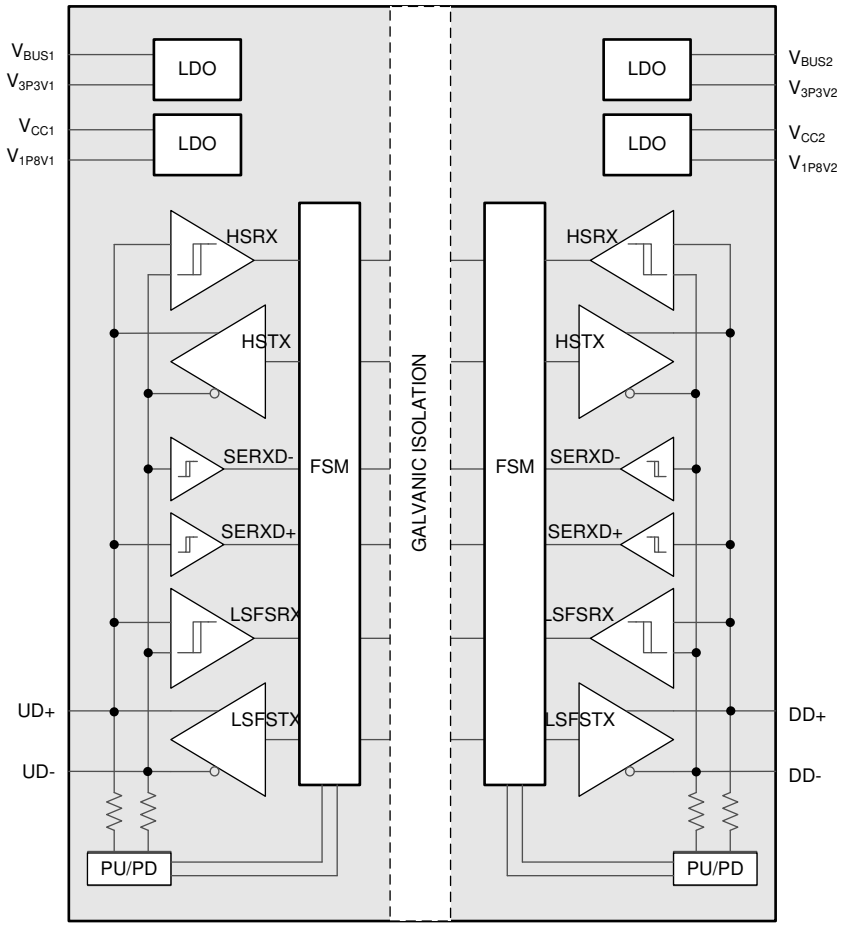

Figure 1-1. Functional Block Diagram

The ISOUSB211 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the ISOUSB211 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	35
Die FIT rate	7
Package FIT rate	28

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 1210mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	60 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the ISOUSB211 (DP-28 package) in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
DD+ and DD- stuck low DD+ or DD- stuck low	7.5
DD+ and DD- stuck high DD+ or DD- stuck high	7.5
DD+ and DD- undetermined DD+ or DD- undetermined	20
DD+ and DD- out of electrical or timing specification DD+ or DD- out of electrical or timing specification	15
UD+ and UD- stuck low UD+ or UD- stuck low	7.5
UD+ and UD- stuck high UD+ or UD- stuck high	7.5
UD+ and UD- undetermined UD+ or UD- undetermined	20
UD+ and UD- out of electrical or timing specification UD+ or UD- out of electrical or timing specification	15

The FMD in Table 3-1 excludes short-circuit faults across the isolation barrier. Faults for short circuits across the isolation barrier can be excluded according to IEC 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a safety-separated extra low voltage (SELV) or protective extra low voltage (PELV) power supply is used, pollution degree 2 / OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the ISOUSB211 (DP-28 package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the ISOUSB211 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the ISOUSB211 data sheet.

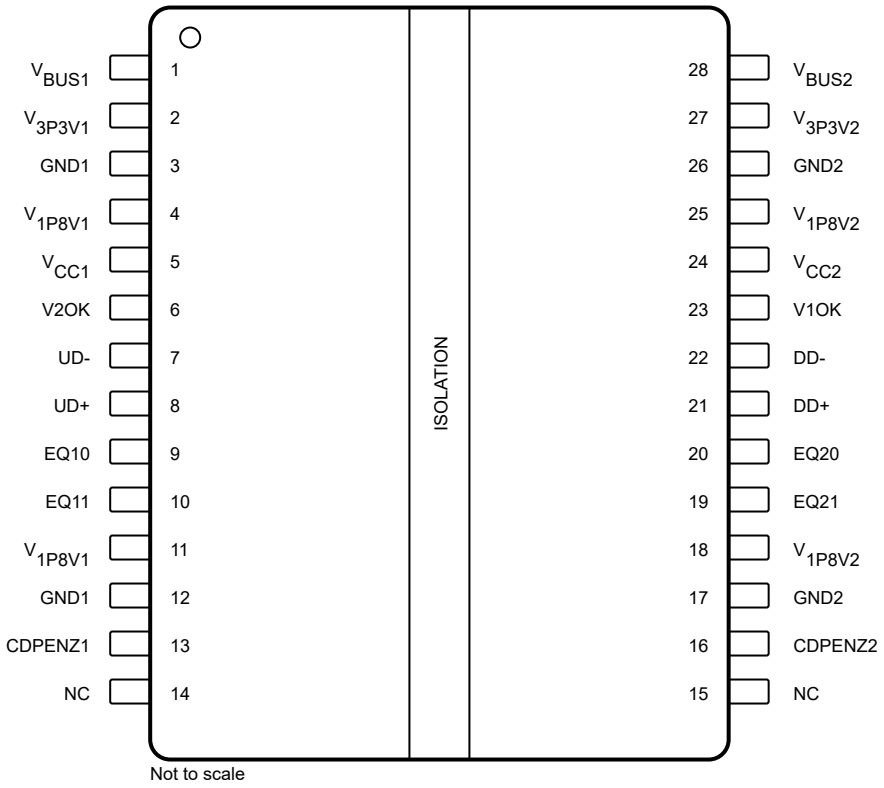

Figure 4-1. Pin Diagram

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VBUS1	1	No power to the device on side one. Observe that the absolute maximum ratings for all pins of the device are met; otherwise device damage is plausible.	A
V3P3V1	2	No power to the device on side one. Observe that the absolute maximum ratings for all pins of the device are met; otherwise device damage is plausible.	A
GND1	3	Device continues to function as expected. Normal operation.	D
V1P8V1	4	No power to the high-speed device on side one. Observe that the absolute maximum ratings for all pins of the device are met; otherwise device damage is plausible.	A
VCC1	5	No power to the high-speed device on side one. Observe that the absolute maximum ratings for all pins of the device are met; otherwise device damage is plausible.	A
V2OK	6	Loss of the indication of the power condition of side two.	A
UD-	7	Upstream facing port D- is shorted to ground. Loss of signal communication.	B
UD+	8	Upstream facing port D+ is shorted to ground. Loss of signal communication.	B
EQ10	9	EQ10 stuck low. Cannot set the EQ10 for higher equalization.	C
EQ11	10	EQ11 stuck low. Cannot set the EQ11 for higher equalization.	C
V1P8V1	11	No power to the high-speed device on side one. Observe that the absolute maximum ratings for all pins of the device are met; otherwise device damage is plausible.	A
GND1	12	Device continues to function as expected. Normal operation.	D
CDPENZ1	13	Charging downstream port (CDP) is advertized through the UD+ and UD- pins.	B
NC	14	Device continues to function as expected. Normal operation.	D
NC	15	Device continues to function as expected. Normal operation.	D
CDPENZ2	16	Charging downstream port (CDP) is advertized through the DD+ and DD- pins.	B
GND2	17	Device continues to function as expected. Normal operation.	D
V1P8V2	18	No power to the high-speed device on side two. Observe that the absolute maximum ratings for all pins of the device are met; otherwise device damage is plausible.	A
EQ21	19	EQ20 stuck low. Cannot set the EQ20 for higher equalization.	C
EQ20	20	EQ21 stuck low. Cannot set the EQ21 for higher equalization.	C
DD+	21	Downstream facing port D+ is shorted to ground. Loss of signal communication.	B
DD-	22	Downstream facing port D- is shorted to ground. Loss of signal communication.	B
V1OK	23	Loss of the indication that side one is powered up.	A
VCC2	24	No power to the high-speed device on side two. Observe that the absolute maximum ratings for all pins of the device are met; otherwise device damage is plausible.	A
V1P8V2	25	No power to the high-speed device on side two. Observe that the absolute maximum ratings for all pins of the device are met; otherwise device damage is plausible.	A
GND2	26	Device continues to function as expected. Normal operation.	D
V3P3V2	27	No power to the high-speed device on side two. Observe that the absolute maximum ratings for all pins of the device are met; otherwise device damage is plausible.	A
VBUS2	28	No power to the high-speed device on side two. Observe that the absolute maximum ratings for all pins of the device are met; otherwise device damage is plausible.	A

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VBUS1	1	VBUS1 has no power supply. If V3P3V1 connects to a power supply, the internal LDO can be damaged from the reverse current. If V3P3V1 does not connect to a power supply, observe that the absolute maximum ratings for all pins of the device are met; otherwise device damage is plausible.	A

Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
V3P3V1	2	If VBUS1 connects to a power supply ≥ 4.25V, the internal LDO is functioning and providing 3.3V to the circuitry. However, the 3.3V voltage output can have stability issues without proper external bypass capacitors. If VBUS1 does not connect to a power supply, observe that the absolute maximum ratings for all pins of the device are met; otherwise device damage is plausible.	A
GND1	3	Device continues to function as expected with potential degraded performance with pin 12 as GND1.	C
V1P8V1	4	Device continues to function as expected as pin 11 is functioning as the V1P8V1. Normal operation.	B
VCC1	5	VCC1 has no power supply. If V1P8V1 connects to a power supply, the internal LDO can be damaged from the reverse current. If V1P8V1 does not connect to a power supply, observe that the absolute maximum ratings for all pins of the device are met; otherwise device damage is plausible.	A
V2OK	6	Loss of the indication of the power condition of side two.	D
UD-	7	Upstream facing port D- is floating. Loss of signal communication.	B
UD+	8	Upstream facing port D+ is floating. Loss of signal communication.	B
EQ10	9	EQ10 is floating. Cannot adjust the EQ10.	C
EQ11	10	EQ11 is floating. Cannot adjust the EQ11.	C
V1P8V1	11	Device continues to function as expected as pin 4 is functioning as the V1P8V1. Normal operation.	B
GND1	12	Device continues to function as expected with potential degraded performance with pin 3 as GND1.	C
CDPENZ1	13	Loss of the ability to advertize CDP on the UD+ and UD- pins.	B
NC	14	Device continues to function as expected. Normal operation.	D
NC	15	Device continues to function as expected. Normal operation.	D
CDPENZ2	16	Loss of the ability to advertize CDP on the DD+ and DD- pins.	B
GND2	17	Device continues to function as expected with potential degraded performance with pin 26 as GND2.	C
V1P8V2	18	Device continues to function as expected as pin 25 is functioning as the V1P8V1. Normal operation.	B
EQ21	19	EQ21 is floating. Cannot adjust the EQ21.	C
EQ20	20	EQ20 is floating. Cannot adjust the EQ20.	C
DD+	21	Downstream facing port D- is floating. Loss of signal communication.	B
DD-	22	Downstream facing port D+ is floating. Loss of signal communication.	B
V1OK	23	Loss of the indication of the power condition of side one.	D
VCC2	24	VCC2 has no power supply. If V1P8V2 connects to a power supply, the internal LDO can be damaged from the reverse current. If V1P8V2 does not connect to a power supply, observe that the absolute maximum ratings for all pins of the device are met; otherwise device damage is plausible.	A
V1P8V2	25	No power to the high-speed device on side two. Observe that the absolute maximum ratings for all pins of the device are met; otherwise device damage is plausible. OUTD state is undetermined.	B
GND2	26	Device continues to function as expected with potential degraded performance with pin 17 as GND2.	C
V3P3V2	27	No power to the high-speed device on side two. Observe that the absolute maximum ratings for all pins of the device are met; otherwise device damage is plausible. OUTD state is undetermined.	A
VBUS2	28	No power to the high-speed device on side two. Observe that the absolute maximum ratings for all pins of the device are met; otherwise device damage is plausible. OUTD state is undetermined.	A

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
VBUS1	1	V3P3V1	If VBUS1 is connected to a power supply > 4.25V, the supply input exceeds the V3P3V1 absolute maximum rating and damage to the device is plausible.	A
V3P3V1	2	GND1	No power to the device on side one. Observe that the absolute maximum ratings for all pins of the device are met; otherwise device damage is plausible.	A
GND1	3	V1P8V1	No power to the device on side one. Observe that the absolute maximum ratings for all pins of the device are met; otherwise device damage is plausible.	A
V1P8V1	4	VCC1	If VCC1 is connected to a power supply > 2.1V, the supply input exceeds the V1P8V1 absolute maximum rating and damage to the device is plausible.	A
VCC1	5	V2OK	V2OK is stuck high.	A
V2OK	6	UD-	Loss of information for V2OK and UD-.	A
UD-	7	UD+	Loss of information for UD- and UD+.	B
UD+	8	EQ10	Loss of information for UD+ and EQ10.	B
EQ10	9	EQ11	EQ10 and QE11 are set to the same logic state.	C
EQ11	10	V1P8V1	EQ11 is set to 1.8V. EQ11 setting is undetermined.	C
V1P8V1	11	GND1	No power to the device on side one. Observe that the absolute maximum ratings for all pins of the device are met; otherwise device damage is plausible.	A
GND1	12	CDPENZ1	Loss of the ability to advertize CDP on the UD+ and UD- pins.	B
CDPENZ1	13	NC	Device continues to function as expected. Normal operation.	D
NC	14	CDPENZ1	Device continues to function as expected. Normal operation.	D
NC	15	CDPENZ2	Device continues to function as expected. Normal operation.	D
CDPENZ2	16	NC	Device continues to function as expected. Normal operation.	D
GND2	17	CDPENZ2	Loss of the ability to advertize CDP on the DD+ and DD- pins.	B
V1P8V2	18	GND2	No power to the device on side two. Observe that the absolute maximum ratings for all pins of the device are met; otherwise device damage is plausible.	A
EQ21	19	V1P8V2	EQ21 is set to 1.8V. EQ21 setting is undetermined.	C
EQ20	20	EQ21	EQ20 and QE21 are set to the same logic state.	C
DD+	21	EQ20	Loss of information for DD+ and EQ20.	B
DD-	22	DD+	Loss of information for DD- and DD+.	B
V1OK	23	DD-	Loss of information for V2OK and DD-.	A
VCC2	24	V1OK	V1OK is stuck high.	A
V1P8V2	25	VCC2	If VCC2 is connected to a power supply > 2.1V, the supply input exceeds the V1P8V2 absolute maximum rating and damage to the device is plausible.	A
GND2	26	V1P8V2	No power to the device on side two. Observe that the absolute maximum ratings for all pins of the device are met; otherwise device damage is plausible.	A
V3P3V2	27	GND2	No power to the device on side two. Observe that the absolute maximum ratings for all pins of the device are met; otherwise device damage is plausible.	A
VBUS2	28	V3P3V2	If VBUS2 is connected to a power supply > 4.25V, the supply input exceeds the V3P3V2 absolute maximum rating and damage to the device is plausible.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VBUS1	1	Device continues to function as expected. Normal operation.	D
V3P3V1	2	When shorted to the 5V supply, the supply input of the V3P3V1 pin exceeds the absolute maximum rating of 4.25V and damage to the device is plausible.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
GND1	3	Can create potential difference between pin 3 and pin 12 causing high current to flow in the device; damage to the device is plausible.	A
V1P8V1	4	When shorted to the 5V supply, the supply input of the V1P8V1 pin exceeds the absolute maximum rating of 2.1V and damage to the device is plausible.	A
VCC1	5	Device continues to function as expected. Normal operation.	D
V2OK	6	V2OK is stuck high. Loss of the indication of the power condition of side two.	A
UD-	7	Upstream facing port D- stuck high. Lost of signal communication.	B
UD+	8	Upstream facing port D+ is stuck high. Loss of signal communication.	B
EQ10	9	EQ10 is stuck high. Cannot adjust the EQ10.	C
EQ11	10	EQ11 is stuck high. Cannot adjust the EQ11.	C
V1P8V1	11	When shorted to the 5V, the supply input of the V1P8V1 pin exceeds the absolute maximum rating of 2.1V and damage to the device is plausible.	A
GND1	12	Can create potential difference between pin 3 and pin 12 causing high current to flow in the device; damage to the device is plausible.	A
CDPENZ1	13	CDPENZ1 is stuck high. Loss of the ability to advertize CDP on the UD+ and UD- pins.	B
NC	14	Device continues to function as expected. Normal operation.	D
NC	15	Device continues to function as expected. Normal operation.	D
CDPENZ2	16	CDPENZ2 is stuck high. Loss of the ability to advertize CDP on the DD+ and DD- pins.	B
GND2	17	Can create potential difference between pin 17 and pin 26 causing high current to flow in the device; damage to the device is plausible.	A
V1P8V2	18	When shorted to the 5V, the supply input of the V1P8V2 pin exceeds the absolute maximum rating of 2.1V and damage to the device is plausible.	A
EQ21	19	EQ21 is stuck high. Cannot adjust the EQ21.	C
EQ20	20	EQ20 is stuck high. Cannot adjust the EQ20.	C
DD+	21	Downstream facing port D- is stuck high. Loss of signal communication.	B
DD-	22	Downstream facing port D+ is stuck high. Loss of signal communication.	B
V1OK	23	V1OK is stuck high. Loss of the indication of the power condition of side one.	A
VCC2	24	Device continues to function as expected. Normal operation.	D
V1P8V2	25	When shorted to the 5V, the supply input of the V1P8V2 pin exceeds the absolute maximum rating of 2.1V and damage to the device is plausible.	A
GND2	26	Can create potential difference between pin 17 and pin 26 causing high current to flow in the device; damage to the device is plausible.	A
V3P3V2	27	When shorted to the 5V, the supply input of the V3P3V2 pin exceeds the absolute maximum rating of 4.25V and damage to the device is plausible.	A
VBUS2	28	Device continues to function as expected. Normal operation.	D

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
January 2025	*	Initial Release

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265