Functional Safety Information

ADS1013-Q1
Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

Trademarks

1 Overview

This document contains information for the ADS1013-Q1 (VSSOP and UQFN packages) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

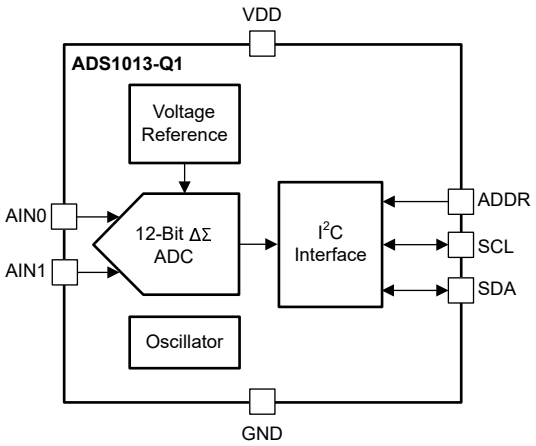

Figure 1-1. Functional Block Diagram

The ADS1013-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 VSSOP Package

This section provides functional safety failure in time (FIT) rates for the VSSOP package of the ADS1013-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	6
Die FIT rate	2
Package FIT rate	4

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 1.5 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 UQFN Package

This section provides functional safety failure in time (FIT) rates for the UQFN package of the ADS1013-Q1 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	4
Die FIT rate	2
Package FIT rate	2

The failure rate and mission profile information in Table 2-3 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 1.5 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for ADS1013-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Channel-channel short	10%
ADC output code bit error	20%
ADC gain out of specification	20%
ADC offset out of specification	20%
Communication error	30%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the ADS1013-Q1 (VSSOP and UQFN packages). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2 and Table 4-6)
- Pin open-circuited (see Table 4-3 and Table 4-7)
- Pin short-circuited to an adjacent pin (see Table 4-4 and Table 4-8)
- Pin short-circuited to VDD (see Table 4-5 and Table 4-9)

Table 4-2 through Table 4-9 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- RC filters on every analog input, AINx. Series resistors are sized to limit the input currents into the analog inputs to <10 mA in all circumstances (for example, if the device is unpowered and an input signal is applied).
- External pullup resistors on the SDA, SCL, and ALERT/RDY pins to VDD.
- External pulldown resistor on the ADDR pin to GND (I^2C address = 48h) or a pullup resistor to VDD (I^2C address = 49h). Other I^2C address configurations are not considered.
- NC pins are left unconnected.
- The device is the only target on the I^2C bus.

4.1 VSSOP Package

Figure 4-1 shows the ADS1013-Q1 pin diagram for the VSSOP package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the ADS1013-Q1 data sheet.

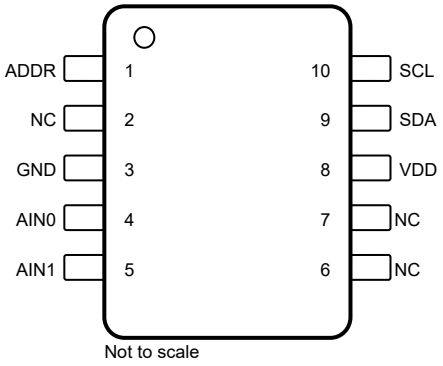

Figure 4-1. Pin Diagram (VSSOP) Package

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
ADDR	1	Pullup resistor on the ADDR pin to VDD: ADDR is stuck low. No I^2C communication with the device is possible because of change in I^2C address configuration.	B
		Pulldown resistor on the ADDR pin to GND: ADDR is stuck low. No effect. Normal operation.	D
NC	2	No effect. Normal operation.	D
GND	3	No effect. Normal operation.	D
AIN0	4	AIN0 is stuck low. Conversion results for multiplexer channel combinations using AIN0 are corrupted, unless AIN0 is tied to GND anyway.	B
AIN1	5	AIN1 is stuck low. Conversion results for multiplexer channel combinations using AIN1 are corrupted, unless AIN1 is tied to GND anyway.	B
NC	6	No effect. Normal operation.	D
NC	7	No effect. Normal operation.	D
VDD	8	The device is unpowered and not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage is plausible.	A
SDA	9	SDA is stuck low. No I^2C communication with the device is possible.	B
SCL	10	SCL is stuck low. No I^2C communication with the device is possible.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
ADDR	1	The state of the ADDR input is undetermined. The I^2C address of the device is undetermined. I^2C communication with the device is not possible if the host assumes a different I^2C address than the device is set to.	B
NC	2	No effect. Normal operation.	D
GND	3	Device functionality is undetermined. The device can be unpowered or connected to ground internally through an alternate pin ESD diode and power up.	B
AIN0	4	The state of the AIN0 input is undetermined. Conversion results for multiplexer channel combinations using AIN0 are undetermined.	B
AIN1	5	The state of the AIN1 input is undetermined. Conversion results for multiplexer channel combinations using AIN1 are undetermined.	B
NC	6	No effect. Normal operation.	D
NC	7	No effect. Normal operation.	D
VDD	8	Device functionality is undetermined. The device is unpowered if all external analog and digital pins are held low. The device can power up through internal ESD diodes to VDD if voltages above the device power-on reset threshold are present on any of the analog or digital pins.	B
SDA	9	No I^2C communication with the device is possible.	B
SCL	10	No I^2C communication with the device is possible.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
ADDR	1	NC	No effect. Normal operation.	D
NC	2	GND	No effect. Normal operation.	D
GND	3	AIN0	AIN0 is stuck low. Conversion results for multiplexer channel combinations using AIN0 are corrupted, unless AIN0 is tied to GND anyway.	B
AIN0	4	AIN1	Conversion results for multiplexer channel combinations using AIN0 or AIN1 are undetermined.	B
AIN1	5	NC	Not considered. Corner pin.	D
NC	6	NC	No effect. Normal operation.	D
NC	7	VDD	No effect. Normal operation.	D
VDD	8	SDA	SDA is stuck high. No I^2C communication with the device is possible. High SDA input current when the device tries to drive SDA low. Device damage is plausible.	A
SDA	9	SCL	I^2C communication is corrupted. No I^2C communication with the device is possible.	B
SCL	10	ADDR	Not considered. Corner pin.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to VDD

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
ADDR	1	Pullup resistor on the ADDR pin to VDD: ADDR is stuck high. No effect. Normal operation.	D
		Pulldown resistor on the ADDR pin to GND: ADDR is stuck high. No I^2C communication with the device is possible because of change in I^2C address configuration.	B
NC	2	No effect. Normal operation.	D
GND	3	The device is unpowered and not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage is plausible.	A
AIN0	4	AIN0 is stuck high. Conversion results for multiplexer channel combinations using AIN0 are corrupted, unless AIN0 is tied to VDD anyway.	B
AIN1	5	AIN1 is stuck high. Conversion results for multiplexer channel combinations using AIN1 are corrupted, unless AIN1 is tied to VDD anyway.	B
NC	6	No effect. Normal operation.	D
NC	7	No effect. Normal operation.	D
VDD	8	No effect. Normal operation.	D
SDA	9	SDA is stuck high. No I^2C communication with the device is possible. High SDA input current when the device tries to drive SDA low. Device damage is plausible.	A
SCL	10	SCL is stuck high. No I^2C communication with the device is possible.	B

4.2 UQFN Package

Figure 4-2 shows the ADS1013-Q1 pin diagram for the UQFN package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the ADS1013-Q1 data sheet.

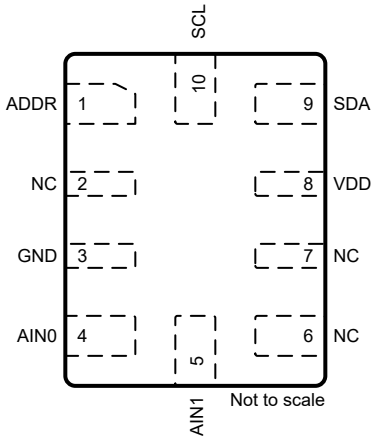

Figure 4-2. Pin Diagram (UQFN Package)

Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
ADDR	1	Pullup resistor on the ADDR pin to VDD: ADDR is stuck low. No I^2C communication with the device is possible because of change in I^2C address configuration.	B
		Pulldown resistor on the ADDR pin to GND: ADDR is stuck low. No effect. Normal operation.	D
NC	2	No effect. Normal operation.	D
GND	3	No effect. Normal operation.	D
AIN0	4	AIN0 is stuck low. Conversion results for multiplexer channel combinations using AIN0 are corrupted, unless AIN0 is tied to GND anyway.	B
AIN1	5	AIN1 is stuck low. Conversion results for multiplexer channel combinations using AIN1 are corrupted, unless AIN1 is tied to GND anyway.	B
NC	6	No effect. Normal operation.	D
NC	7	No effect. Normal operation.	D
VDD	8	The device is unpowered and not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage is plausible.	A
SDA	9	SDA is stuck low. No I^2C communication with the device is possible.	B
SCL	10	SCL is stuck low. No I^2C communication with the device is possible.	B

Table 4-7. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
ADDR	1	The state of the ADDR input is undetermined. The I^2C address of the device is undetermined. I^2C communication with the device is not possible if the host assumes a different I^2C address than the device is set to.	B
NC	2	No effect. Normal operation.	D
GND	3	Device functionality is undetermined. The device can be unpowered or connected to ground internally through an alternate pin ESD diode and power up.	B
AIN0	4	The state of the AIN0 input is undetermined. Conversion results for multiplexer channel combinations using AIN0 are undetermined.	B
AIN1	5	The state of the AIN1 input is undetermined. Conversion results for multiplexer channel combinations using AIN1 are undetermined.	B
NC	6	No effect. Normal operation.	D
NC	7	No effect. Normal operation.	D
VDD	8	Device functionality is undetermined. The device is unpowered if all external analog and digital pins are held low. The device can power up through internal ESD diodes to VDD if voltages above the device power-on reset threshold are present on any of the analog or digital pins.	B
SDA	9	No I^2C communication with the device is possible.	B
SCL	10	No I^2C communication with the device is possible.	B

Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
ADDR	1	NC	No effect. Normal operation.	D
NC	2	GND	No effect. Normal operation.	D
GND	3	AIN0	AIN0 is stuck low. Conversion results for multiplexer channel combinations using AIN0 are corrupted, unless AIN0 is tied to GND anyway.	B
AIN0	4	AIN1	Conversion results for multiplexer channel combinations using AIN0 or AIN1 are undetermined.	B
AIN1	5	NC	No effect. Normal operation.	D
NC	6	NC	No effect. Normal operation.	D
NC	7	VDD	No effect. Normal operation.	D
VDD	8	SDA	SDA is stuck high. No I^2C communication with the device is possible. High SDA input current when the device tries to drive SDA low. Device damage is plausible.	A
SDA	9	SCL	I^2C communication is corrupted. No I^2C communication with the device is possible.	B
SCL	10	ADDR	I^2C communication corrupted. No I^2C communication with the device is possible.	B

Table 4-9. Pin FMA for Device Pins Short-Circuited to VDD

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
ADDR	1	Pullup resistor on the ADDR pin to VDD: ADDR is stuck high. No effect. Normal operation.	D
		Pulldown resistor on the ADDR pin to GND: ADDR is stuck high. No I^2C communication with the device is possible because of change in I^2C address configuration.	B
NC	2	No effect. Normal operation.	D
GND	3	The device is unpowered and not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage is plausible.	A
AIN0	4	AIN0 is stuck high. Conversion results for multiplexer channel combinations using AIN0 are corrupted, unless AIN0 is tied to VDD anyway.	B
AIN1	5	AIN1 is stuck high. Conversion results for multiplexer channel combinations using AIN1 are corrupted, unless AIN1 is tied to VDD anyway.	B
NC	6	No effect. Normal operation.	D
NC	7	No effect. Normal operation.	D
VDD	8	No effect. Normal operation.	D
SDA	9	SDA is stuck high. No I^2C communication with the device is possible. High SDA input current when the device tries to drive SDA low. Device damage is plausible.	A
SCL	10	SCL is stuck high. No I^2C communication with the device is possible.	B

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