Functional Safety Information

TCAN1575-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for TCAN1575-Q1, which is a controller area network flexible data rate (CAN FD) transceiver in 14-pin SOIC (D), 14-pin VSON (DMT), and 14-pin SOT23 (DYY) packages, to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and the distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

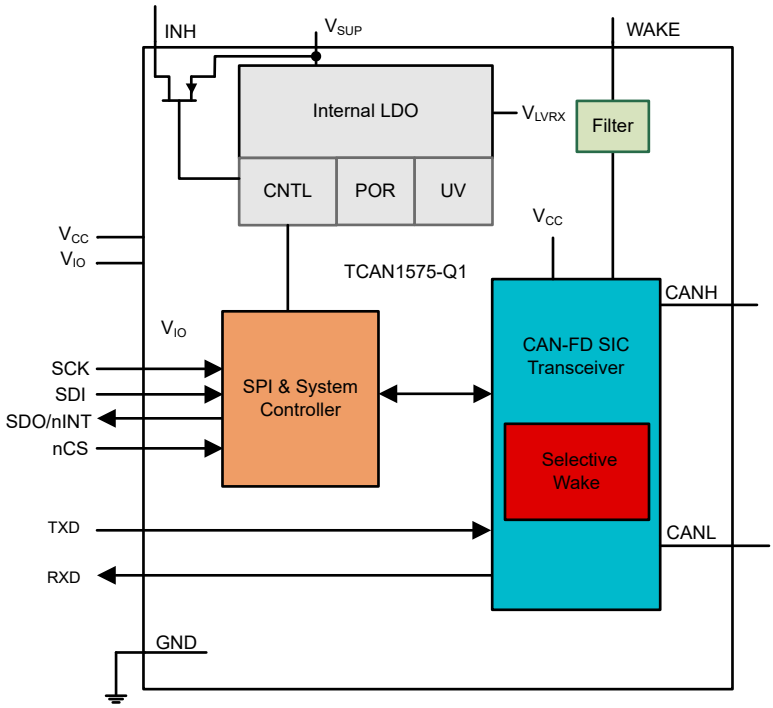

Figure 1-1. Functional Block Diagram

TCAN1575-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the 14-pin SOIC (D), 14-pin VSON (DMT), and 14-pin SOT23 (DYY) packages of the TCAN1575-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours) 14-pin SOIC (D)	FIT (Failures Per 10^9 Hours) 14-pin VSON (DMT)	FIT (Failures Per 10^9 Hours) 14-pin SOT23 (DYY)
Total component FIT rate	21	10	12
Die FIT rate	5	4	5
Package FIT rate	16	6	7

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 310mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog or mixed	60 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TCAN1575-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
CAN transceiver transmitter fail	23
CAN transceiver receiver fail	7
Power rail fail	14
Input or output fail	33
Digital core fail	23

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TCAN1575-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to VSUP (see Table 4-5)
- Pin short-circuited to VCC (see Table 4-6)
- Pin short-circuited to VIO (see Table 4-7)

Table 4-2 through Table 4-7 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the TCAN1575-Q1 pin diagrams. For TCAN1575-Q1, pin 6 only supports SDO output and pin 7 only supports INH output. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TCAN157x-Q1 data sheet.

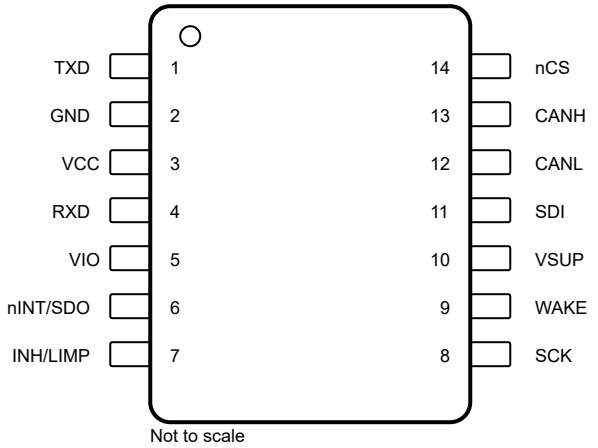

Figure 4-1. 14-pin SOIC (D) Pin Diagram, Top View

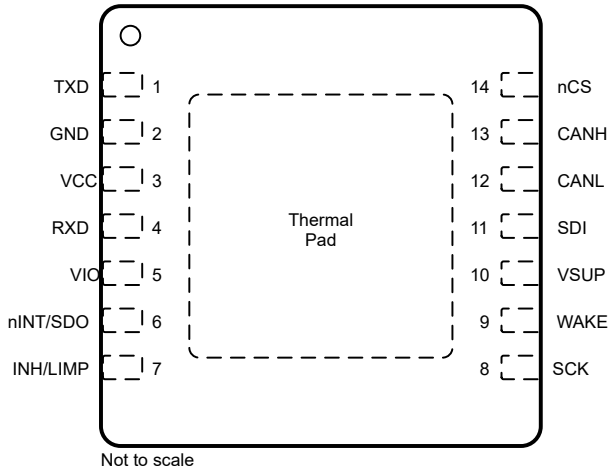

Figure 4-2. 14-pin VSON (DMT) Pin Diagram, Top View

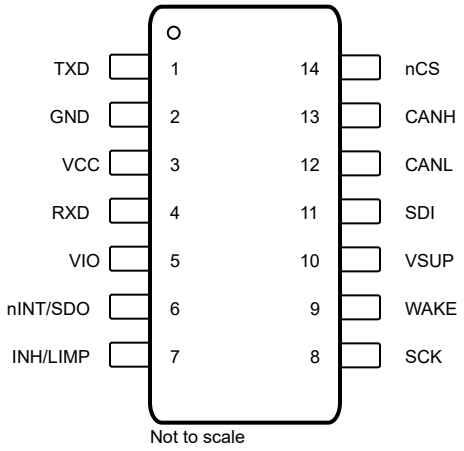

Figure 4-3. 14-pin SOT23 (DYY) Pin Diagram, Top View

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- All conditions are within the recommended operating conditions
- VSUP = see the recommended conditions in the device data sheet
- VCC = 4.75V to 5.25V
- VIO = 1.71V to 5.25V

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
TXD	1	Device enters dominant time out mode. Unable to transmit data from the processor to the CAN bus.	B
GND	2	None.	D
VCC	3	Transceiver not powered, high I_{CC} current.	B
RXD	4	Transceiver output biased dominant. Unable to send data from the CAN bus to the processor.	B
VIO	5	Digital pins are not powered, high I_{IO} current. No communication between the device and the processor is possible.	B
SDO	6	SDO biased low, no SPI read capability from the device to the processor.	B
INH	7	INH does not function, excessive VSUP current and not able to perform power enable function.	B
SCK	8	SCK is biased low, no SPI read or write capability between the device and the processor.	B
WAKE	9	Not able to transition to high, which does not allow the device to recognize a local wake up function.	B
VSUP	10	Device is not powered, high I_{SUP} current.	B
SDI	11	SDI is biased low, no SPI write capability from the processor to the device.	B
CANL	12	$V_{O(REC)}$ specification is violated. Degraded EMC performance.	B
CANH	13	Device cannot drive dominant to the bus, no communication is possible.	B
nCS	14	nCS is biased low, SPI is always active. Only the first SPI transaction after power-up functions as expected. New SPI frames do not work as expected.	C

Note

The VSON (DMT) package includes a thermal pad that is not always soldered to GND. Verify if the thermal pad is, or is not, soldered to GND.

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
TXD	1	Unable to transmit data from the processor to the CAN bus.	B
GND	2	Device is not powered.	B
VCC	3	Transceiver is not powered.	B
RXD	4	Unable to send data from the CAN bus to the processor.	B
VIO	5	Digital pins are not powered. Communication between the device and the processor is not possible.	B
SDO	6	SDO is internally biased to VIO. No SPI read capability from the device to the processor.	B
INH	7	INH is not able to perform a system power enable function.	B
SCK	8	SCK is internally biased to VIO. No SPI read or write capability between the device and the processor.	B
WAKE	9	Not able to transition, which does not allow the device to recognize a local wake up function.	B
VSUP	10	Device is not powered.	B
SDI	11	SDI is internally biased to VIO. No SPI write capability from the processor to the device.	B
CANL	12	Device cannot drive dominant to the bus, unable to communicate.	B
CANH	13	Device cannot drive dominant to the bus, unable to communicate.	B
nCS	14	nCS is internally biased to VIO. No SPI read or write capability between the device and the processor.	B

Note

The VSON (DMT) package includes a thermal pad that is not always soldered to GND. Verify if the thermal pad is, or is not, soldered to GND.

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
TXD	1	GND	Device enters dominant time out mode. Unable to transmit data from the processor to the CAN bus.	B
GND	2	VCC	Device is not powered, high I_{CC} current.	B
VCC	3	RXD	RXD output biased recessive, unable to communicate bus data to processor.	B
RXD	4	VIO	RXD output biased recessive, unable to communicate bus data to the processor.	B
VIO	5	SDO	No SPI read capability from the device to the processor.	B
SDO	6	INH	SDO pin is damaged due to high voltage.	A
SCK	8	WAKE	SCK pin can be damaged if WAKE pin is connected to VSUP.	A
WAKE	9	VSUP	Not able to transition to low, which does not allow the device to recognize a local wake up function.	B
VSUP	10	SDI	SDI pin is damaged and no SPI write communication from the processor to the device is possible.	A
SDI	11	CANL	SPI SDI bus line toggles on and off, based upon CAN traffic. During SPI communication, CANL can toggle, due to SDI traffic.	B
CANL	12	CANH	Bus is biased recessive, no communication is possible. I_{OS} current can be reached on CANH or CANL.	B
CANH	13	nCS	During SPI communication, CANH can be biased dominant.	B

Note

The VSON (DMT) package includes a thermal pad.

There is a chance, if the thermal pad is soldered down, that the thermal pad can short to any pin on the device. What the thermal pad is soldered to determines the behavior.

Example: If the thermal pad is soldered to a ground plane then the adjacent pins behave as if shorted to ground.

Table 4-5. Pin FMA for Device Pins Short-Circuited to VSUP Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
TXD	1	Absolute maximum violation, pin can be damaged. Unable to communicate from the processor to the CAN bus.	A
GND	2	Device is not powered, high I_{SUP} current, can damage the device.	A
VCC	3	Absolute maximum violation, pin can be damaged. Unable to communicate from the processor to the CAN bus.	A
RXD	4	Absolute maximum violation, pin can be damaged. Unable to communicate from the CAN bus to the processor.	A
VIO	5	Absolute maximum violation, pin can be damaged.	A
SDO	6	Absolute maximum violation, pin can be damaged. No SPI read capability from the device to the processor.	A
INH	7	INH is biased on and is not able to turn off.	B
SCK	8	Absolute maximum violation, pin can be damaged. No SPI read or write capability between the device and the processor.	A
WAKE	9	Not able to transition, which does not allow the device to recognize a local wake up function.	B
VSUP	10	None.	D
SDI	11	Absolute maximum violation, pin can be damaged, no SPI write capability from the processor to the device.	A
CANL	12	RXD is biased recessive, communication from the CAN bus to the processor is not possible. I_{OS} current can be reached.	B
CANH	13	$V_{O(REC)}$ specification is violated. Can degrade EMC performance.	C
nCS	14	Absolute maximum violation, transceiver can be damaged. No SPI read or write capability between the device and the processor.	A

Note

The VSON (DMT) package includes a thermal pad.

Table 4-6. Pin FMA for Device Pins Short-Circuited to VCC Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
TXD	1	TXD is biased recessive. Unable to transmit data from the processor to the CAN bus. Processor can be damaged if VCC > VIO.	B
GND	2	Device is not powered, high I_{CC} current.	B
VCC	3	None.	D
RXD	4	Transceiver output biased is recessive. Unable to send data from the CAN bus to the processor. Processor can be damaged if VCC > VIO.	B
VIO	5	IO pins operate as 5V inputs or outputs. Processor can be damaged if VCC > VIO.	C
SDO	6	No SPI read capability from the device to the processor. Processor can be damaged if VCC > VIO.	B
INH	7	Can damage the transceiver if absolute maximum voltage on VCC is exceeded.	A
SCK	8	No SPI read or write capability between the device and the processor. Processor can be damaged if VCC > VIO.	B
WAKE	9	Can damage transceiver if absolute maximum voltage on VCC is exceeded. Potentially not able to transition states, which prevents the device from recognizing a local wake up function.	A
VSUP	10	Absolute maximum violation on VCC, transceiver can be damaged. Unable to communicate from the processor to the CAN bus.	A
SDI	11	No SPI write capability from the processor to the device. Processor can be damaged if VCC > VIO.	B
CANL	12	RXD is always recessive, no communication is possible. I_{OS} current can be reached.	B
CANH	13	$V_{O(REC)}$ specification is violated, degraded EMC performance.	C
nCS	14	No SPI read or write capability between the device and the processor. Processor can be damaged if VCC > VIO.	B

Note

The VSON (DMT) package includes a thermal pad.

Table 4-7. Pin FMA for Device Pins Short-Circuited to VIO Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
TXD	1	TXD is biased recessive. Unable to transmit data from the processor to the CAN bus.	B
GND	2	Device is not powered, high I_{IO} current.	B
VCC	3	IO pins operate as 5V inputs or outputs. Processor can be damaged if VCC > VIO.	C
RXD	4	Transceiver output is biased recessive. Unable to send data from the CAN bus to the processor.	B
VIO	5	None.	D
SDO	6	No SPI read capability from the device to the processor.	B
INH	7	Can damage the transceiver if absolute maximum voltage on VIO is exceeded.	A
SCK	8	SCK is biased high. No SPI read or write capability between the device and the processor.	B
WAKE	9	Can damage the transceiver if absolute maximum voltage on VIO is exceeded. Potentially not able to transition states, which prevents the device from recognizing a local wake up function.	A
VSUP	10	Absolute maximum violation on the VIO pin, transceiver can be damaged.	A
SDI	11	SDI is biased high. No SPI write capability from the processor to the device.	B
CANL	12	RXD is biased recessive, no communication from the bus to the processor. I_{OS} current can be reached if VIO ≥ 3.3V.	B
CANH	13	$V_{O(REC)}$ specification is violated. Can degrade EMC performance.	C
nCS	14	nCS is biased high. No SPI read or write capability between the device and the processor.	B

Note

The VSON (DMT) package includes a thermal pad.

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
February 2025	*	Initial Release

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