Functional Safety Information

ADS131M08-Q1
Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

Trademarks

1 Overview

This document contains information for the ADS131M08-Q1 (TSSOP package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

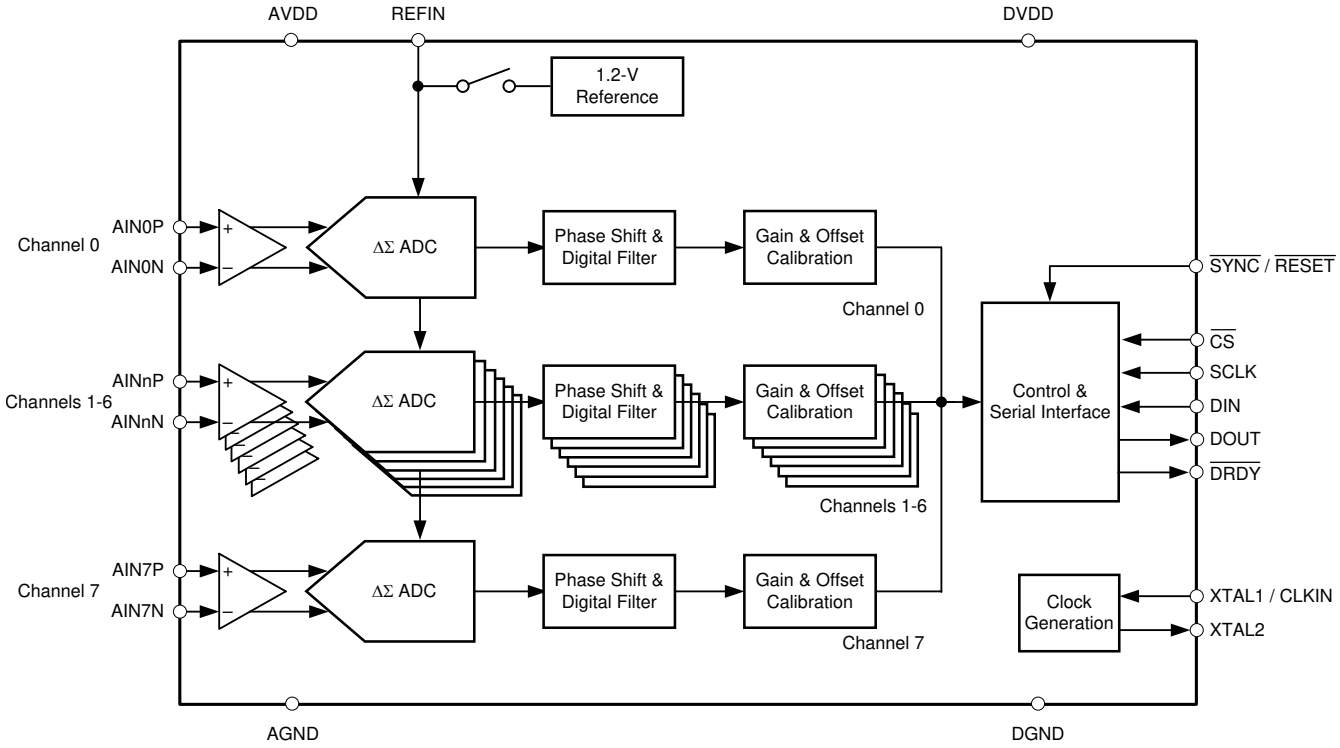

Figure 1-1. Functional Block Diagram

The ADS131M08-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the ADS131M08-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	18
Die FIT rate	2
Package FIT rate	16

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 25.8 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	60 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the ADS131M08-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Incorrect conversion result of an individual ADC(1) (for example, if the ADC output code is at positive or negative full scale, 0 V, undetermined, or is otherwise incorrect).	45%
SPI communication error	10%
Register bit error leading to incorrect device configuration (device behavior depends on which user or internal register bit is affected).	5%
Gain error of an individual ADC out of specification(1)	5%
Offset error of an individual ADC out of specification(1)	5%
Noise of the conversion result of an individual ADC out of specification(1)	5%
INL of an individual ADC out of specification(1)	5%
Gain error, INL, or noise of the conversion results of all four ADCs out of specification because of common circuitry (common circuitry includes the internal supplies, voltage reference, bias current generator, and clock).	5%
Crystal oscillator fault leading to an incorrect data rate (for example, if the oscillator frequency is too high or low, or if the oscillator output is stuck-at).	5%
The ADC output code bit is stuck-at	5%
Device behavior is undetermined	5%

(1) The failure mode percentage provided is for the sum of all four ADCs. For a single ADC, divide the failure mode percentage by 8x.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the ADS131M08-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the ADS131M08-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the ADS131M08-Q1 data sheet.

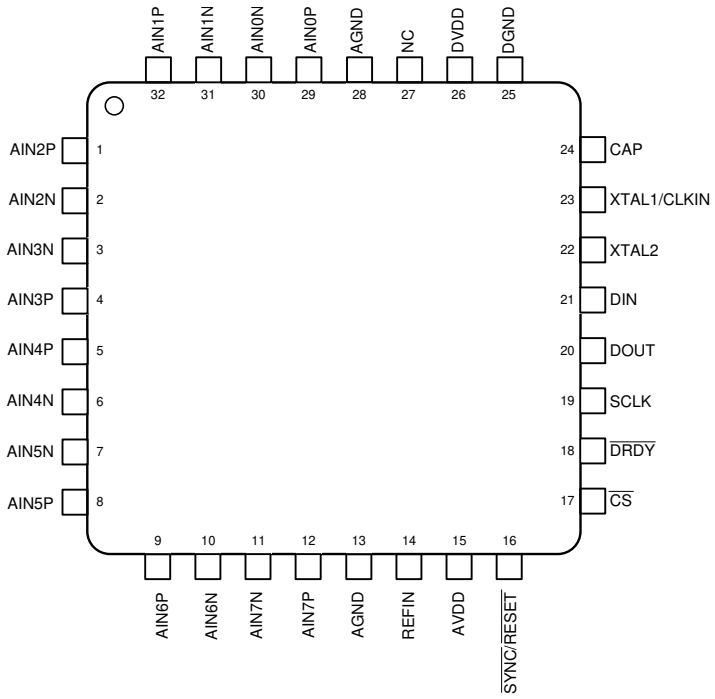

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- AVDD and DVDD use the same 3.3-V supply voltage.
- *Short-circuit to supply* means short AVDD to DVDD.
- *Short-circuit to ground* means short AGND to DGND.
- Differential RC filters on every ADC channel.
  Series resistors are sized to limit the input currents into the analog inputs to <10 mA in all circumstances (for example, if the device is unpowered and an input signal is applied).
- The device is the only peripheral on the SPI bus.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
AIN2P	1	AIN2P is stuck low. $V_{IN2} = V_{AIN2P} – V_{AIN2N} = AGND – V_{AIN2N}$. The conversion results of ADC2 are incorrect.	B
AIN2N	2	AIN2N is stuck low. $V_{IN2} = V_{AIN2P} – V_{AIN2N} = V_{AIN2P} – AGND$. The conversion results of ADC2 are incorrect.	B
AIN3N	3	AIN3N is stuck low. $V_{IN3} = V_{AIN3P} – V_{AIN3N} = V_{AIN3P} – AGND$. The conversion results of ADC3 are incorrect.	B
AIN3P	4	AIN3P is stuck low. $V_{IN3} = V_{AIN3P} – V_{AIN3N} = AGND – V_{AIN3N}$. The conversion results of ADC3 are incorrect.	B
AIN4P	5	AIN4P is stuck low. $V_{IN4} = V_{AIN4P} – V_{AIN4N} = AGND – V_{AIN4N}$. The conversion results of ADC4 are incorrect.	B
AIN4N	6	AIN4N is stuck low. $V_{IN4} = V_{AIN4P} – V_{AIN4N} = V_{AIN4P} – AGND$. The conversion results of ADC4 are incorrect.	B
AIN5N	7	AIN5N is stuck low. $V_{IN5} = V_{AIN5P} – V_{AIN5N} = V_{AIN5P} – AGND$. The conversion results of ADC5 are incorrect.	B
AIN5P	8	AIN5P is stuck low. $V_{IN5} = V_{AIN5P} – V_{AIN5N} = AGND – V_{AIN5N}$. The conversion results of ADC5 are incorrect.	B
AIN6P	9	AIN6P is stuck low. $V_{IN6} = V_{AIN6P} – V_{AIN6N} = AGND – V_{AIN6N}$. The conversion results of ADC6 are incorrect.	B
AIN6N	10	AIN6N is stuck low. $V_{IN6} = V_{AIN6P} – V_{AIN6N} = V_{AIN6P} – AGND$. The conversion results of ADC6 are incorrect.	B
AIN7N	11	AIN7N is stuck low. $V_{IN7} = V_{AIN7P} – V_{AIN7N} = V_{AIN7P} – AGND$. The conversion results of ADC7 are incorrect.	B
AIN7P	12	AIN7P is stuck low. $V_{IN7} = V_{AIN7P} – V_{AIN7N} = AGND – V_{AIN7N}$. The conversion results of ADC7 are incorrect.	B
AGND	13	No effect. Normal operation.	D
REFIN	14	REFIN is stuck low. The conversion results of all ADCs are incorrect.	B
AVDD	15	The device is unpowered and not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A
$\overline{\text{SYNC/RESET}}$	16	$\overline{\text{SYNC/RESET}}$ is stuck low. The device is held in reset.	B
$\overline{\text{CS}}$	17	$\overline{\text{CS}}$ is stuck low. Normal operation when trying to communicate with the ADS131M08-Q1.	B
$\overline{\text{DRDY}}$	18	$\overline{\text{DRDY}}$ is stuck low. No data-ready indication through the $\overline{\text{DRDY}}$ pin to the host is possible. An increase in supply current occurs when $\overline{\text{DRDY}}$ tries to drive high if the DRDY_HiZ bit = 0b. Device damage plausible if $\overline{\text{DRDY}}$ drives high for an extended period of time.	A
SCLK	19	SCLK is stuck low. No SPI communication with the device is possible.	B
DOUT	20	DOUT is stuck low. No SPI communication back to the host is possible. An increase in supply current occurs when DOUT tries to drive high. Device damage plausible if DOUT drives high for an extended period of time.	A
DIN	21	DIN is stuck low. No SPI communication with the device is possible.	B
XTAL2	22	The device is configured for use with a crystal oscillator: XTAL2 is stuck low. A clock is not provided to the device. The device is not functional, but SPI communication with the device is possible.	B
		The device is configured for use with an external clock: XTAL2 is stuck low. No effect. Normal operation.	D
XTAL1/CLKIN	23	XTAL1/CLKIN is stuck low. A clock is not provided to the device. The device is not functional, but SPI communication with the device is possible.	B
CAP	24	The device is unpowered and not functional.	B
DGND	25	No effect. Normal operation.	D
DVDD	26	The device is unpowered and not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A
NC	27	No effect. Normal operation.	D
AGND	28	No effect. Normal operation.	D
AIN0P	29	AIN0P is stuck low. $V_{IN0} = V_{AIN0P} – V_{AIN0N} = AGND – V_{AIN0N}$. The conversion results of ADC0 are incorrect.	B

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
AIN0N	30	AIN0N is stuck low. $V_{IN0} = V_{AIN0P} – V_{AIN0N} = V_{AIN0P} – AGND$. The conversion results of ADC0 are incorrect.	B
AIN1N	31	AIN1N is stuck low. $V_{IN1} = V_{AIN1P} – V_{AIN1N} = V_{AIN1P} – AGND$. The conversion results of ADC1 are incorrect.	B
AIN1P	32	AIN1P is stuck low. $V_{IN1} = V_{AIN1P} – V_{AIN1N} = AGND – V_{AIN1N}$. The conversion results of ADC1 are incorrect.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
AIN2P	1	The state of the AIN2P input is undetermined. The conversion results of ADC2 are undetermined.	B
AIN2N	2	The state of the AIN2N input is undetermined. The conversion results of ADC2 are undetermined.	B
AIN3N	3	The state of the AIN3N input is undetermined. The conversion results of ADC3 are undetermined.	B
AIN3P	4	The state of the AIN3P input is undetermined. The conversion results of ADC3 are undetermined.	B
AIN4P	5	The state of the AIN4P input is undetermined. The conversion results of ADC4 are undetermined.	B
AIN4N	6	The state of the AIN4N input is undetermined. The conversion results of ADC4 are undetermined.	B
AIN5N	7	The state of the AIN5N input is undetermined. The conversion results of ADC5 are undetermined.	B
AIN5P	8	The state of the AIN5P input is undetermined. The conversion results of ADC5 are undetermined.	B
AIN6P	9	The state of the AIN6P input is undetermined. The conversion results of ADC6 are undetermined.	B
AIN6N	10	The state of the AIN6N input is undetermined. The conversion results of ADC6 are undetermined.	B
AIN7N	11	The state of the AIN7N input is undetermined. The conversion results of ADC7 are undetermined.	B
AIN7P	12	The state of the AIN7P input is undetermined. The conversion results of ADC7 are undetermined.	B
AGND	13	Device functionality is undetermined. The device can be unpowered or connected to ground internally through an alternate pin ESD diode and power up.	B
REFIN	14	The state of the REFIN input is undetermined. The conversion results of all ADCs are undetermined.	B
AVDD	15	Device functionality is undetermined. The device is unpowered and not functional if all external analog pins are held low. The device can power up through internal ESD diodes to AVDD if voltages above the device power-on reset threshold are present on any of the analog pins.	B
$\overline{\text{SYNC}}$/$\overline{\text{RESET}}$	16	The state the of $\overline{\text{SYNC}}$/$\overline{\text{RESET}}$ input is undetermined. Device functionality is undetermined. The device can operate normally or be held in reset.	B
$\overline{\text{CS}}$	17	The state of the $\overline{\text{CS}}$ input is undetermined. SPI communication is corrupted.	B
$\overline{\text{DRDY}}$	18	The state of the $\overline{\text{DRDY}}$ output is undetermined. No data-ready indication through the $\overline{\text{DRDY}}$ pin to host is possible.	B
SCLK	19	The state of the SCLK input is undetermined. No SPI communication with the device is possible.	B
DOUT	20	The state of the DOUT output is undetermined. No SPI communication back to the host is possible.	B
DIN	21	The state of the DIN input is undetermined. No SPI communication with device is possible.	B
XTAL2	22	The device is configured for use with a crystal oscillator: the state of the XTAL2 input is undetermined. A clock is not provided to device. The device is not functional, but SPI communication with the device is possible.	B
		The device is configured for use with an external clock: the state of the XTAL2 input is undetermined. No effect. Normal operation.	D
XTAL1/CLKIN	23	The state of the XTAL1/CLKIN input is undetermined. A clock is not provided to the device. The device is not functional, but SPI communication with the device is possible.	B
CAP	24	The internal digital LDO is unstable. Device functionality is undetermined.	B
DGND	25	Device functionality is undetermined. The device can be unpowered or connected to ground internally through an alternate pin ESD diode and power up.	B
DVDD	26	Device functionality is undetermined. The device is unpowered and not functional if all external digital pins are held low. The device can power up through internal ESD diodes to DVDD if voltages above the device power-on reset threshold are present on any of the digital pins.	B
NC	27	No effect. Normal operation.	D
AGND	28	Device functionality is undetermined. The device can be unpowered or connected to ground internally through an alternate pin ESD diode and power up.	B
AIN0P	29	The state of the AIN0P input is undetermined. The conversion results of ADC0 are undetermined.	B
AIN0N	30	The state of the AIN0N input is undetermined. The conversion results of ADC0 are undetermined.	B
AIN1N	31	The state of the AIN1N input is undetermined. The conversion results of ADC1 are undetermined.	B
AIN1P	32	The state of the AIN1P input is undetermined. The conversion results of ADC1 are undetermined.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
AIN2P	1	AIN2N	$V_{IN2} = V_{AIN2P} – V_{AIN2N}$ = 0 V. The conversion result of ADC2 is approximately 0 V.	B
AIN2N	2	AIN3N	The conversion results of ADC2 and ADC3 are undetermined.	B
AIN3N	3	AIN3P	$V_{IN3} = V_{AIN3P} – V_{AIN3N}$ = 0 V. The conversion result of ADC3 is approximately 0 V.	B
AIN3P	4	AIN4P	The conversion results of ADC3 and ADC4 are undetermined.	B
AIN4P	5	AIN4N	$V_{IN4} = V_{AIN4P} – V_{AIN4N}$ = 0 V. The conversion result of ADC4 is approximately 0 V.	B
AIN4N	6	AIN5N	The conversion results of ADC4 and ADC5 are undetermined.	B
AIN5N	7	AIN5P	$V_{IN5} = V_{AIN5P} – V_{AIN5N}$ = 0 V. The conversion result of ADC5 is approximately 0 V.	B
AIN5P	8	AIN6P	Not considered. Corner pin.	D
AIN6P	9	AIN6N	$V_{IN6} = V_{AIN6P} – V_{AIN6N}$ = 0 V. The conversion result of ADC6 is approximately 0 V.	B
AIN6N	10	AIN7N	The conversion results of ADC6 and ADC7 are undetermined.	B
AIN7N	11	AIN7P	$V_{IN7} = V_{AIN7P} – V_{AIN7N}$ = 0 V. The conversion result of ADC7 is approximately 0 V.	B
AIN7P	12	AGND	AIN7P is stuck low. $V_{IN7} = V_{AIN7P} – V_{AIN7N}$ = AGND – V_{AIN7N}. The conversion results of ADC7 are incorrect.	B
AGND	13	REFIN	REFIN is stuck low. The conversion results of all ADCs are incorrect.	B
REFIN	14	AVDD	REFIN is stuck high. The conversion results of all ADCs are incorrect.	B
AVDD	15	$\overline{\text{SYNC}}/\overline{\text{RESET}}$	No effect. Normal operation. The device cannot be reset or synchronized using the $\overline{\text{SYNC}}/\overline{\text{RESET}}$ pin anymore.	B
$\overline{\text{SYNC}}/\overline{\text{RESET}}$	16	$\overline{\text{CS}}$	Not considered. Corner pin.	D
$\overline{\text{CS}}$	17	$\overline{\text{DRDY}}$	SPI communication is corrupted. No SPI communication with the device is possible. An increase in supply current is possible when $\overline{\text{DRDY}}$ tries to drive low when $\overline{\text{CS}}$ is driven high and vice versa. Device damage plausible if this condition exists for an extended period of time.	A
$\overline{\text{DRDY}}$	18	SCLK	SPI communication is corrupted. No SPI communication with the device is possible. An increase in supply current is possible when $\overline{\text{DRDY}}$ tries to drive low when SCLK is driven high and vice versa. Device damage plausible if this condition exists for an extended period of time.	A
SCLK	19	DOUT	SPI communication is corrupted. No SPI communication with the device is possible. An increase in supply current is possible when DOUT tries to drive low when SCLK is driven high and vice versa. Device damage plausible if this condition exists for an extended period of time.	A
DOUT	20	DIN	SPI communication is corrupted. No SPI communication with the device is possible. An increase in supply current is possible when DOUT tries to drive low when DIN is driven high and vice versa. Device damage plausible if this condition exists for an extended period of time.	A
DIN	21	XTAL2	The device is configured for use with a crystal oscillator: SPI communication is corrupted. No SPI communication with the device is possible. The XTAL2 signal is corrupted. Device behavior is undetermined.	B
			The device is configured for use with an external clock: no effect. Normal operation as long as DIN can drive the pulldown resistor between XTAL2 and DGND.	D
XTAL2	22	XTAL1/CLKIN	XTAL1/CLKIN and XTAL2 are shorted. A clock is not provided to the device. The device is not functional, but SPI communication with the device is possible.	B
XTAL1/CLKIN	23	CAP	Device behavior is undetermined. Device damage plausible when the XTAL1/CLKIN pin drives the digital core LDO output on the CAP pin to >1.8 V.	A
CAP	24	DGND	Not considered. Corner pin.	D

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
DGND	25	DVDD	The device is unpowered and not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A
DVDD	26	NC	No effect. Normal operation.	D
NC	27	AGND	No effect. Normal operation.	D
AGND	28	AIN0P	AIN0P is stuck low. $V_{IN0} = V_{AIN0P} – V_{AIN0N} = AGND – V_{AIN0N}$. The conversion results of ADC0 are incorrect.	B
AIN0P	29	AIN0N	$V_{IN0} = V_{AIN0P} – V_{AIN0N} = 0$ V. The conversion result of ADC0 is approximately 0 V.	B
AIN0N	30	AIN1N	The conversion results of ADC0 and ADC1 areundetermined.	B
AIN1N	31	AIN1P	$V_{IN1} = V_{AIN1P} – V_{AIN1N} = 0$ V. The conversion result of ADC1 is approximately 0 V.	B
AIN1P	32	AIN2P	Not considered. Corner pin.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
AIN2P	1	AIN2P is stuck high. $V_{IN2} = V_{AIN2P} – V_{AIN2N} = AVDD – V_{AIN2N}$. The conversion results of ADC2 are incorrect.	B
AIN2N	2	AIN2N is stuck high. $V_{IN2} = V_{AIN2P} – V_{AIN2N} = V_{AIN2P} – AVDD$. The conversion results of ADC2 are incorrect.	B
AIN3N	3	AIN3N is stuck high. $V_{IN3} = V_{AIN3P} – V_{AIN3N} = V_{AIN3P} – AVDD$. The conversion results of ADC3 are incorrect.	B
AIN3P	4	AIN3P is stuck high. $V_{IN3} = V_{AIN3P} – V_{AIN3N} = AVDD – V_{AIN3N}$. The conversion results of ADC3 are incorrect.	B
AIN4P	5	AIN4P is stuck high. $V_{IN4} = V_{AIN4P} – V_{AIN4N} = AVDD – V_{AIN4N}$. The conversion results of ADC4 are incorrect.	B
AIN4N	6	AIN4N is stuck high. $V_{IN4} = V_{AIN4P} – V_{AIN4N} = V_{AIN4P} – AVDD$. The conversion results of ADC4 are incorrect.	B
AIN5N	7	AIN5N is stuck high. $V_{IN5} = V_{AIN5P} – V_{AIN5N} = V_{AIN5P} – AVDD$. The conversion results of ADC5 are incorrect.	B
AIN5P	8	AIN5P is stuck high. $V_{IN5} = V_{AIN5P} – V_{AIN5N} = AVDD – V_{AIN5N}$. The conversion results of ADC5 are incorrect.	B
AIN6P	9	AIN6P is stuck high. $V_{IN6} = V_{AIN6P} – V_{AIN6N} = AVDD – V_{AIN6N}$. The conversion results of ADC6 are incorrect.	B
AIN6N	10	AIN6N is stuck high. $V_{IN6} = V_{AIN6P} – V_{AIN6N} = V_{AIN6P} – AVDD$. The conversion results of ADC6 are incorrect.	B
AIN7N	11	AIN7N is stuck high. $V_{IN7} = V_{AIN7P} – V_{AIN7N} = V_{AIN7P} – AVDD$. The conversion results of ADC7 are incorrect.	B
AIN7P	12	AIN7P is stuck high. $V_{IN7} = V_{AIN7P} – V_{AIN7N} = AVDD – V_{AIN7N}$. The conversion results of ADC7 are incorrect.	B
AGND	13	The device is unpowered and not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A
REFIN	14	REFIN is stuck high. The conversion results of all ADCs are incorrect.	B
AVDD	15	No effect. Normal operation.	D
$\overline{\text{SYNC/RESET}}$	16	No effect. Normal operation. The device cannot be reset or synchronized using the $\overline{\text{SYNC/RESET}}$ pin anymore.	B
$\overline{\text{CS}}$	17	$\overline{\text{CS}}$ is stuck high. No SPI communication with the device is possible.	B
$\overline{\text{DRDY}}$	18	$\overline{\text{DRDY}}$ is stuck high. No data-ready indication through the $\overline{\text{DRDY}}$ pin to the host is possible. An increase in supply current occurs when $\overline{\text{DRDY}}$ tries to drive low. Device damage plausible if $\overline{\text{DRDY}}$ drives low for an extended period of time.	A
SCLK	19	SCLK is stuck high. No SPI communication with the device is possible.	B
DOUT	20	DOUT is stuck high. No SPI communication back to the host is possible. An increase in supply current occurs when DOUT tries to drive low. Device damage plausible if DOUT drives low for an extended period of time.	A
DIN	21	DIN is stuck high. No SPI communication with the device is possible.	B
XTAL2	22	The device is configured for use with a crystal oscillator: XTAL2 is stuck high. A clock is not provided to the device. The device is not functional, but SPI communication with the device is possible.	B
		The device is configured for use with an external clock: XTAL2 is stuck high. No effect. Normal operation.	D
XTAL1/CLKIN	23	XTAL1/CLKIN is stuck high. A clock is not provided to the device. The device is not functional, but SPI communication with the device is possible.	B
CAP	24	The device can operate normally, but permanent device damage within a short period of time is very plausible. The device is not functional anymore in case of damage.	A
DGND	25	The device is unpowered and not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A
DVDD	26	No effect. Normal operation.	D
NC	27	No effect. Normal operation.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
AGND	28	The device is unpowered and not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A
AIN0P	29	AIN0P is stuck high. $V_{IN0} = V_{AIN0P} – V_{AIN0N} = AVDD – V_{AIN0N}$. The conversion results of ADC0 are incorrect.	B
AIN0N	30	AIN0N is stuck high. $V_{IN0} = V_{AIN0P} – V_{AIN0N} = V_{AIN0P} – AVDD$. The conversion results of ADC0 are incorrect.	B
AIN1N	31	AIN1N is stuck high. $V_{IN1} = V_{AIN1P} – V_{AIN1N} = V_{AIN1P} – AVDD$. The conversion results of ADC1 are incorrect.	B
AIN1P	32	AIN1P is stuck high. $V_{IN1} = V_{AIN1P} – V_{AIN1N} = AVDD – V_{AIN1N}$. The conversion results of ADC1 are incorrect.	B

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